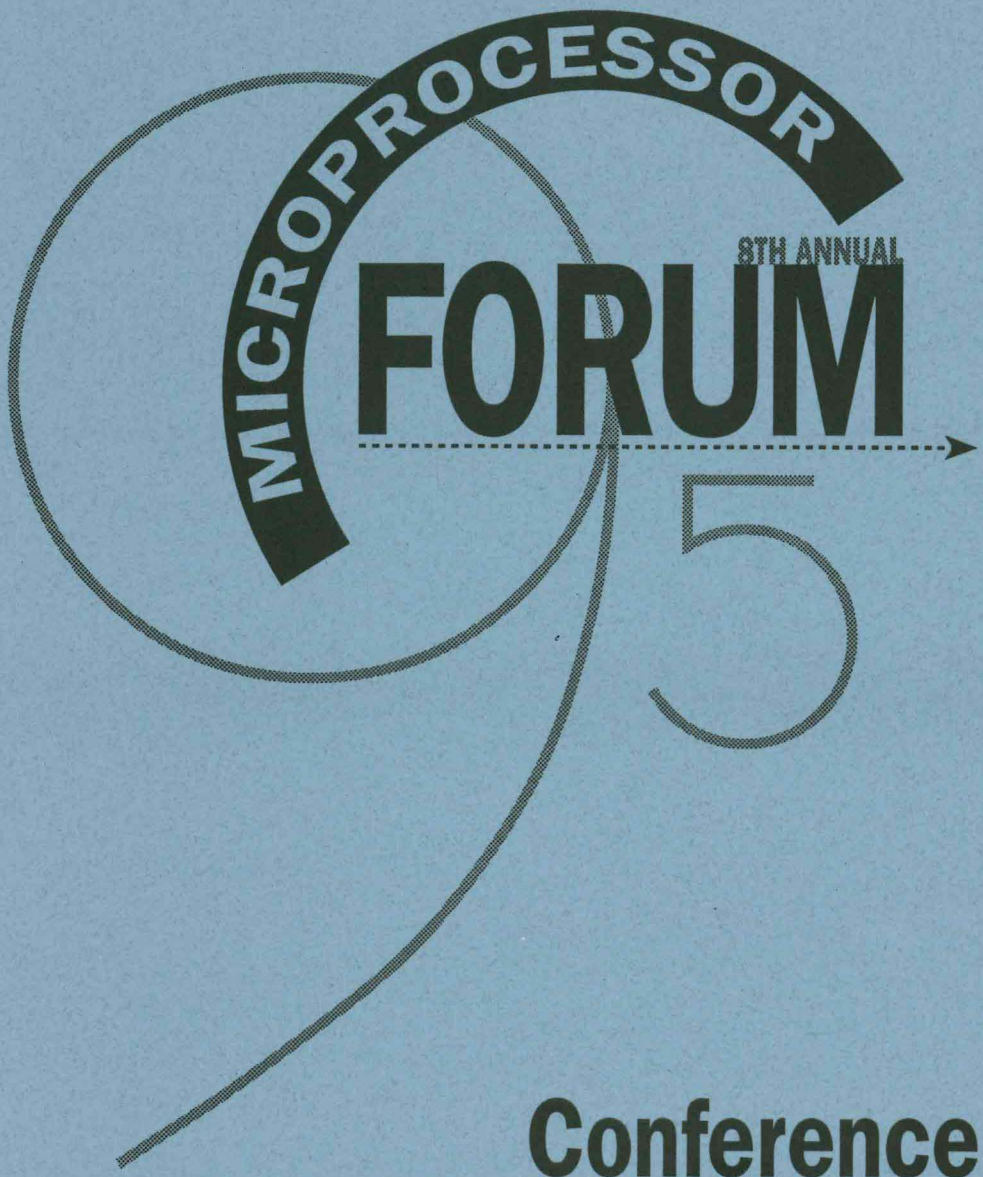

Conference Materials

Fairmont Hotel, San Jose
October 10-11, 1995

Sponsored by

MICRODESIGN RESOURCES

DAY ONE Tuesday, October 10

8:30 **WELCOME** *Michael Slater*

8:40 **KEYNOTE: SEMICONDUCTOR TECHNOLOGY AND THE GROWTH OF THE PC INDUSTRY**
Craig Barrett, Intel

9:20 **X86 MICROPROCESSORS** *Moderator: Michael Slater, MicroDesign Resources*

Shifting Sands in the x86 Landscape
Michael Slater

P6: The Myths and Realities
Robert Colwell, Intel

10:00 **BREAK: SPONSORED BY NEC ELECTRONICS**

AMD-K5 Performance and Microarchitecture Tradeoffs
David Witt, AMD

Optimizing the M1 for Windows 95
Mark Bluhm, Cyrix

Overview of the Nx686 Processor
Greg Favor, NexGen

Q&A Panel
All Speakers above

12:00 **LUNCH**

1:10 Market Trends for x86 Microprocessors
Aaron Goldberg, Computer Intelligence InfoCorp

1:30 **PROCESSORS FOR MULTIMEDIA** *Moderator: Yong Yao, MicroDesign Resources*

Implementation Strategies for Multimedia
Yong Yao

Architecture of a Broadband Mediaprocessor
John Moussouris, MicroUnity

A VLIW and SIMD Vector Processor for PC Multimedia
Stephen Purcell, Chromatic

The TriMedia VLIW-Based PCI Multimedia Processor
Gerrit Slavenburg, Philips Semiconductors

2:50 **BREAK: SPONSORED BY LSI LOGIC**

3:10 M.F.A.S.T: A Highly Parallel, Scalable, Single-Chip DSP
Gerald Pechanek, IBM Microelectronics

UltraSPARC's Instruction Set Extensions for Multimedia
Marc Tremblay, Sun Microsystems

A Multimedia 586 Processor for Consumer PCs
Forrest Norrod, Cyrix

Q&A Panel
All speakers above

5:00 **MICROPROCESSOR REPORT AWARDS**
Nick Tredennick, Tredennick, Inc.

5:30 **RECEPTION/LITERATURE & DEMONSTRATION CENTER OPENING**

8:30PM-10:30PM **AFFINITY SESSIONS**

Open Session on Cryptography
Packaging Technology Directions
Benchmarks & Workloads Roundtable
The Issue of Branding Microprocessors

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DAY TWO Wednesday, October 11

8:30 EMBEDDED PROCESSORS
Moderator: James L. Turley, MicroDesign Resources

Ubiquitous Computers: The New Embedded Applications
James L. Turley

Bringing RISC Technology to Communications
Robert O'Dell, Motorola

An Integrated i960 to Enhance Server and Network I/O
Elliot Garbus, Intel

SH-DSP & SH-FPU: Optimized Communication & Consumer Microprocessors
Jim Slager, Hitachi

StrongARM Reaches for Ever Higher Performance
Rich Witek, Digital

10:20 BREAK: SPONSORED BY FUJITSU MICROELECTRONICS

A Scalable 64-bit RISC for Custom Designs
Bob Caulk, LSI Logic

A PowerPC Core for Cost-Sensitive Consumer Applications
Kim O'Donnell, IBM

A Next-Generation DSP Solution for Communications Applications & Beyond
Roman Robles, Motorola

Q&A Panel
All speakers above

12:00 LUNCH

1:10 HIGH-PERFORMANCE RISC MICROPROCESSORS
Moderator: Linley Gwennap, MicroDesign Resources

RISC Processors: Generations
Linley Gwennap

PA-7300LC: A Highly Integrated System on a Chip
Tom Meyer, Hewlett-Packard

The Performance of PowerPC 603e and 604e Microprocessors
Kaivalya Dixit, IBM

Colorado 4 Extends 32-bit SPARC Performance
Mitch Alsup, Ross Technology

2:30 BREAK: SPONSORED BY MIPS TECHNOLOGIES

UltraSPARC2: Advancing SPARC Performance
Anant Agrawal, Sun Microsystems

Alpha 21164A: Continued Performance Leadership
Pete Bannon, Digital Semiconductor

Q&A Panel
All speakers above

4:10 PANEL: FUTURE OF MICROPROCESSOR SYSTEM ARCHITECTURE
Moderator: Michael Slater

Dirk Meyer, Digital
Lin Nease, Hewlett-Packard
Don North, Apple
Richard Oehler, IBM
Fred Pollack, Intel
George White, Corollary

5:00 WRAP-UP *Michael Slater*

5:10 CONFERENCE ADJOURNED

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Michael Slater, moderator
Founder and President of MicroDesign Resources, Michael Slater serves as the Editorial Director and Publisher of *Microprocessor Report* and Director of the Microprocessor Forum. He is internationally recognized as a leading authority on microprocessor technology and system trends. Michael has lectured at Stanford University, Santa Clara University, and National Technological University. He has presented hundreds of seminars and consults regularly for companies including IBM, Apple, Sun, Intel, Motorola, AMD, Amdahl, Digital, and Tektronix. He is a columnist for *Electronic Engineering Times*, *Nikkei Electronics Asia*, and *Computer Shopper*, and he has written for many computer publications.

Linley Gwennap, moderator
is Editor-in-Chief of *Microprocessor Report* and Director of Product Development for MicroDesign Resources. He joined MDR in 1992 after eight years at Hewlett-Packard working on RISC systems. His positions at HP included Product Manager for the HP PA7100 microprocessor, Program Manager for the HP9000 model 815, and System Designer for the HP9000 model 870. He currently consults on microprocessor developments and strategies for leading processor and system vendors.

James Turley, moderator
Senior Analyst and Senior Editor of *Microprocessor Report*, specializing in high-performance embedded microprocessors, Jim joined MDR in 1994 after devoting more than a dozen years to design engineering, engineering management, product marketing, and program management. He has designed embedded processors into a variety of products and developed both hardware and software for leading companies around Silicon Valley and in Europe. He has also conducted numerous seminars and training courses.

Yong Yao, moderator
Director of the Technology Roadmap Service and Senior Analyst for PC technology for *Microprocessor Report*, is the most recent addition to the MicroDesign Resources staff of analysts. Prior to joining MDR, Yong was with Vitesse Semiconductor, where he was the director of product planning as well as the designer of the multiprocessor V-Bus.

Craig Barrett, keynote speaker
is Executive Vice President and Chief Operating Officer of Intel Corporation, having corporate-wide responsibility for internal operations of the company. He joined Intel in 1974 and served in various technical and business management positions. In 1984 Dr. Barrett was named a Vice President, and he became General Manager of the Components Technology and Manufacturing Group in 1985. Dr. Barrett was named a Senior Vice President in 1987 and became comanager of the Microcomputer Components Group in 1989. He was promoted to the post of Executive Vice President in 1990. Dr. Barrett was elected to the Board of Directors in 1992 and was named Chief Operating Officer in January 1993.

Anant Agrawal is Vice President of Engineering for Sun's SPARC Technology Business. He has been involved in the design and development of the SPARC microprocessors at Sun since 1984.

Mitch Alsup is ROSS Technology's Chief Architect for its SPARC CPU product line. Mitch joined ROSS in 1991 from Motorola, where he was the Architect of Motorola's 88000.

Peter Bannon is a Consulting Engineer with Digital Semiconductor, Pete has participated in the design or verification of several microprocessor chips and was a member of the Alpha 21164 architecture team.

Mark Bluhm is the Chief Architect of Cyrix's M1 as well as director of engineering responsible for all future superscalar processors. As one of Cyrix's initial design engineers, Mark helped define and design several generations of wholly original x86 processors and math coprocessors.

Bob Caulk has spent the last six years at LSI Logic leading architecture definition and product development for LSI's MIPS RISC processor family of embedded cores and derivative products.

Robert Colwell manages the P6 architecture organization at Intel. Bob joined Intel in 1990 as a Senior Architect on the P6 project, and became manager of the architecture group two years later. Prior to Intel he was a CPU architect at Multiflow Computer.

Kaivalya Dixit is IBM's Director of Perfomance. Previous to joining IBM, he was Engineering Program Manager at SUN Microsystems.

Gregory Favor is NexGen's Director of 686 Processor Development. Previous to his appointment to the Director position he was the Chief Processor Architect.

Elliot Garbus is Strategic Development Manager in Intel's Semiconductor Products Group. Elliot has participated in the definition of the three generations of 80960 microprocessor products. He is currently working on products to enhance the I/O performance of servers.

Aaron Goldberg is Executive Vice President of Computer Intelligence InfoCorp. Prior to joining InfoCorp in 1992, Aaron was Senior Vice President of the Desktop Computing Group at International Data Corporation.

Dirk Meyer is the Lead Architect of Digital's third-generation high-end Alpha microprocessor. Dirk was a co-microarchitect of Digital's first-generation Alpha 21064 microprocessor and an original member of the Alpha CPU team.

Tom Meyer is currently a member of Hewlett-Packard's Systems Technology Division and Project Manager for the PA7300LC integrated memory and I/O controller. Previously he worked on the PA7100LC and the memory controller for several of the HP9000 Series computers.

John Moussouris is President and CEO of MicroUnity Systems Engineering, which he founded in 1988. Prior to that John was Vice President of VLSI Development at MIPS Computer Systems.

Lin Nease has been a System Architect for several of Hewlett-Packard's UNIX server products, including the G-, H-, and I-class midrange/low-end systems. He has been involved in the development of HP's commercial UNIX servers since the advent of that product line.

Forrest Norrod is Program Manager and Principal Architect of the multimedia 586 CPU at Cyrix. Prior to joining Cyrix in 1993, Forrest was with Hewlett-Packard, where he designed advanced 3D graphic systems.

Don North has been associated with the Advanced Technology Group at Apple since its inception in 1985, and currently manages a systems architecture research group. His current research interests include high-performance system interconnect issues and multiprocessor systems architecture.

Richard Oehler is the Director of Systems Software in the Power Personal Systems Division at IBM. In over 20 years with IBM he has been involved in development of the 801, the first RISC machine, was lead architect for the the RISC System/6000, and is responsible for all dealings on PowerPC. In 1994 Rich became an IBM Fellow.

Robert O'Dell has played a significant role in the definition of Motorola's integrated communications controller family of products. Robert is currently the Applications Manager for the Data Communications Operation in the High Performance Embedded Systems Division of Motorola's Semiconductor Products Sector.

Kim O'Donnell, as Senior Engineering Manager for IBM, is responsible for the design and development of the IBM PowerPC 400 Series of Embedded Controllers.

Gerald Pechanek, at IBM Microelectronics Mwave group, is involved in the research and development of parallel computer architectures for graphics-, video-, neural-, and signal-processing multimedia applications.

Fred Pollack is director of the group responsible for all Intel platform architecture and performance analysis. He also directs the planning for Intel's future microprocessors. Prior to this, he was the manager of the P6 architecture. In January of 1993 he was promoted to an Intel Fellow, one of nine in the company.

Stephen Purcell is co-founder of Chromatic. He was previously a founder and Chief Architect at C-Cube Microsystems where he created the architecture for four generations of video CODECs, including the VideoRISC processor.

Roman Robles is manager of Motorola's 24- and 32-bit DSP applications group. He has worked in Motorola's DSP applications group for the past five years, focusing primarily on Motorola's industry-standard 24-bit DSP56000 architecture and applications.

Jim Slager specializes in microprocessor and multimedia products, Jim is Director of Advanced Product Planning at Hitachi Micro Systems. He participated in the design of the 286, 386, and 486 at Intel and was involved in SPARC design at Sun Microsystems.

Gerrit Slavenberg, Chief Scientist, TriMedia technology, for Philips Semiconductors, Gert is responsible for development of current and future TriMedia products.

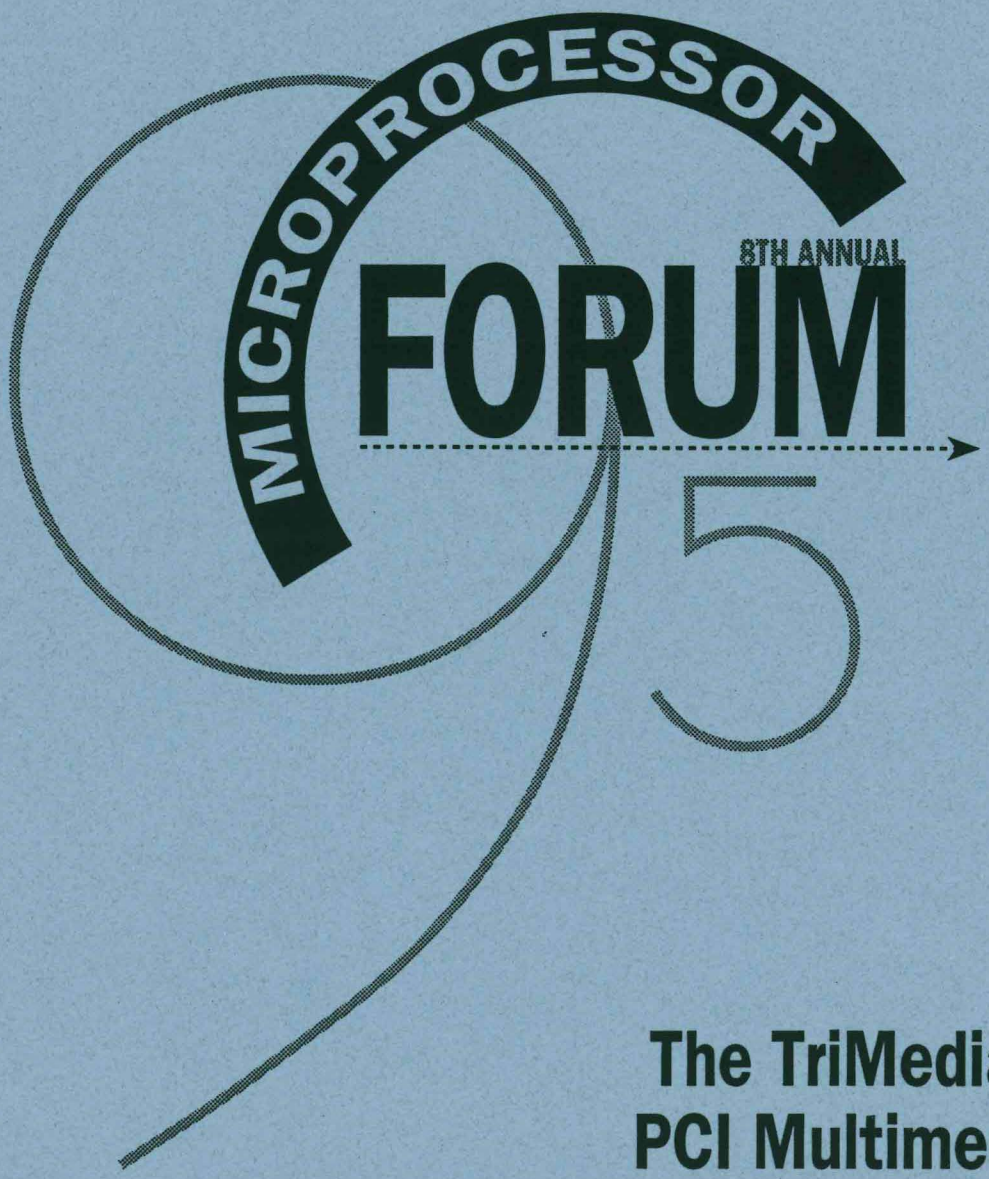
Nick Tredennick is President of Tredennick, Inc. He created the logic design for the 68000 at Motorola and for the Micro/370 microprocessor at IBM.

Marc Tremblay, as a computer architect involved in the research and development of high-performance processors at Sun Microsystems Marc's main contributions have focused on the microarchitecture definition and performance evaluation for the 64-bit UltraSPARC Processor.

George White, a cofounder and President of Corollary, George has pioneered a new category of computer, the PC-compatible multiprocessor system. He was instrumental in the development of the NuBus and was the chairman of the IEEE committee that standardized the NuBus.

Rich Witek, a principal designer of the Alpha architecture and co-architect of the first Alpha chip, Rich is currently the Chief Architect for the StrongARM microprocessor family at Digital.

David Witt is a Product Development Manager at AMD, where he is in charge of the Argon/K7 processor development. David was in charge of the K5 development effort at AMD, where he has been working for the past 11 years.



The TriMedia VLIW-Based PCI Multimedia Processor

Gerrit Slavenburg
Philips Semiconductors

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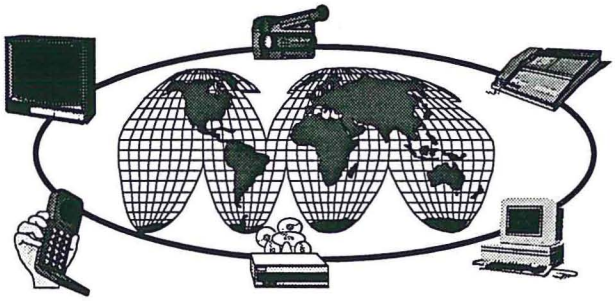
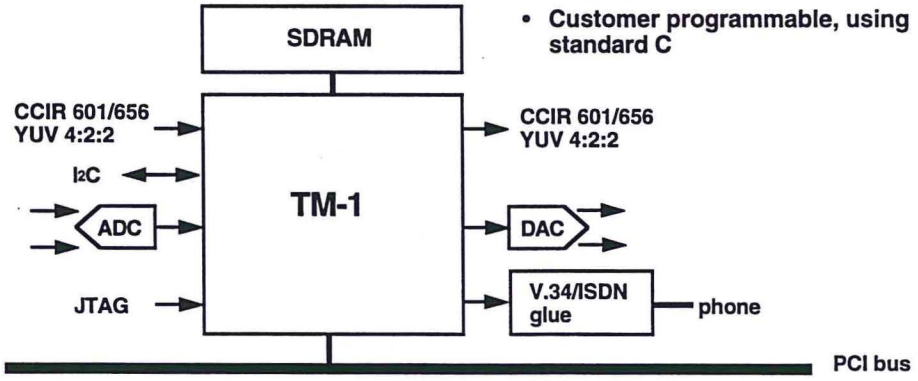
The Trimedia VLIW-based PCI Multimedia Processor System

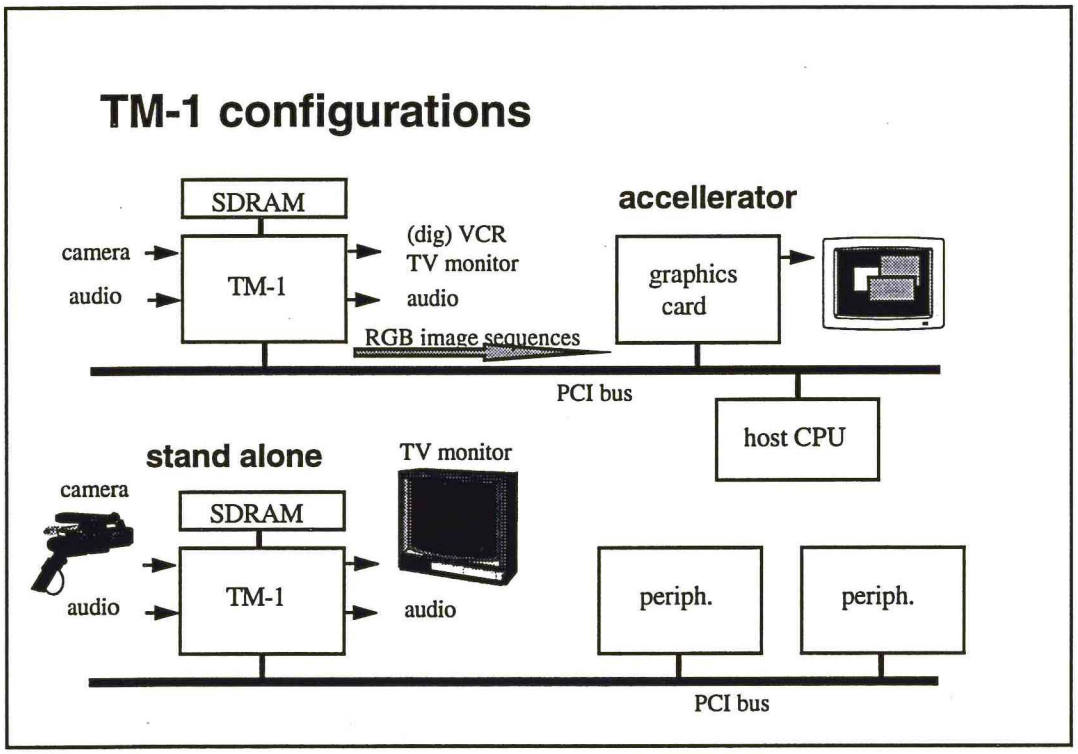
Gerrit Slavenburg - Philips Semiconductors

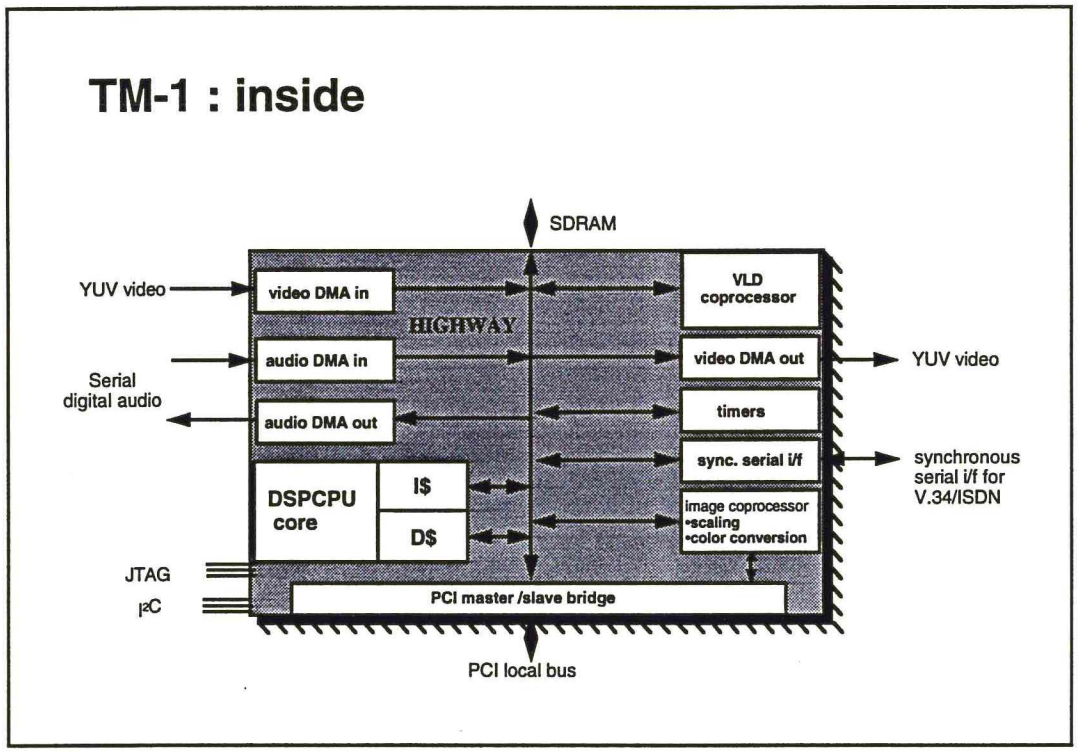


TM-1 : outside

- multi-standard, as in "any"
- Video and Audio (de)compression
- 3D graphics
- Customer programmable, using standard C




TM-1 configurations
SDRAM
camera
audio
TM-1
(dig) VCR
TV monitor
audio
RGB image sequences
accellerator
graphics card
PCI bus
host CPU
stand alone
TV monitor
camera
SDRAM
audio
TM-1
audio
periph.
periph.
PCI bus


TM-1 : inside
SDRAM
YUV video
video DMA in
HIGHWAY
VLD coprocessor
audio DMA in
video DMA out
YUV video
Serial digital audio
audio DMA out
timers
sync. serial i/f
synchronous serial i/f for V.34/ISDN
DSPCPU core
I$
D$
image coprocessor
•scaling
•color conversion
JTAG
I2C
PCI master /slave bridge
PCI local bus

TM-1 Functional

hardware

Video DMA in:
- CCIR601/656 YUV 4:2:2 input
- horizontal scaling by 1:1 or 2:1

Video DMA out:
- CCIR601/656 YUV 4:2:2 out
- horizontal scaling by 1:1 or 1:2
- graphics overlay (alpha blending)

Image co-processor
- memory-to-memory
- memory to PCI windows, with YUV to RGB
- V resizing, H resizing

VLD co-processor
- memory-to-memory de-tokenize
- MPEG-2, MPEG-1 slice/time

hardware

Audio DMA in/out:
- 8 or 16 bit
- mono or stereo
- programmable 0 - 80 kHz sampling

software

multi-tasking in C on DSPCPU:
- compression (any standard)
- decompression (any standard)
- 3D graphics
- system control
- PC API support

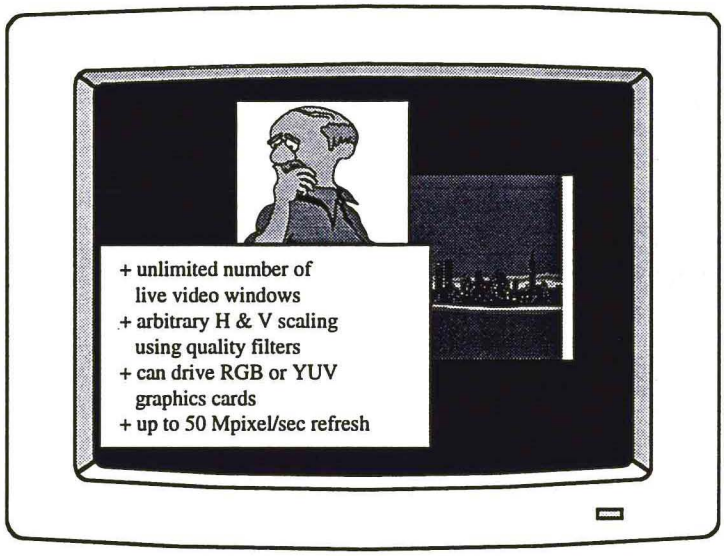
using powerful custom multimedia operations

TM-1 Highway Arbitration

- software assigns bandwidth to each master
- every master is guaranteed:
  - minimum bandwidth as assigned
  - associated max. latency
- all unused bandwidth is available:
  - to the DSPCPU/caches within 1 cycle
  - to any other master within a few cycles from request

this is an essential function for audio/video

Image Co-Processor capabilities

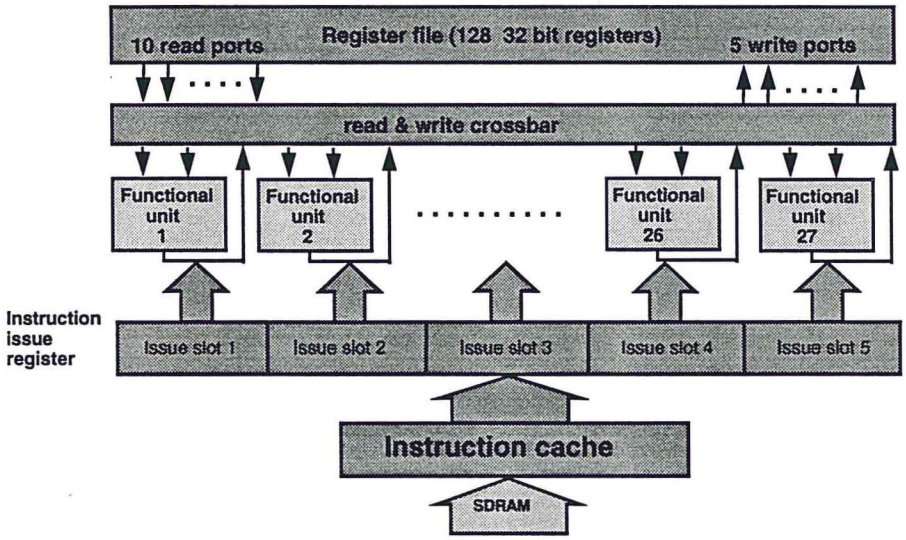


Audio/Video synchronization

Video In :	**camera/outside world is pixel clock master**
Video Out :	**programmable 10 MHz - 38 MHz, resolution 0.02 Hz (very low jitter synthesizer)**
Audio In, Audio Out:	**programmable 256 or 384f_s of 0 - 20 MHz, 0.02 Hz**

Synchronization is achieved by software PLL's that vary the sampling frequencies/phase by minute amounts. This powerful method is universal and avoids application specific external hardware.

TM-1 DSPCPU block diagram

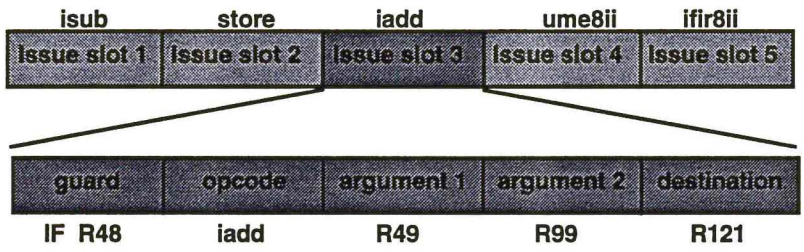


TM-1 DSPCPU functional units

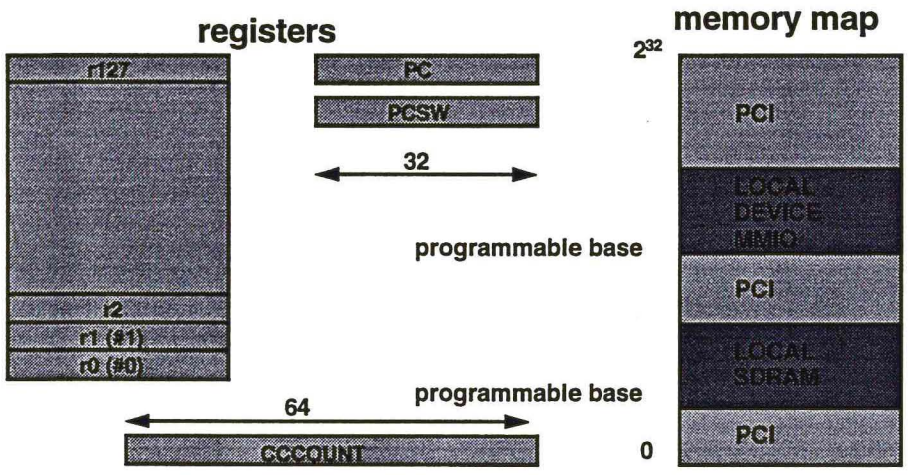
Functional Unit	Quantity	Latency	Recovery Time
constant	5	1	1
integer ALU	5	1	1
load/store	2	3	1
DSP ALU	2	2	1
DSP MUL	2	3	1
shifter	2	1	1
branch	3	3	1
int/float mul	2	3	1
float ALU	2	3	1
float compare	1	1	1
float sqrt/div	1	17	16

TM-1 instruction format

- 5 operations issued every clock cycle (10 nSec)
- Functional units are pipelined -- each can start one operation per cycle
- Issue slots are "guarded" for branch avoidance, delay slot utilization
- Interruptable opcodes facilitate lightweight context switching
- Instructions compressed in memory and Icache, decompressed on the fly



Trimedia programmer's model



Trimedia operation examples

Typical 32 bit RISC CPU operations

- Integer, unsigned, logical, floating point (32 bit IEEE compatible)
- Conditional branches
- Loads/stores with address modes

Typical 8, 16 and 32 bit DSP operations

- Saturation arithmetic (add, multiply-add, ...)

Branch-avoiding operations

- Min, max
- Select one of two operands depending on a third (implemented as branch-free three-operation sequence)

35 Multimedia-enhancing operations

- me8(abcd,efgh) |a-e| + |b-f| + |c-g| + |d-h| (motion estimation)
- fir16(ab,cd) Dual multiply-add -- ac+bd (FIR filters)
- quadavg(abcd,efgh) $\frac{a+e+1}{2}, \frac{b+f+1}{2}, \frac{c+g+1}{2}, \frac{d+h+1}{2}$ (subsampling filters)

TM-1 DSPCPU key features

- dual bytesex, determined by PCSW flag
- byte addressed memory, natural alignment required
- speculative loads & floating point supported
- precise IEEE exceptions, even when using speculation
- 5 ops/cycle, sustained
- conditional (guarded) execution of each operation
- compressed, byte aligned VLIW instructions
- vectored interrupts, zero overhead enter/return
  - compiler inserts interruptable points
  - CPU can handle simple interrupts at > 100 kHz with low loading
- instruction & data (address/value) breakpoint hardware
- level-1 boot from I2C resident serial xxROM

Example TM-1 (simplified to 3/cycle)

cycle			
101	#13→r11	ld32 r12(4)→r13	me8 r101,r100→r14
102	ileq r11,r15→r11	iaddi r12,220→r17	#LABEL→r18
103	r11:st32 r12(8) r14	ld32x r17,r19 →r16	cjmpt r11,r18
104	bitinv r11→r21	r11:st32 r12(12) r13	r11:me8 r99,r98→r42
105	r21:st32 r12(12) r17	r21:fir8 r101,r102→r23	r11:me8 r97,r96→r43
106	r21:#1234→r24	r21:fir8 r103,r16→r25	r11:me8 r95,r94→r44
107	fir8 r104,r105→r26	fir8 r106,r107→r27	iadd r42,r43→r45
107	me8 r93,r92→r45	me8 r91,r90→r46	#0xffff000→r18

TM-1 system key stats

- consumer electronics price level, ranging to sub $50
- Early Access Program:
  - software development tools (now)
  - samples Q2 '96
- application performance:
  - MPEG-2 main level, main profile, 15 Mbit/sec. Video+Audio+System decoding
  - H.320 codec Video+Audio
  - H.324 codec Video+Audio+software V.34 modem
  - any custom V/A algorithms with similar compute requirements
- typical 4 W (@ 100 MHz, 3.3 V)
- 0.5u CMOS, 4L metal with shrink to 0.35u to follow
- available in 240 pin EDQUAD or SuperBGA package

Software development

'human assisted microcode compilation'

- sophisticated compiler/debugger environment
- compile, run, recompile for automatic fine grain parallelization
- programmer feedback (where is time spent, where is parallelism limited)

TM-1 Innovations

- very high performance CPU on a chip at a consumer price point
  - enhanced VLIW architecture with conditional execution
  - VLIW instruction compression : sub RISC code size
  - multimedia operation set based on actual application ports
  - zero overhead interrupt handling
  - sophisticated compiler : profile driven program transformation and instruction scheduling
- complete audio/video system + CPU on single chip
  - software controlled Audio/Video synchronization
  - DMA mastering I/O units
  - DMA mastering co-processors (image & VLD co-processor)
- 100 MHz SDRAM interface, under worst-case conditions

Trimedia

A "Family" of software compatible media processors

- continuous renewal of CPU cores
- interfaces addressing different market segments (PC, settop, TV, ..)
- mainline & derivative product strategy
- a single architecture for all audio, video, graphics, communication, user-interface and system control

Superior flexibility and programmability

- "Any" compression standard
- All programming in Standard C
- Applications/libraries available for Audio, Video, Graphics
- SUN and PC hosted programming environment
- Automatic fine-grain parallelization
- Sophisticated source-level debugging of Device Under Test