



**System
Central
Interface
SCI**

SCI Specifications

3 independent parallel ports, each bit programmable input or latched output. Handshake signals for each port.

Serial port with RS-232, 20ma, 60ma current loops, speed selectable between 45 and 9600 baud.

High-speed biphase cassette interface with selectable speeds from 800 to 100,000 baud. Can also be used as a signal generator to test audio equipment.

Two on-board relays control two recorders. Three status lines for external recorder control.

Reset-jump: on reset, the CPU jumps to the SCI monitor.

2708 programmer.

256 bytes of RAM for stack and buffer space.

2k monitor in 2708's provides system control and I/O.

SCI requires the following S-100 bus signals:

+8 volts, +16 volts, -16 volts, circuit ground

$\overline{\text{PWR}}$, $\overline{\text{PDBIN}}$, $\overline{\text{PHOLD}}$, $\overline{\text{PRESET}}$, $\overline{\text{PSYNC}}$

SINP, SOUT

A0-A15, DIO-DI7, DOO-DO7

2 mhz clock

Power Requirements: (nominal)

+8 - 450 ma

+16- 85 ma

-16- 65 ma

Dimensions: 10.0 " wide x 5.1 " high (excluding edge connector)

SCI generates its own wait states, independent of the processor used, and can use 650ns 2708's.

SYSTEM CENTRAL INTERFACE

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SCI Assembly

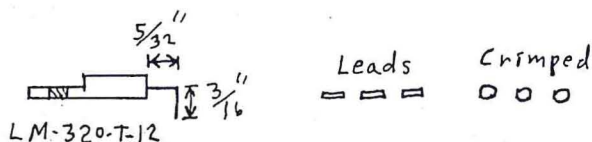
A note of caution: This is an expensive interface. To protect your investment, and ensure a long operating life, exercise care in the construction of this board. Take your time, be certain of parts placement, don't force I.C.'s into their sockets, solder thoroughly, but sparingly, as a little solder goes a long way. Handle the I.C.'s carefully, making sure that the pins are straight before inserting them into their sockets. I.C. pins can break, and lead receptacles damaged, by careless insertion. Take the time to inspect and test the finished board before applying power. This avoids the smoke test.

Personal care: wear eye protection when cutting leads and soldering. This prevents foreign material from entering your eyes.

Use a metallic holder for the soldering iron. This prevents heat-damaged tables, possible fires, and carpet burns when soldering irons get loose. The soldering iron need only be 25 watts with a 1/8 inch spade tip. A welder is not necessary. An iron with a three-wire cord is preferable for electrical safety. An Ungar #135 is an excellent iron for p.c. work, and costs about \$8.00. Rosin-core solder is supplied with the kit. If it's not enough, use 60/40 lead-tin rosin-core solder only. Acid-core solder will destroy the circuit and void the warranty.

All parts mount on the FRONT side, and solder on the BACK. Solder the parts after each step.

- Check the parts list and the parts layout. These should agree with the parts supplied. Contact us immediately if anything is missing, as shipping takes time.
 - Locate the 7-pole DIP switch. Mount it in the upper left corner of the board. Mount it with the numbers toward the top of the board.
 - Note the orientation of the I.C.'s: For vertical I.C.'s, pin 1 is to the upper left, and for horizontal I.C.'s, pin 1 is to the upper right.
 - Install the three standard profile 24-pin sockets in pads 17, 18, and 19. These are the sockets for the 2708's.
- Note that IC pad 6 is the address jumper pad and does not have a socket.
- Install the remaining sockets.
 - Install the four regulators and the two heat sinks. Line up the heat sinks over the areas marked on the p.c. board. Bend the leads of the regulators at right angles as shown on the parts list. The holes for the LM-320-T-12 were small on early production boards, and the leads of the regulator should be bent and cut approximately as shown, then crimp the leads slightly with pliers so they will fit the p.c. holes. Use 4-40 nuts and bolts to secure the regulators.



Next, install the capacitors. Observe the polarity of the 16 tantalum capacitors: the + lead must line up with the + shown in the layout and marked on the p.c. board.

The - lead for the tantalum capacitor on the right-hand side of the board must be bent inward, to avoid hitting the guide rails of the card rack.

Install the diodes, being careful to align the cathode bands with the markings on the p.c. board and shown in the layout drawing.

All resistors mount vertically:



Install the 1/2 watt resistors. These are about 50% larger than the 1/4 watt resistors. All are near IC-45. Note: There is an extra 51 ohm 1/2 watt, used in the 60 ma serial.

Install the remaining resistors.

There are two types of small-signal transistors used: 2N3904 and 2N3906. Be sure to place them at the correct locations, and oriented as shown in the layout. Spread the leads slightly to fit the hole patterns.

The MJE-180 transistor in the upper right-hand corner of the board, has leads that must be crimped slightly to fit the mounting holes. Trim the leads, then crimp with pliers to fit.

Insert the LED's, noting that the flat edge is the cathode. Check the parts list for details.

Jumper Options

Strap the address jumpers for the board address you specified when ordering. If you didn't specify, D000 hex is the standard address in the firmware supplied by DAJEN.

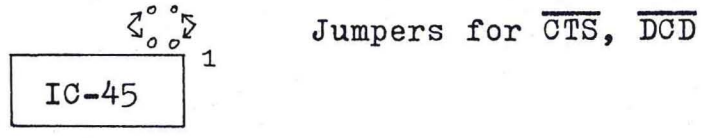
A15 14 13 A12
 ○ ○ ○
 |
 ○
 ○ ○ ○ Address pad, D000 shown

ADDRESS	Jumper(s)	ADDRESS	Jumper(s)
8000 hex	A-12,13,14	C000 hex	A-12,13
9000	A-13,14	D000	A-13
A000	A-12,14	E000	A-12
B000	A-14	F000	None

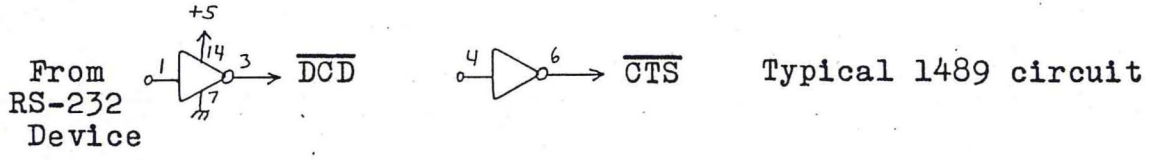
Lower addresses (6000,7000) could be used, but are not recommended, as system RAM usually occupies the first 32 K of memory space, if not more.

Note: I/O addresses use 16 consecutive ports, with the same byte as the board address. For a board address of D000, the I/O addresses are: D0, D1, D2, ... DE, DF. For a board address of A000, the I/O addresses are: A0, A1, A2, ... AE, AF.

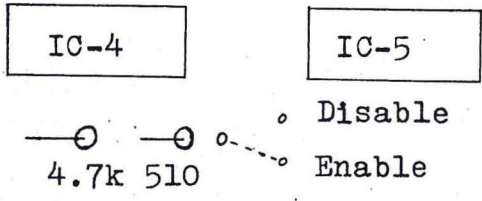
The two jumpers in the upper right-hand corner next to pins 1 and 2 of IC pad 45, the serial port, should be installed if there are no immediate plans for connection to a Modem.



When used, \overline{CTS} (Clear To Send) and \overline{DCD} (Data Carrier Detect) must be converted to RS-232 levels (they are TTL compatible) using a 1489 or equivalent RS-232 line receiver.



Reset-Jump Jumper



IC-4 and 5 are located in the lower left portion of the SCI board.

The reset-jump circuit takes control of the S-100 bus when the reset line (pin 75 on the bus) is active (low). No other jump circuits should be active, as they will probably conflict and the system will hang-up.

This circuit is enabled by placing a jumper from the reset-jump pad to the enable pad. It is disabled by placing a jumper to the disable pad.

The address to which the processor jumps is determined by the first three bytes of the 2708 in IC position 17 (P0). With the SCI monitor, the jump address is directed to the initialization routine of the monitor, and is typically:

- H000 C3 Jump instruction for CPU
- H001 1E Low-order jump address
- H002 H0 High-order jump address

The manner in which the SCI jump circuit is set up requires that the CPU jump to a location within the first 1k of the SCI board address to reset the jump circuit. This design eliminates false reset of the reset-jump circuit when the SCI is addressed at F000. Thus, if other than the SCI monitor is used, and a jump outside the first 1k of the SCI memory block is desired, a second jump instruction must be used, and could be placed immediately following the first jump instruction.

Example: SCI addressed for D000-DFFF, desired jump address is to E000:

- D000 C3 03 D0 first jump instruction
- D003 C3 00 E0 second jump instruction

If a Modem is to be used, the $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ (Clear to Send, Data Carrier Detect) from the 1489 will connect to pins 1 and 2 on the interface plug. If a Modem with CTS and DCD is to be used interchangeably with a device not sending those signals, wire one I/O plug for the Modem, and another for the other device, connecting pins 1 and 2 to pin 6 on the plug for the other device.

RS-232 or Current Loop

Both an RS-232 device and a current-loop device can be connected to the SOI at the same time. Each keyboard can independently provide input, but each printer will print the same output. The devices must operate at the same baud rate. If only one device is used, the other input must be jumpered on the 14 pin connection plug.

$\overline{\text{Gnd}}$	$\overline{\text{Gnd}}$	$\overline{\text{RTS}}$	$\overline{\text{DCD}}$	$\overline{\text{CTS}}$
⑦	⑥	⑤	④	③

Pad 45

⑧	⑨	⑩	⑪	⑫	⑬	⑭
Curr IN	-12	RS 232 IN	RS 232 OUT	60 MA	20 MA	OUT

Serial Port Connections

$\overline{\text{RTS}}$ is a TTL level output

If a current loop device is used, connect the printer + lead to pin 13 for a 20 ma loop, or to pin 12 for a 60 ma loop, and the other lead to pin 6. The keyboard contacts connect to pins 8 (+) and 7. The RS-232 input must be jumpered from pin 10 to pin 9.

If an RS-232 device is used, connect the printer lead to pin 11, and the keyboard to pin 10, with common signal lead to pin 7. De-activate the current loop keyboard contact with a jumper from pin 8 to pin 7.

Remember, when only one keyboard device is used on the serial port, the other must be de-activated with an appropriate jumper.

It is recommended that coaxial cable such as RG-174 be used for connection to the serial devices, as the shielding prevents extraneous noise pick-up.

EIA RS-232 Connections

The following page lists the pin numbers used on the EIA RS-232 standard connections. RS-232 is normally used on Modems, and data terminals, for high-speed serial data transfers. The standard connector used is a 25 pin EIA designated type. The use of cables under 50 feet is recommended. If longer cables are used, the total capacitance of the cable and terminator must not exceed 2500 picofarads (micro-micro-farad). Normal cable capacitance is about 30 picofarads per foot.

EIA Connections

The following are the standard connections used with a 25-pin EIA port connector (RS-232).

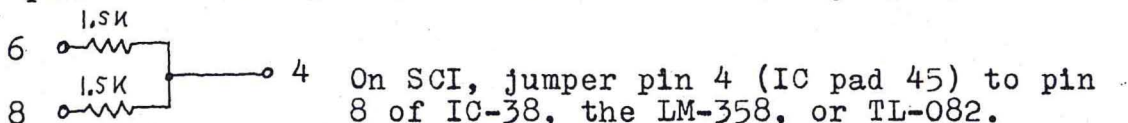
EIA pin	Signal	SCI pin on pad 45	Description
1	Frame ground	--	Connect to chassis ground (Tie to bolt of EIA socket).
2	Terminal Out	10	Data from terminal keyboard.
3	Terminal In	11	Data to terminal printer.
4	Request to Send	--	Request by terminal to send.
5	Clear to Send	--	Send data.
6	Data Set Ready	--	To terminal. If needed, tie to +12 volts through a 1.5k resistor.
7	Signal ground	7	ground, common signal.
8	Received line signal detector		If needed, tie to +12 volts via 1.5k resistor.
9-16	Not used		
17	TTY output	8	Keyboard of TTY serial loop. (Tie to pin 6 if not used.)
18-22	No connection		
24	TTY output	6	ground for TTY loop.
23	TTY input	13	20ma current loop to TTY printer.
25	TTY input	6	ground reference for loop.

If the RS-232 input is not used (SCI pin 10), tie to -12 volts on pin 9.

If the serial input to the SCI is not used, tie pin 8 to pin 6 or 7.

Resistor connections to +12 volts if Data Set Ready or Received Line Signal Detector are needed by terminal:

EIA pin SCI pin (connect to +12 with a jumper).



Keyboard and Parallel Port Wiring

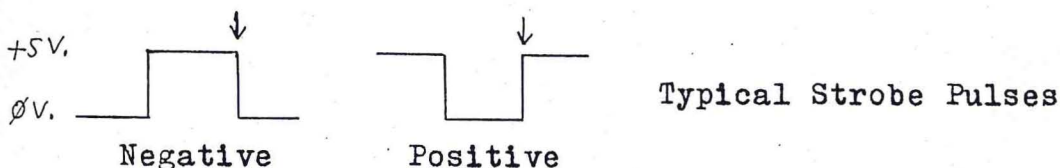
All three parallel ports are wired identically, except that IC pad 44, the "Keyboard" port, has -12 volts supplied on pin 1, for keyboards that require a negative bias. Otherwise the ports are identical, and the software determines which ports are input or output. The current available on the +5 volt supply is mainly a function of the regulator temperature. If forced air cooling is used, the regulator will remain cool, and a total of 500 ma is available. If convection cooling is used, it is recommended that total current be held to 100 ma.

If a keyboard is used that has only seven data lines, don't use D7, leave it open.

Gnd 06 07 50 SI -12 (44)
7 6 5 4 3 2 1 Parallel Ports, 42, 43, 44

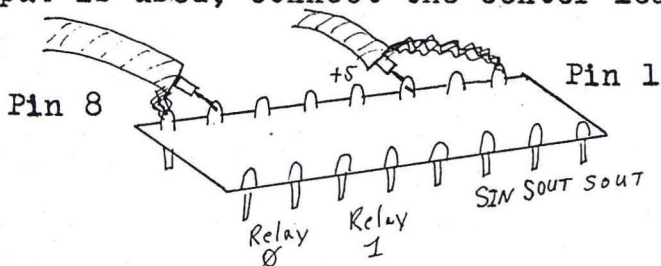
8 9 10 11 12 13 14 D0-D7= Data lines
05 04 03 02 01 00 +5 SI= Strobe in S0= Strobe out

Strobe polarity is determined by software, and is normally negative. The 2k monitor supplied looks at DIP switch 7 to determine the strobe of the Keyboard port. If switch 7 is on, the monitor expects a negative strobe. If the switch is off or "Open", the monitor expects a positive strobe.



Cassette Cable Connections

□ Cut the audio cable into two equal lengths. These ends then solder to appropriate pins of a 16 pin DIP plug for record and playback connections. If a standard cassette recorder is being used, connect the lead from the speaker jack to pins 7 and 8 on the plug (pin 8, is the shield connection). If a high-impedance output from a deck is used, connect the center lead to pin 6. For a microphone input, connect to pins 1 and 2 (shield to pin 1). If an AUX input is used, connect the center lead to pin 3.



Cassette Control

□ If you plan to use two recorders, connect the Read recorder remote control line to pins 9 and 10 on the plug. Connect the Write recorder remote line to pins 11 and 12. When reading a cassette tape, the Read recorder will be activated, and when writing a tape, the Write recorder will be active.

If you will be using one recorder for both reading and writing, wire pin 9 to pin 11, and pin 10 to pin 12. Then connect the recorder remote line to pins 11 and 12, and it will be active when reading and writing.

When using more sophisticated cassette control, pins 14, 15, and 16, provide additional control and status lines. Normally, with the monitor supplied, pin 14 is set for status input, for turns counters, or other status info, and pins 15 & 16 output for additional control, connecting to a transistor relay driver or equivalent. These lines can be set up for other configurations, such as all outputs or two outputs and one input, by changing the initialization routine as desired. Complete control of an automatic deck, such as a Phi-Deck, can be easily implemented, to control forward, reverse, read, and write. One status output controls Fast-Forward, or Rewind, one status output controls Read-Write, one on-board relay turns power on and off to the drive motors, and the other

relay controls the Playback-Record solenoid. The status input counts the turns of the tape reel to locate files. Further information is forth-coming.

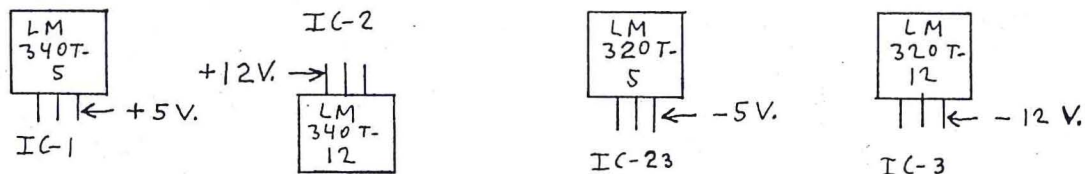
Check-out

Before inserting the I.C.'s or applying power, inspect the finished board. Are all connections soldered, are there any solder bridges? Are any leads touching other leads? Solder bridges are not likely to occur with the solder-masked p.c. board. If they do, draw the solder away with the tip of the iron. Compare the orientation of capacitors, diodes, transistors, and sockets, with the layout drawing. Correct any discrepancies. Excess solder flux can be removed with Miller-Stephenson Heavy Duty Flux Remover. Alternatively, isopropyl alcohol and a clean rag will remove flux. Soak a corner of the rag in the alcohol and wipe the flux off, in a direction away from the edge connector, as flux remaining on the connector fingers could cause intermittent connection.

After inspecting and cleaning the board, use a VOM (Volt Ohm Meter) set to resistance scale X 100, to check the resistance of all fingers of the edge connector to ground, pins 50 and 100, and to +5 volts on board (pin 16 of IC 5 or IC 7). This eliminates the destruction of bus drivers in the computer if a problem exists. Most fingers will have infinite resistance.. Zero, or low resistance indicates a problem. Only pins 2 (+16), 52 (-16), and Reset pin 75 will have any resistance indication. Even here, the resistance should be greater than 200 ohms. Of course, pins 1 and 51 the +8 supply will show resistance to ground and to the on-board +5 supply. If there is an abnormal indication, or short, follow the p.c. trace from that finger and look for a solder bridge or an etch problem. Repair the problem.

Caution: never insert or remove a board in the system bus with the power on. Always turn the power off, and wait half a minute for the power supply capacitors to discharge.

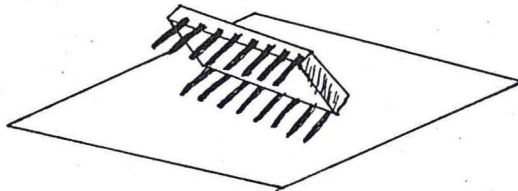
After a satisfactory resistance check, plug the SCI into the system bus and apply power. Measure the voltages out of the four regulators. The values should be within 10 % of the nominal value shown:



If any voltage measurement is not within range, there may be a problem with the regulator, associated bypass capacitor, a short in the p.c. power trace, or inadequate supply voltage. If the regulator is getting very hot, there is probably a short. Check that the associated tantalum bypass capacitors are correctly installed, the + lead is aligned with the + mark on the P.C. board. Or there is a short somewhere from the output trace to ground. If the

regulator is cool to the touch, check the supply voltage to the regulator. If the supply is ok (+8,+16, or -16), the regulator is faulty. Contact DAJEN for a replacement.

With the regulators working correctly, turn off the power and remove the SCI. The next step is to insert the I.C.'s. Be careful when handling the I.C.'s. Avoid conditions that can generate static electricity: don't walk across carpets and then touch the I.C.'s, ground yourself to a metal object such as a desk or chair. Don't slide across plastic covered chairs. Leave the I.C.'s in the pink anti-static plastic bags until actually installing them. Place the p.c. board in front of you, the bag of I.C.'s to one side, and the layout picture to the other side. Remove one I.C. from the bag at a time and install it. Prior to inserting each I.C., straighten any bent pins, and squeeze them in slightly so they line up with the lead receptacles of the socket. One way to do this is to hold the I.C. between thumb and fore-finger, and with the leads resting on a table top, press down lightly. Forming the leads prevents damage to the I.C. pins and to the socket.



To insert the I.C., place the pins directly over the socket receptacles and with an even pressure press the IC into the socket until it seats firmly. The 24 pin I.C.'s will require a great deal of force to seat into the socket.

Note: the 2708 marked P0 plugs into the left-most standard profile socket. P1 plugs into the middle socket, and P2, when supplied, plugs into the right-hand socket(IC-19).

After all the I.C.'s have been installed, make a visual check of their orientation and location. For all vertical I.C.'s, the orientation mark faces toward the top of the board, and for all horizontal I.C.'s the orientation mark faces to the right of the board. Make sure all I.C.'s are in their correct position.

Power-on Test

Plug the completed board into the system bus. Connect the various peripherals (Tape recorder, keyboard, teletype, etc). If you are using a video monitor as the principal console output device, connect to the video interface board in the bus, and turn on the monitor. If you specified a teletype or serial device as the main console output, turn it to "Line". Apply power to the computer. If you have a front panel, hit the "Reset" switch. The front panel lights should indicate address 0000, and the data bus should show C3 (bits 7,6,1,0 on). Hit "Run", the data lights should all glow, and the high-order address lights (A-15,14,13,12) should indicate the address of the SCI board (For example, for address D000, A-15,14, and 12 on, A-13 off). If you don't have a

front panel, hit "Reset". When running, the SCI monitor program clears the video monitor screen, outputs a prompt character (>) to the main console output device, and waits for a command from the main console input device. Characters typed on the input device are echoed to the output device. This action confirms that 90 % of the SCI is functional, so proceed to the Cassette Checkout.

If SCI fails to perform up to here, there is a problem. A few tests can be performed with a voltmeter. To know where to begin, analyze what is happening: when "Reset" is pressed the reset-jump circuit is activated. SCI grabs the bus and outputs a jump instruction to the processor (the jump instruction is the first three bytes in Prom 0). The CPU reads the jump data and jumps to the beginning of the SCI monitor. At this time the reset-jump circuit is reset and the SCI monitor initializes the LSI circuits on board, clears the video screen, outputs the prompt character, and waits for input. Troubleshooting determines where the chain of events is interrupted. This then identifies the area of the faulty component. Start with the reset-jump circuit. With a VOM measure the voltage to circuit ground (pin 7, IC-4) of pin 6 on IC-4, while holding the reset button pressed. This voltage should be less than 0.3 volt. Still holding reset, check the voltage at pin 6 of IC-13, which should be low (0.3), check pin 6 of IC-27, also low, and finally, check the voltage on the DI pins of the edge connector. DI-7,6,1,0, should be high (3 volts or so), and DI-5,4,3,2 should be low. Use the schematic to identify the pin numbers of the DI lines. A problem at this point isolates the reset-jump circuit (IC-4,13,27) or the bus driver IC-10. Tests beyond this point require a front panel and an oscilloscope to trace signals. Contact us immediately.

Programmer

The on-board programmer power supply is active when the switch marked "P" is off or open. Place this switch off. Measure the output voltage at E of the 2N3906 transistor next to IC-29. It should be about 27 volts or slightly higher. Place the switch back in the on position.

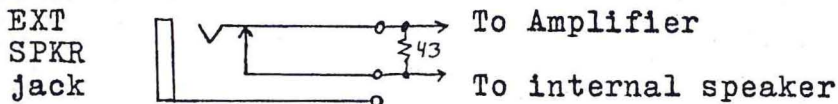
When programming 2708's, switch "P" must be in the off position, otherwise leave it in the on position.

Cassette Check-out

With SCI functioning and responding to commands, insert the supplied tape into the cassette recorder. Turn the recorder volume control to about 1/3 of full range, and the tone control to mid-range. Hit the reset button and type in the command: SR 03E8(CR) (CR=Carriage Return). This sets the cassette read speed to 1500 baud. Place the recorder in the playback mode and type RC(CR) on the keyboard. The recorder should start playing and when the leader tone on the tape is reached, the "Level" light on SCI should glow. Adjust the level of the recorder to illuminate the "Level" light. When the sync code is received, the "Sync"

light will glow. If it doesn't, change switch "R" to the opposite of its present position and repeat the entire procedure from the beginning.

For recorders that can't monitor the tape with a plug in the external speaker jack, add a 43 ohm resistor across the amp and speaker leads as shown:



With the Read circuit working, fast forward the tape to a blank area. Record the digital counter reading. Hit the reset button and use the Z command as follows: Z 0 800 E6(CR). This writes sync bytes into the first 2k of memory. Place the recorder in the record mode and type in this command: WC 0 800(CR). The recorder should start, and then stop after about 10 seconds. Rewind the tape to the beginning of this section, place the recorder in the playback mode, and read in the data. The sync light should glow. If it doesn't glow with sync bytes coming from the recorder, try reversing the "R" switch, hitting reset, and read in the sync bytes again. If they read in this time, return the "R" switch to its original position and flip the "X" switch to the opposite of its present position. This reverses the phase of the data recorded on the tape so it will read in.

Try recording some random memory blocks to check for errors on playback. If there are errors, try adjusting the tone control on the recorder to eliminate them. On some recorders there is an optimum setting of tone for best results.

Tape

We recommend Scotch "Highlander" or AVC series tape, which is low noise, high density, and costs around one to two dollars per 60 minute cassette. With this tape, we estimate an error rate of about one in ten million. We have never had a non-recoverable error (re-reading fails to bring correct data).

Recorders

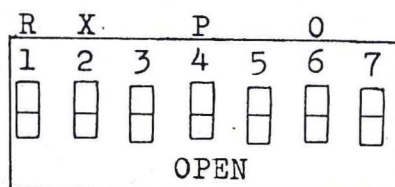
We believe you get what you pay for. A medium-priced recorder will provide better reliability, capability, and much longer life. For a moderately priced recorder, we recommend the Panasonic RQ-430S, at about \$50-\$60. For best price-performance, we have found the Superscope C-104 at \$80-\$100 unbeatable. This recorder can routinely record reliably at 5000 baud (624 bytes per second). We have one that's seen continuous service for a year and a half and still provides reliable, fast data recording.

Characteristics to look for in a recorder: a digital tape counter to keep track of program locations, automatic level to eliminate guess-work about recording, freedom from line-noise pick-up. This last requirement can only be deter-

mined by actual use with your system. When you buy a recorder, buy it on condition that you can return it in exchange for one that works with your computer system. Most dealers are willing to comply with your desires. If yours won't, find one who deserves your business.

Maintenance is essential for reliable performance. Keep the tape heads and capstan pressure roller clean. A Q-tip soaked in isopropyl alcohol is a good tool to get to those hard-to-reach places in the recorder. The dirt you see on the cotton swab can cause drop-outs and lost data. Keeping the capstan roller clean will help keep wow and flutter down. Although the SCI cassette interface can tolerate a 33% change in speed, a dirty pressure roller can cause that amount of speed change and consequent loss of data. We routinely record 24k data blocks, and following the above precautions, we almost never have errors.

DIP Switch Functions



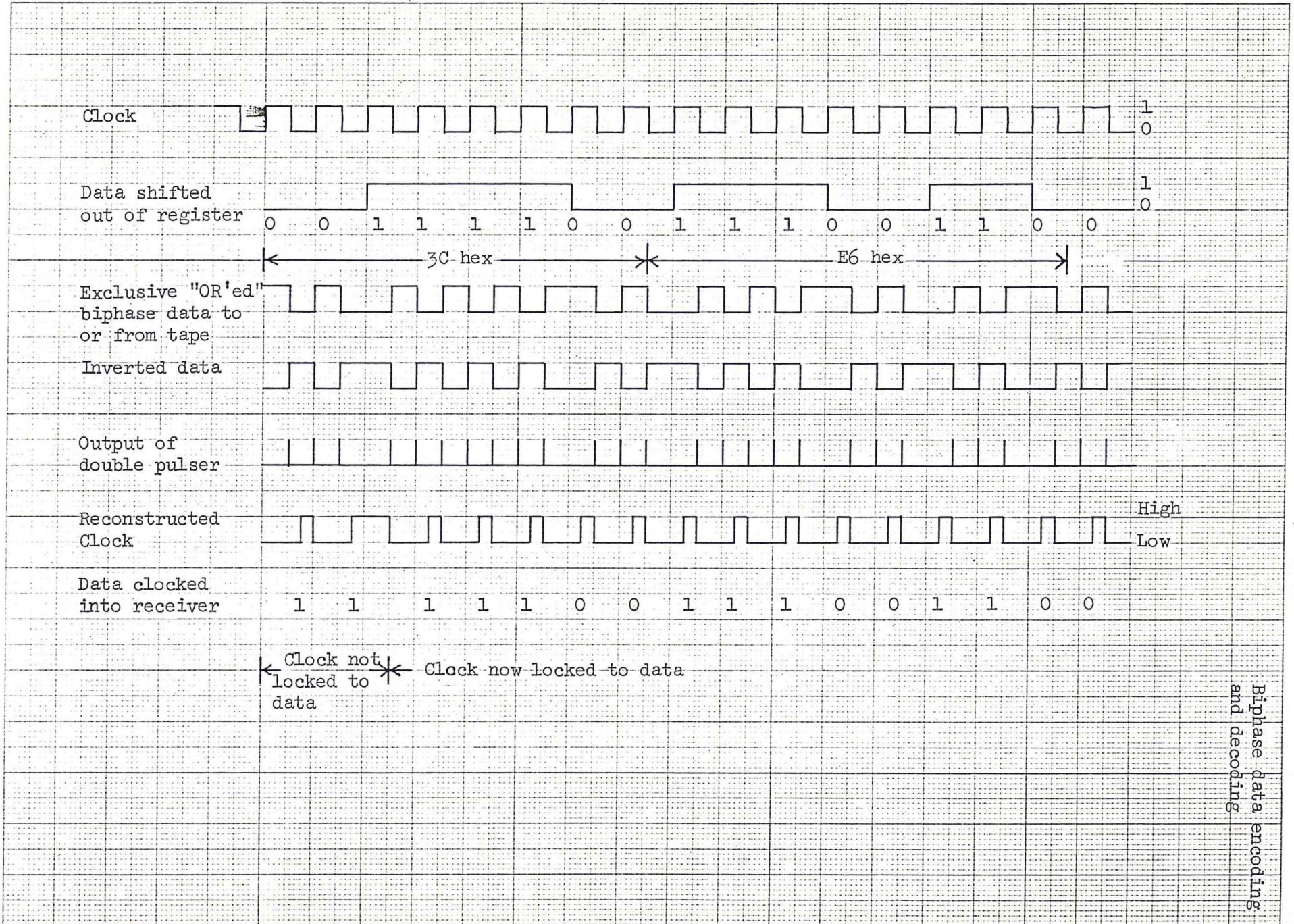
DIP Switch in IC pad 39

Switches 1 and 2 control the data inversion in the biphase cassette interface. Switch 1, "R", inverts the received data from the tape recorder. Switch 2, "X", inverts the data transmitted to the recorder. These switches compensate for different data inversions in different recorders.

Switches 3 and 5 are not used, and are available to the user if so desired.

Switch 4, "P", is the Programmer enable switch. When "OPEN" or "OFF", the on-board 2708 programmer is active. Normally, except when programming 2708's, this switch is "ON" to prevent inadvertent programming of the 2708 in IC pad 19 (3rd standard profile socket on the right.).

Switches 6 and 7 control options selected by the SCI monitor program. In current versions of the SCI software, switch 6, on initial start-up or reset, selects the console devices used for input and output. When switch 6 is "ON", a keyboard connected to IC pad 44 is assumed to be the console input device, and a video interface is assumed for output. When switch 6 is "OPEN" or "OFF", a serial device connected to IC pad 45 is assumed for both input and output.



Biphase data encoding
and decoding

Theory of Biphase Cassette Operation

Biphase recording is a means of recording digital data in a high-speed, densely-packed format, on cassette tape. Because each cycle of the recording process represents one data bit, there is no wasted space. A standard cassette recorder operating well within its capabilities can record data at 2500 baud error-free. This is 2500/8, or 312 bytes per second. In comparison, Kansas-City recording, operating with shifting frequencies, runs at 300 baud, or 37 bytes per second. Thus biphase is faster, and can as a consequence store more data on a given cassette. A 30 minute side of a standard Phillips cassette can hold 500 k-bytes of data.

To understand how biphase works, look at the figure on page 12 titled "Biphase Data Encoding and Decoding". Look at the top drawing. This is the basic cassette clock which sets the data transmission speed, or baud rate (one baud is one bit per second). This clock is generated by dividing the crystal-controlled system clock through a series of dividers. Contained within the cassette interface is a shift register which is loaded with one byte of data to be output. Each positive transition of the cassette clock shifts one bit out of the shift register. Data in a Tarbell-type system is shifted most significant bit first (bit 7 first, then bit 6, 5,1, 0). When all eight bits of the present byte are shifted out, the interface requests another byte.

The data shifted out of the register is then exclusive-OR'ed with the cassette clock. The logic states of a two-input exclusive-OR gate are as follows:

Inputs	A	\oplus	B	=	Y	Output
	0		0		0	
	0		1		1	
	1		0		1	
	1		1		0	

Note: when both inputs are the same, the output is low.

The third line of the figure on page 12 illustrates the data after it has been exclusive-OR'ed with the clock. This is then fed to the recorder input. Notice that when the data is unchanging (a string of zeroes or ones), the output to the recorder is the cassette clock frequency, and when the data changes from a one to a zero, or a zero to a one, an extra one-half clock cycle is added to the data output. These extra half-cycles are the basis of biphase. When they occur, the phase changes and the decoded data changes to the opposite state.

Now consider the decoding process. For the decoder presented, the input data must be inverted to provide the correct data output.

After being amplified and squared by a comparator, the data from the tape recorder is fed to a receiver shift register and a "double pulser". The "double pulser" puts out a pulse every time the incoming data changes state.

This output triggers a digital timer which is set equal to 75% of the time required for one complete cassette clock cycle. The output of this timer is the "reconstructed clock" shown in the figure. When triggered, this timer output goes low until it times out and returns to the high state. As it returns, the timer output pulse clocks the present data bit into the receiver shift register. When eight bits of data have entered the shift register, the cassette interface signals the computer that a data byte is available.

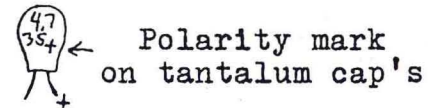
Notice that the first two data bits clocked into the receiver are 1's, where 0's were sent originally. The interface, started at random, has not locked to the data stream. However, after the first data transition from a 0 to a 1, the clock is now locked to the data stream, and the correct bits are entered into the receiver register. That first byte of data (3C hex) is called the clock synchronizing byte, because it synchronizes the reconstructed clock with the data stream.

The byte following the clock sync byte, is the data synchronizing byte (E6 hex). Up to the time it is received, the receiver shift register has been reset, not signalling the reception of bytes to the computer. When the receiver recognizes the data "sync" byte, it knows the next 8 bits will be a data byte, and readies the data flag to signal the computer that a data byte is available.

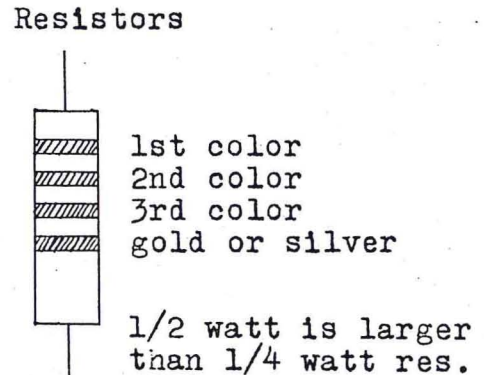
Analyze what would happen if the original, non-inverted data had been input to the receiver: all the data would be inverted. This is why the receiver has a data inversion switch. If the tape recorder doesn't invert the data it receives, then the interface must.

The reason there is a transmitted data inversion switch is to allow easy software interchange among biphas-system owners. Each interface is shipped with a pre-recorded cassette tape. The system owner adjusts his interface and recorder to be compatible with that tape and he is then able to easily exchange tapes with other owners.

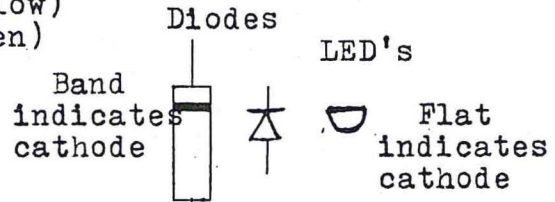
- Capacitors
 3 39 pf
 2 .001 uf
 4 .0047uf
 3 .01 uf
 4 .05 uf
 16 4.7uf 35 VDC



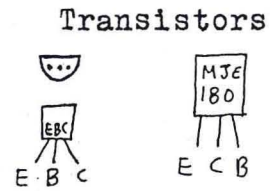
- Resistors 1/4 watt, unless noted
 4 4.7 ohm (Yellow-Violet-Gold)
 3 20 1/2 watt (Red-Black-Black)
 1 51 1/2 watt (Green-Brown-Black)
 2 43 (Yellow-Orange-Black)
 2 300 (Orange-Black-Brown)
 1 300 1/2 watt (Orange-Black-Brown)
 6 510 (Green-Brown-Brown)
 1 510 1/2 watt (Green-Brown-Brown)
 10 2k (Red-Black-Red)
 28 4.7k (Yellow-Violet-Red)
 5 20k (Red-Black-Orange)
 2 39k (Orange-White-Orange)
 3 100k (Brown-Black-Yellow)
 1 1Meg (Brown-Black-Green)



- 6 1N4148 diodes
 2 MV-5075 LED lights
 4 2N3904 transistor
 3 2N3906 transistor
 1 MJE 180 transistor
 1 7-pole DIP switch
 4 14 pin DIP plugs
 1 16 pin DIP plug

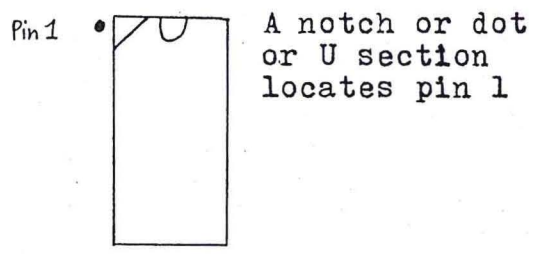


- Sockets
 3 8 pin
 15 14 pin
 10 16 pin
 3 20 pin
 3 24 pin low profile
 3 24 pin standard profile
 2 40 pin

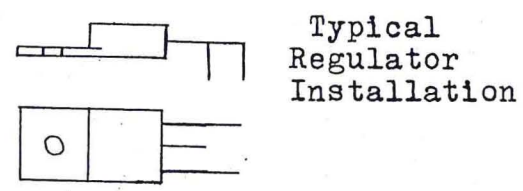


- 2 Heat Sinks

I.C.'s and sockets



- I.C.'s
- | | | | |
|---|---------|----|---------------------|
| 2 | 74LS00 | 1 | LM-320-T5 |
| 2 | 74LS04 | 1 | LM-320-T 12 |
| 2 | 74LS11 | 1 | LM-340-T 5 |
| 1 | 74LS32 | 1 | LM-340-T 12 |
| 2 | 74LS155 | 1 | TL-082 |
| 2 | 74LS221 | 1 | LM-380 |
| 2 | 74LS367 | 2 | LM-2903 |
| 1 | 74LS386 | | |
| 2 | 2112 | | |
| 2 | 2708 | 1 | Audio Cable |
| 2 | 6820 | 1 | Cassette tape |
| 1 | 6850 | | with Sync code |
| 1 | 6852 | 1 | P.C. Board |
| 1 | 8131 | 4 | 4-40 bolts and nuts |
| 3 | 81LS97 | 15 | feet of solder |
| 1 | 8253 | | |



Baud Rate Table

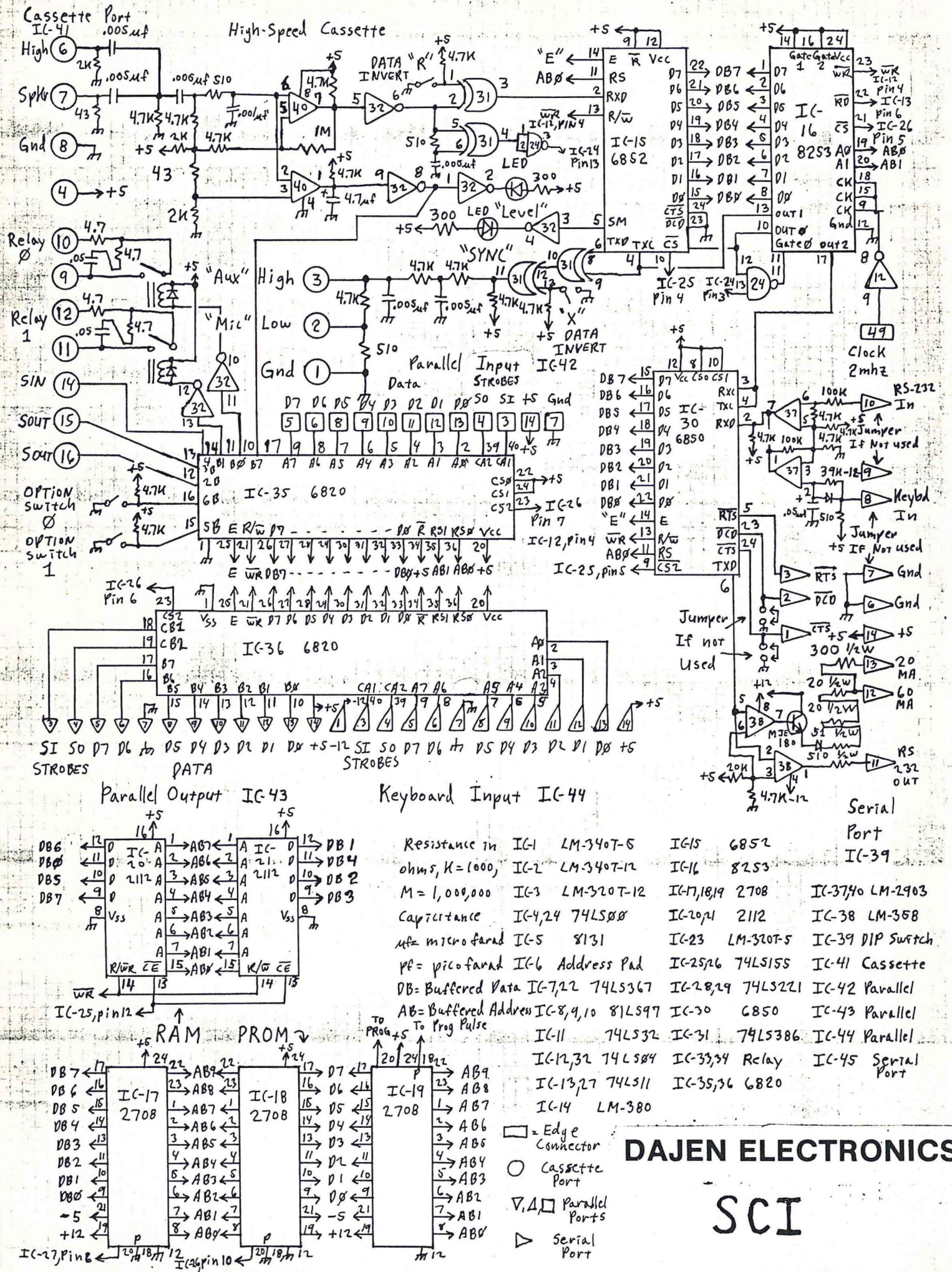
This table lists some of the baud rates which the cassette and serial ports can generate. Use the appropriate command (SR for Read, SS for serial, SW for write) to set the desired baud rate by inserting the hex number listed in the table, after the command letters. For example, to set the Read speed for 3600 baud, the command is: SR 01A0 CR (Carriage Return). Remember that when reset, or started cold, the various speeds are set by the pre-determined values in the initialization routine. For speeds not listed in the table, the appropriate hex number can be calculated as follows:

For Write: $N=2,000,000/\text{Baud Rate}$, N must be expressed in hex.
 Example: 2500 baud desired. $N=2,000,000/2500=800$ decimal
 A hex number is N3 N2 N1 N0, where N3 has a value of 4096, N2 256, N1 16, N0 ones. 800 has 0-4096, so N3=0; 800 has 3-256, so N2=3. This leaves $800-3 \times 256=32$. N1=2 ($2 \times 16=32$), and N0=0 because nothing remains. Thus the hex number is 0320. The command is: SW 0320CR (Carriage Return).

Read speed: $N=1,500,000/\text{Baud Rate}$

Serial speed: $N=125,000/\text{Baud Rate}$

Baud Rate	Cassette System		Serial Port	
	Write	Read	Serial	
45.45	ABE4	80EB	0ABE	60 WPM, Baudot
75	682A	4E20	0682	
75.75	6722	4D59	0672	110 WPM, Baudot
110	4705	3544	0470	
150	3415	2710	0341	
300	1A0A	1388	01A0	
600	0D05	09C4	00D0	
900	08AE	0682	008A	
1200	0682	04E2	0068	
1500	0535	03E8	0053	Tarbell cassette
1800	0457	0341	0045	
2200	038D	02A9	0038	
2400	0341	0271	0034	
2500	0320	0258	0032	DAJEN Cassette
3000	029A	01F4	0029	
3600	022B	01A0	0022	
4000	01F4	0177	001F	
4800	01A0	0138	001A	
5400	0172	0115	0017	
6000	014D	00FA	0014	
7200	0115	00D0	0011	
8000	00FA	00BB	000F	
9600	00D0	009C	000D	
10400	00C0	0090	000C	
12000	00A6	007D	000A	
14000	008E	006B	0008	
18000	006F	0053	0006	
19200	0068	004E	0006	
31000	0040	0030		
45000	002C	0021		
70000	001C	0015		
100000	0014	000F		

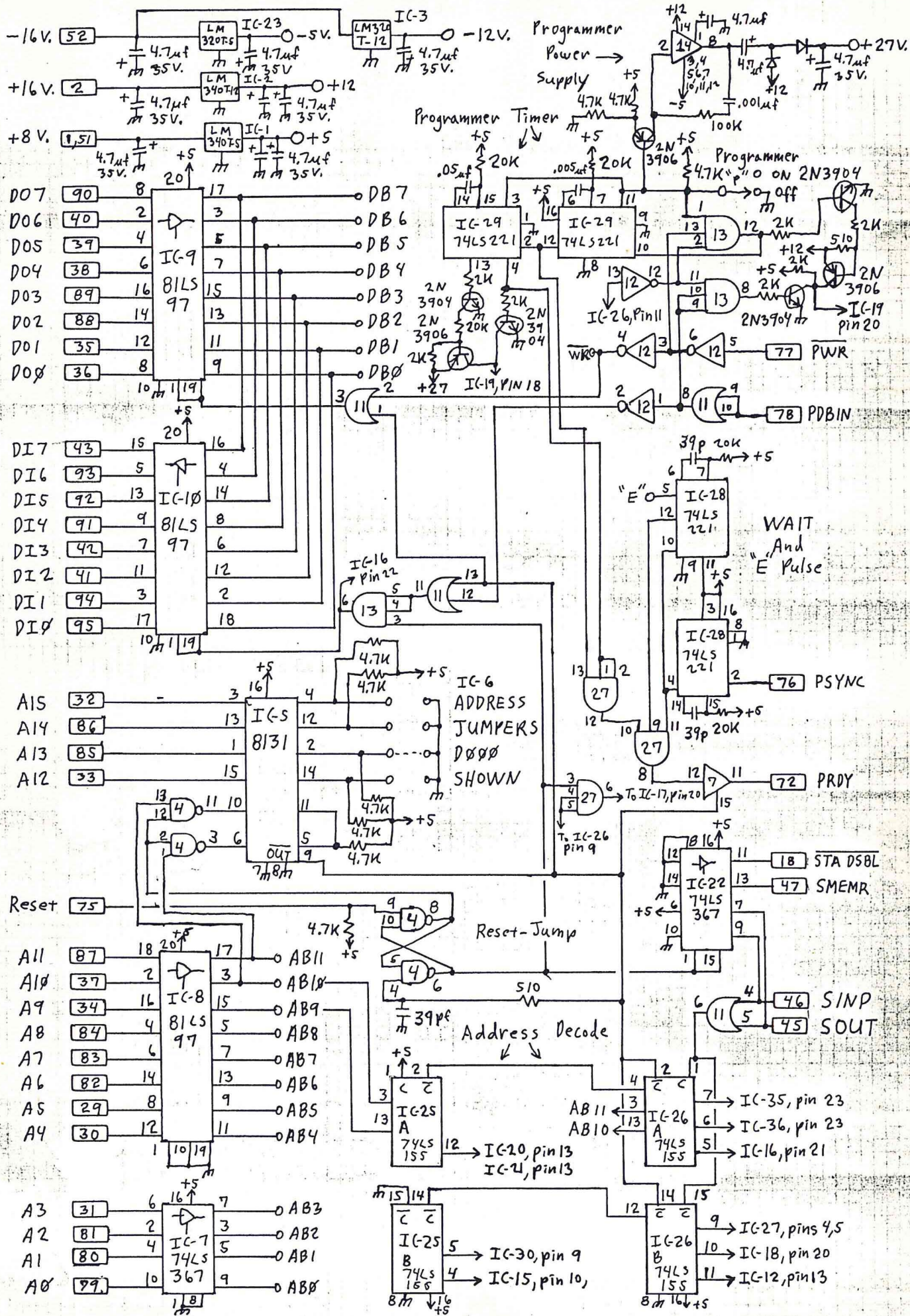


Resistance in IC-1	LM-340T-5	IC-15	6852	
ohms, K=1000,	IC-2	LM-340T-12	IC-16	8253
M=1,000,000	IC-3	LM-320T-12	IC-17,18,19	2708
Capacitance	IC-4,24	74LS00	IC-20,21	2112
µF= micro farad	IC-5	8131	IC-23	LM-320T-5
pF= pico farad	IC-6	Address Pad	IC-25,26	74LS155
DB= Buffered Data	IC-7,22	74LS367	IC-28,29	74LS221
AB= Buffered Address	IC-8,9,10	81LS97	IC-30	6850
	IC-11	74LS32	IC-31	74LS386
	IC-12,32	74LS04	IC-33,34	Relay
	IC-13,27	74LS11	IC-35,36	6820
	IC-14	LM-380		
				IC-37,40
				LM-2903
				IC-38
				LM-358
				IC-39
				DIP Switch
				IC-41
				Cassette
				IC-42
				Parallel
				IC-43
				Parallel
				IC-44
				Parallel
				IC-45
				Serial
				Port

DAJEN ELECTRONICS

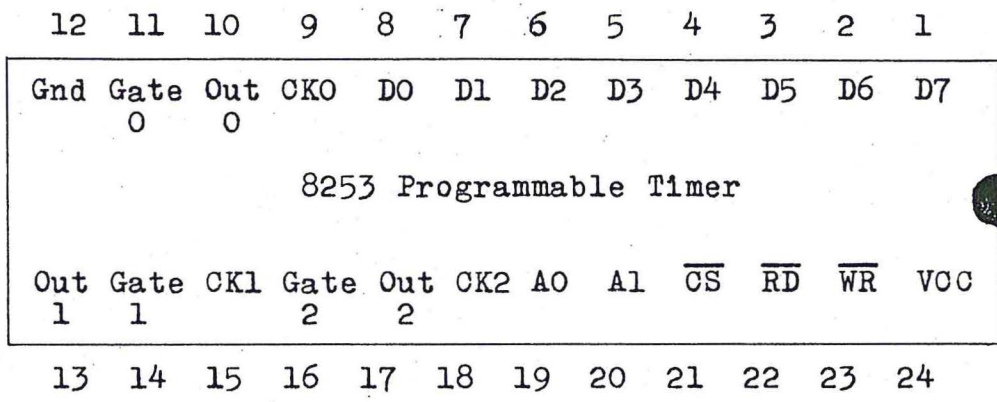
SCI

- = Edge Connector
- = Cassette Port
- ▽, △, □ = Parallel Ports
- ▷ = Serial Port



8253 Programmable Timer

Pin Configuration



DO-D7 Data lines \overline{CS} Chip Select
 AO,A1 Address lines \overline{RD} Read
 CKO,1,2 Clock inputs \overline{WR} Write

The 8253 consists of three independent 16-bit programmable timers, with a maximum count rate of 2 mhz. Each counter is programmed by writing a mode control word into the control word register. Depending on the mode, the count is loaded into the appropriate count register.

Control Word: D7 D6 D5 D4 D3 D2 D1 D0

Bit assigned: SC1 SC0 RL1 RLO M2 M1 M0 BCD

Where: SC=Select Counter to which control word applies

SC1	SC0	Counter	BCD=	0= Binary counter
0	0	0		1= 4-decade BCD counter
0	1	1		
1	0	2		
1	1	Illegal		

RL=Read/Load command

RL1	RLO	
0	0	Latch counter for read operation
0	1	Read/Load least significant byte only
1	0	Read/Load most significant byte only
1	1	Read/Load least sig.byte first, then most sig.byte.

Mode:	M2	M1	M0	Mode	Bus Address:	A1	A0	Device Selected
	0	0	0	0		0	0	Count Reg. 0
	0	0	1	1		0	1	Count Reg. 1
	X	1	0	2		1	0	Count Reg. 2
	X	1	1	3		1	1	Control Reg.
	1	0	0	4				
	1	0	1	5				

where X= don't care

8253 Programmable Timer

Mode Definitions

Mode 0: Out will be low at start of count, goes high and remains high at the end of the count. The Gate input inhibits counting when low, and enables counting when high. Out goes low when count register is re-loaded. Re-loading during counting: 1st load byte stops the count, 2nd load byte starts the new count.

Mode 1: Programmable One-shot. Out goes low following the rising edge of the Gate input. Out goes high at the end of the count. If a new count value is loaded during the counting, the current count will not be affected. The One-shot is retriggerable and Out will remain low for the full count after the last trigger.

Mode 2: Rate Generator. Divides by N (the count). Out is low for one period of the input clock after each N counts. Gate when low inhibits counting and holds Out high. When Gate goes high, the counter starts counting for the full count. Gate will synchronize the counter. If the count register is reloaded, only subsequent counts will be affected. When Mode 2 is set, Out remains high until the count is loaded.

Mode 3: Square wave generator. Similar to mode 2, but the output is a square wave. If the count is odd, Out is high for $(N+1)/2$ counts, and low for $(N-1)/2$. If the count register is reloaded, the new count is effective immediately after the next output transition. Gate controls counting.

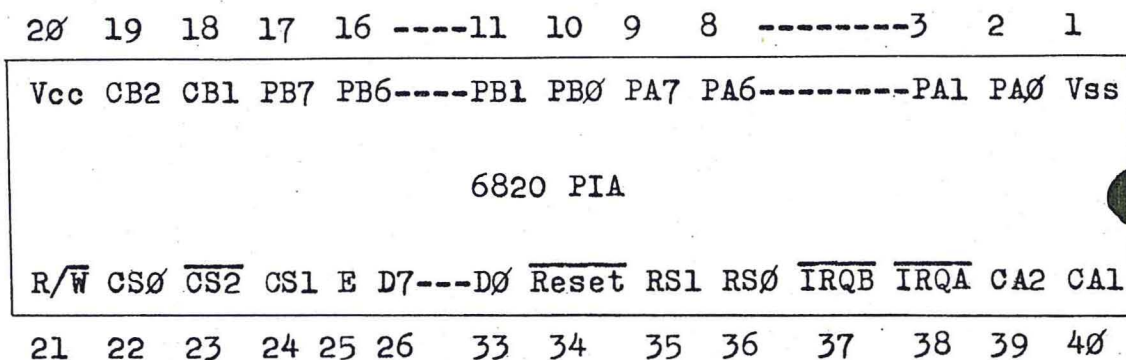
Mode 4: Software triggered strobe. Out is high after the mode is set. When the count is loaded, counting begins. Gate low inhibits counting. On reaching the count, Out goes low for one clock period. Reloading the count register while counting does not affect the present count. Reloading the count register restarts counting. Gate low inhibits counting.

Mode 5: Hardware triggered strobe. The counter starts counting after the rising edge of the Gate input, and Out goes low for one clock period when the count is reached. The counter is retriggerable.

The loading of the count register does not have to immediately follow the loading of the Mode register. The sequence of bytes specified in the mode word must be followed. All counters are down counters (count down from the count loaded).

To read the counter while counting, issue the RL $\emptyset \emptyset$ mode addressed to the correct counter in a mode word. Then reading the counter will produce a latched count. The mode of reading must then be issued, and either one or two reads made to input the least significant byte, then the most significant byte of the count. The entire reading procedure must be completed. If two bytes are to be read, then two bytes must be read, otherwise the WR command can't be sent to the counter.

6820 Peripheral Interface Adapter



CA1, CA2 Control lines for parallel port A
 CB1, CB2 Control lines for parallel port B
 CS0, CS1, CS2 Chip select inputs
 D0-D7 Data bus lines
 E Enable pulse, clocks valid data, conditions control lines.
 IRQA, IRQB Interrupt flag lines for use in interrupt-driven systems.
 PA0-PA7 Parallel Port A
 PB0-PB7 Parallel Port B
 R/W Read/Write control
 Reset Resets control registers and flags
 RS0, RS1 Address lines to select internal registers.

The 6820 Peripheral Interface Adapter consists of two independent parallel ports, each with its own handshake signals and interrupt request line, each bit programmable as input or latched output, and the necessary control registers to implement operation.

Register Addressing

RS1	RS0	Control Register bit	Location selected
0	0	CRA-2= 1	Data Register A
0	0	CRA-2= 0	Direction Register A
0	1		Control Register A
1	0	CRB-2= 1	Data Register B
1	0	CRB-2= 0	Direction Register B
1	1		Control Register B

The Data Direction registers determine the function of each bit in the associated parallel port. A 0 bit sets the corresponding peripheral line to an input mode. A 1 results in a latched output mode.

The Control Registers set the operation of the control lines, CA-1,2, CB-1,2, and enable the interrupts. Bits 0-5 of the control register may be written and read, while bits 6 and 7 are read-only.

Control Word Format for Control Registers

Bit 7	6	5	4	3	2	1	0
IRQ1	IRQ2	CA-2 Control	CB-2 Control		Data or Direction Register	CA-1 Control	CB-1 Control

6820 continued

Bit 2 of each control word allows access to either the data or direction register. See the register addressing on page E-3.

Bits 6 and 7 are read-only flags, and are set by signals on the Control lines. They are reset after read operations, by an E pulse, when the PIA is not selected.

Control lines CA-1,2, and CB-1,2, can be programmed for a variety of input-output functions. The following tables summarize the options available:

Interrupt inputs CA-1 and CB-1

Bit 1	Bit 0	Interrupt Input	Interrupt Flag Bit 7	Interrupt Request IRQA or IRQB
0	0	↓ Active	set high	Disabled- $\overline{\text{IRQ}}$ stays high
0	1	↓ Active	set high	Low when <u>flag</u> goes high
1	0	↑ Active	set high	Disabled- $\overline{\text{IRQ}}$ stays high
1	1	↑ Active	set high	Low when flag goes high

CA-2 and CB-2 as interrupt inputs

Bit5	Bit4	Bit3	Interrupt Input	Flag Bit 6	Interrupt request IRQA or IRQB
0	0	0	↓ Active	set high	Disabled- $\overline{\text{IRQ}}$ stays high
0	0	1	↓ Active	set high	Low when <u>flag</u> goes high
0	1	0	↑ Active	set high	Disabled- $\overline{\text{IRQ}}$ stays high
0	1	1	↑ Active	set high	Low when flag goes high

CB-2 configured as an output

Bit5	Bit4	Bit3	CB-2 Cleared	CB-2 Set
1	0	0	Low on positive transition of first E pulse after a write B operation.	High when flag bit 7 is set by active transition of CB-1.
1	0	1	Low on positive transition of first E pulse after a write B operation.	High on pos. edge of first E pulse after E pulse which occurred when not selected.
1	1	0	Low when CR bit 3 goes low after write into Control Register B.	Low as long as CR bit 3 is low. High when CR bit 3 is written high.
1	1	1	same	same

CA-2 configured as an output

1	0	0	Low on negative transition of E after a read operation of reg A.	High when flag goes high from active transition on CA-1
1	0	1	same	High after first E pulse when part not selected

6820 continued

Bit5	Bit4	Bit3	CA-2 Cleared	CA-2 Set
1	1	0	Low when CR bit 3 is set low. (A' Control Register)	High when CR bit 3 is set high (A' Control Register)
1	1	1	same	same

Parallel Port A has internal pull-up resistors that represent about one TTL load. When configured as outputs, the voltages at the port pins must be above 2.0 volts, or erroneous data will be seen when trying to read what was written.

Parallel Port B when configured as output, can drive up to 1 ma of current, and the output voltage does not have to be above 2.0 volts for the output to be read correctly after a write operation. Thus, Port B can drive the base of a transistor switch directly.

The E pulse conditions the interrupt control lines. At least one E pulse must occur from the inactive edge to the active edge of the input signal to condition the edge sense network. In other words, at least one E pulse (about 2 us apart) must occur between strobe inputs from an external device. Then the interrupt flag will be set on the next active transition of the strobe.

The interrupt flags are cleared after a read of the particular data register. They can not be set again until an E pulse occurs while the part is deselected.

Interrupts

When using interrupts, \overline{IRQA} or \overline{IRQB} is tied to the appropriate Vectored Interrupt pin on the S-100 bus, or they may be tied together to \overline{Int} (pin 73), as they are open-drain outputs. Then when an interrupt occurs, the appropriate flags can be checked in the Control Registers to determine the requesting device.

6850 Asynchronous Communications Interface
Adapter, or ACIA

Pin-outs

				Definition of pins	
1	Vss	$\overline{\text{CTS}}$	24	$\overline{\text{CS0}}, \text{CS1}, \overline{\text{CS2}}$ Chip-select inputs. When $\overline{\text{CS0}}$ and CS1 are high, and CS2 is low, the 6850 is selected by the bus.	
2	RxDData	$\overline{\text{DCD}}$	23		
3	RxCK	D0	22		
4	TxCK	D1	21		
5	RTS	D2	20		
6	TxDData	D3	19		
7	IRQ	6850 D4	18		$\overline{\text{CTS}}$ Clear to Send input from a modem, when low indicates that the data channel is ready for transmission. When a modem is not used, must be tied to ground.
8	$\overline{\text{CS0}}$	D5	17		
9	$\overline{\text{CS2}}$	D6	16		
10	CS1	D7	15		
11	RS	E	14	$\overline{\text{DCD}}$ Data Carrier Detect input from a modem, when low the data carrier is present. If high, the data carrier is lost, and the 6850 will generate an interrupt to reflect the DCD status in the status register. The receive interrupt must be enabled for this to happen. Must be tied to ground when not used.	
12	Vdd	R/ $\overline{\text{W}}$	13		

- D0-D7 Eight bidirectional data lines to the central bus.
- E Enable input. Clocks data to and from the ACIA and enables the input/output bus drivers.
- $\overline{\text{IRQ}}$ TTL compatible, open drain, active low output that requests an interrupt when the ACIA interrupts are enabled. It may be tied together with other open-drain interrupt outputs in a polled-interrupt system where the interrupt routine checks the status of each device to determine which one requested service.
- RS Register Select. Tied to address line A0. When low, the status/control registers are selected. When high, the receive/transmit data registers are selected.
- $\overline{\text{RTS}}$ Ready to Send output. Signals the modem that the ACIA is ready to send data. Active low.
- R/ $\overline{\text{W}}$ Read/Write signal from the bus.
- RxCK Receiver clock, normally 16 times the actual data rate.
- RxDData Received data, serial input, least significant bit first.
- TxCK Transmitter clock, normally 16 times the data rate.
- TxDData Transmitter data, serial output, least significant bit sent first.
- Vss System ground.
- Vdd +5 volt supply, nominally 5%.

The ACIA transmits and receives serial data in an asynchronous format, with one start bit, seven or eight data bits, and one or two stop bits, with or without parity. As used in the SCI, the ACIA is set up for one start bit, eight data bits, no parity, two stop bits, and divides the clock by a factor of 16.

Status Register Bit Assignments:

The status register is selected when RS is low, and R/W is high, and the ACIA is selected.

Bit 7	6	5	4	3	2	1	Ø
IRQ	PE	OVRN	FE	CTS	DCD	TDRE	RDA
CTS	Indicates the state of the CTS pin. When high, TDRE is disabled.						
DCD	Indicates the state of the DCD pin. Remains high after DCD goes low, until reset by reading the status register then the data register, or reset by Master Reset.						
FE	Framing error which indicates a lack of the proper stop bit, which can be the result of a poor transmission, or the break condition (open loop).						
IRQ	Interrupt request status, reflects the state of the IRQ pin. High indicates interrupt. Cleared by a read or write data operation.						
OVRN	Indicates a receiver over-run. The last received data was not read by the time the new data was ready.						
PE	Parity Error, when parity is selected, indicates that the parity of the received data did not match the parity of the data transmitted, which results from a lost data bit.						
RDA	Received data available in the receiver buffer.						
TDRE	Transmit Data Register Empty, ready for new data to be entered for transmission.						

Control Register Bit Assignment:

The control register is selected when RS is low, R/W is low, and the ACIA is selected.

Bit 1	Bit Ø	Select	Clock divide ratio, or reset
Ø	Ø		Divide by 1
Ø	1		Divide by 16 (SCI)
1	Ø		Divide by 64
1	1		Master Reset
Bit 4	3	2	Word Length, Parity, Stop bits
Ø	Ø	Ø	7 data bits, even parity, 2 stop bits
Ø	Ø	1	7 bits, odd parity, 2 stop bits
Ø	1	Ø	7 bits, even parity, 1 stop bit
Ø	1	1	7 bits, odd parity, 1 stop bit
1	Ø	Ø	8 bits, 2 stop bits (SCI)
1	Ø	1	8 bits, 1 stop bit
1	1	Ø	8 bits, even parity, 1 stop bit
1	1	1	8 bits, odd parity, 1 stop bit

Bit 6	5	State of RTS	Transmit control
0	0	low	transmit interrupt disabled
0	1	low	interrupt enabled
1	0	high	interrupt disabled
1	1	low	interrupt disabled, break level (open loop) transmitted.

Bit 7	Receive interrupt control
0	disabled
1	enabled

Reference information

For further information on the 8253 Programmable Counter, see the Intel Data Catalog
Intel Corporation
3065 Bowers Ave.
Santa Clara, Ca 95051

For information on the 6820, 6850, and 6852, see the M6800 Microcomputer System Design Data from:
Motorola Semiconductor Products, Inc
Box 20912
Phoenix, Arizona 85036

A good source of data for TTL IC's is:

The TTL Data Book for Design Engineers

Texas Instruments, Inc.
P.O. Box 5012
Dallas, Texas 75222

SCI 2K Monitor version 1.6

This monitor provides the routines that initialize and interface the LSI circuits on board the System Central Interface. Other monitor functions are a video driver for a video display interface, commands to display and alter memory, high-speed cassette routines to store and load blocks of memory or data in a check-summed format (Automatically starting and stopping the tape recorders), assign I/O devices, and program 2708's.

Monitor Operation

When reset is activated, or on initial start-up, the monitor configures the I/O ports, sets the speeds for cassette and serial port operation, and turns off the relays. The monitor then erases the screen of the video display, clears the command buffer area, outputs a prompt character (>) to the main console output device, and waits for a command.

Commands consist of one or two letters followed by hexadecimal addresses where appropriate. Command letters must be followed by a space, then addresses as necessary. If a mistake is made when typing in a command, hit rubout or control H (backspace) to delete the last character typed. Addresses can be from one to four hex characters (0-9,A-F). If more than four hex characters are typed without any intervening space, only the last four characters will be used. For example, if AC100 is typed, only C100 is seen by the monitor. To read 16 bytes of a tape, and place them at 0000 hex, the following is sufficient: RS 0 10 (CR).

All command strings are terminated by a carriage return. At this time, a line feed and carriage return are output, and the command is executed. If the command is erroneous, or there is an error in the command string, ERROR is output and the monitor waits for a new command. After the command has been executed, an appropriate remark is output and the monitor awaits another command.

Escape

All command routines contain an escape. To return to the command mode, just hit the Escape (Esc) key on the main console input device. The routine being executed will abort, and the monitor will wait for a command input. When escape is used to exit cassette routines, the cassette relays are left activated. This allows the operator to rewind, or fast forward the cassette. Before using the cassette routines again, the reset switch must be activated, or a command to go to the start of the monitor. This re-initializes the cassette ports and turns the relays off.

Video Driver Software

This driver assumes that the video interface is a 1k block of memory located at CC00 to CFFF hex, and that CC00 is the upper left-hand corner of the monitor screen. A cursor is displayed on-screen to indicate where the next character will be written. Control commands available are: carriage return, which moves the cursor to the left-

hand margin; line feed, which moves the cursor down one line; control H, a backspace, which moves the cursor back one position (when the cursor is at the left-hand margin, backspace moves it to the right-hand margin, one line up); rubout, does the same thing as backspace; control K, a vertical tab, moves the cursor to the upper left-hand corner of the screen (useful for live-action games, the program can use the upper left corner as a reference point to the rest of the screen when changing parts of the display); control L, form feed, which erases the entire screen and places the cursor at the upper left corner of the screen.

When the last line of the display is filled, the screen is scrolled up one line. The speed at which this occurs can be varied by typing 0-9 during the scrolling process. 0 is the slowest speed, about 2 seconds per line, and 9 is the fastest, about 10 lines per second. Typing a space will stop the scroll. Typing any other character will start it again.

There are differences among the video interfaces offered on the market. The P-Tech VDM requires that bit 7 be low for characters output to the screen. The Poly VTI requires bit 7 be high. The areas where bit 7 is critical are illustrated in the video driver section of the assembly listing.

Jump Locations

At the beginning of the monitor are 12 jump instructions. The first jump simply jumps to the start of the monitor. The following jumps are the solution to easy interfacing with any program. Just call the appropriate routine and the SCI monitor takes over to do all the interface work. No need to worry about port locations, status data, or cassette routines. Each call (3 bytes) replaces at least 10 bytes in a typical status check, data handling routine, and the 12 bytes of cassette functions replace at least 38 bytes of code, in addition to providing much more advanced functioning. So program modification is simple, fast, and saves memory space.

Data in the routines is always handled in the accumulator (A). H is the high-order nibble of the SCI memory location (example, D000, E000, F000, etc.).

- H003 Jumps to the input routine and returns to the calling program with the character from the console input device. Bit 7 is not masked.
- H006 Jumps to the console output routine, outputs the character, then returns.
- H009 Cassette input. Calling this location starts the recorder, waits for a level indication, initializes the cassette circuits, and returns with a data byte. Each subsequent call returns with a byte of data.
- H00C End cassette read operation. Call this location when all the data has been read. This routine then waits for an inter-record gap (a blank spot), then turns off the recorder.
- H00F Cassette write. This routine turns on the recorder, writes a leader on tape, sets the baud rate, outputs

the sync bytes then the data. Subsequent calls will write data to tape.

- H012 Cassette write end, writes a brief trailer, followed by an inter-record gap, turns off the recorder, and returns to the calling program.
- H015 Parallel input from the second parallel input port. (Port H0). Gets the data byte and returns. Useful for paper tape readers or analog-to-digital converters.
- H018 Parallel output, port H6. Outputs a byte, then a strobe pulse to the peripheral, and returns.
- H01B Input status check. The status of the currently-selected input device is polled. If data is not available, the zero flag is set. If data is available, the zero flag is not set, and the accumulator will return with the data byte. This is useful for escape routines, data input, and is directly compatible with Processor Technology software. Bit 7 is masked low on all data (E6 7F).
- H01E Input masked. This routine is identical to H003, but masks bit 7 low for all data. Saves two bytes in the user's program.
- H021 Write B. This routine outputs the data byte passed in the B register. Directly compatible with Processor Technology software.
- H024 *Call Escape, check input character, return*
For details on the use of these jump locations, and interfacing the SCI to popular software, see appendix H, "Patches to Popular Software".

Cassette Format

The cassette tapes written and read by this monitor have the following format: a leader of tone, a clock synchronizing byte (3C hex), a data synchronizing byte (E6 hex), a low-order starting address byte (where the data will be stored), a high-order starting address byte, a high-order block-length byte, a low-order block-length byte (the number of data bytes), the data, and a checksum which is the 8-bit result of adding all the bytes (excluding the clock and data sync bytes), and finally a trailer tone and an inter-record gap (a blank spot).

When an external program is calling cassette functions via the jump locations, the sync bytes and the leader and trailer tones with an inter-record gap are generated by the SCI. The header and data information are the responsibility of the calling program.

Monitor Commands

The SCI monitor will accept both upper and lower case characters. In the command mode, bit 7 is ignored.

In the following explanations, CR means Carriage Return, or simply Return. ADDR means a one to four character hex address. Commands, their operands, and hex addresses must be separated by one space.

- AI K, P, or S(CR) Assign Input device, either Serial, Parallel, or the Keyboard port at IC-44. When reset is activated, input returns to the device specified by the DIP switch (see page 11).
- AO P, S, or V(CR) Assign Output device, either Parallel, Serial, or Video interface using the SCI video software driver.
- D ADDR(CR) Dump hex data from memory. Dumps one line of 16 hex bytes, starting at ADDR. To dump additional data, hit the space bar. To return to the command mode, hit any other character.
- DA ADDR ADDR(CR) Dump ASCII; displays memory data in hex bytes, and the ASCII equivalent. Useful for locating tables and comments in programs.
- E ADDR(CR) Enter memory. The memory address and its content are displayed. If a new byte is desired, type it in and it will be entered into memory. The byte actually stored will be displayed, and the next memory location will be displayed. If the content is to remain unchanged, typing a space will bring the next byte. Typing a non-hex character will terminate the routine. If you want to move backward in memory, hit Control H, a backspace.
- EM ADDR(CR) Enter Memory. Similar to the E command, but no data is read from memory. Sixteen bytes may be entered per line of type. This routine saves paper when using a printer for console output. Use the DA or D command to verify correct entry of the data into memory.
- G ADDR(CR) Go. Transfers execution to that address.
- H ADDR ADDR(CR) Hex arithmetic. Calculates the sum and difference of the two hex numbers. The first number printed is the sum, the second is the result of subtracting the first number from the second.
- I NN(CR) Input from port NN. The byte at the specified port is displayed. To repeat the input, hit the space bar. To return to the monitor, hit any other key.
- M ADDR ADDR ADDR(CR) Move memory from the block specified by

the first two addresses, to a block starting at the third. The data is moved and then verified. Any errors that occurred in the move are listed. Can be used as a simple memory check, see appendix G.

- O NN MM(CR) Output the hex byte MM to the port NN. To repeat the function, type a space. To return to the monitor, hit any other key.
- P ADDR ADDR(CR) Program a 2708 with data from memory beginning at the first address, to the 2708 at the second address, which for the SCI is H800 (D800, E800, etc). When the 2708 is programmed according to Intel specifications, the data is checked, and any errors listed. Allow about 2 1/2 minutes for execution.
- RC(CR) Read Cassette. Reads a cassette tape of the format specified earlier. When finished, writes COMPLETE. If the checksum read in doesn't agree with the checksum on the tape, an error has occurred. In this case, the monitor writes TAPE ERROR.
- RS ADDR ADDR(CR) Read Specify. If no address is given, reads all information in the file and places it in memory, including the header, beginning at 0000. If one address is given, the information is placed in memory starting at that address. If two addresses are given, that block of memory is filled with the first part of the file. The recorder is stopped when it reaches an inter-record gap. The checksum is calculated to check for errors, except where two addresses are given. In that case, TAPE ERROR always appears.
- RV(CR) Read Verify. Reads a file and compares it with memory. Useful for checking files as they are written to make sure there are no errors.
- S ADDR ADDR N1 N2..N9 Search the memory block specified by the two addresses, for the hex character string N1 N2...N9. The address of the start of each string found is printed. Up to 9 bytes may be specified, and a minimum of one, or the routine will loop forever. If all memory is searched, allow 50 seconds for execution.

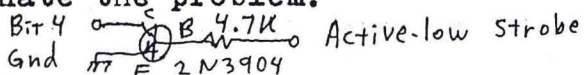
- SR NNNN(CR) Set Read speed for the cassette. The appropriate hex number, NNNN, is given in the Baud Rate table, page C-1. When reset is hit, the SCI returns to the read speed specified in the initialization routine.
- SS NNNN(CR) Set Serial speed for the serial port. Same requirements as SR.
- SW NNNN(CR) Set Write speed for the cassette. The requirements are the same as for SR.
- V ADDR ADDR ADDR(CR) Verify a block of memory specified by the first two addresses, with a block of memory starting at the third address. Useful for checking the programming of 2708's, or changing bits in different memory blocks.
- WC ADDR ADDR(CR) Write Cassette, the memory block specified by the two addresses, in the format defined earlier. The routine says WRITTEN when done. Automatically starts and stops the recorder as do all tape commands.
- Z ADDR ADDR NN(CR) Zero memory from ADDR to ADDR. If NN is not given, zeroes are written. If NN is given, the memory block is filled with that hex byte. Makes a simple means to fill memory with sync bytes to write a sync tape for recorder set-up. Or fill memory with FF to check the erasure of 2708's.

Hitting Escape will cause an exit from all routines, and return to the command mode. If used during a cassette routine, reset must be hit before trying to use the cassette routine again, or Go to the start of the monitor (H000), or output 00 to port H2 the cassette port control.

Cassette commands turn the relays on and off to control two recorders, one for read and one for write. If only one recorder is used, wire the two sets of relay contacts together in parallel, as outlined on page 6, Cassette Control.

Keyboard problems

Keyboards with unlatched outputs may have problems with Escape functions. Increasing the keyboard strobe pulse to 20 ms will allow the strobe and escape character to be recognized, while the monitor is executing a program. Also, some encoders are noisy on the data lines when not active. A false escape character may be occasionally generated which the SCI monitor will interpret as a legitimate escape. Connecting a transistor such as a 2N3904 to bit 4 of the keyboard data lines, and driving it with an active-low strobe will eliminate the problem.



Using the 8253 for a sweep generator.

Using the cassette output pin (2 of IC pad 41 for low level, and pin 3 for high level) as the signal source, and the following program, the 8253 can be programmed to sweep any range of frequencies. This range can start as low as 30 hz, and go as high as 1 mhz (to use the 1 mhz band, the output capacitors of the cassette system must be bypassed, so get the signal direct from pin 11 of IC-31, the 74LS386).

The program as written produces an electronic siren, which provides interesting results when piped through a stereo. For a slowly changing tone that can be used to check the response of an audio amplifier, change the following lines:

```
0000 21 00 30  this changes the start frequency
000A 1E 80     this changes the total range
0013 01 00 E0  this changes the magnitude of the step
```

Program to sweep the 8253

```
0000 21 00 0C  set the starting frequency to 651 hz
0003 01 A0 FF  set B to subtract 60hex each freq change
0006 3E 76     set up 8253
0008 D3 DB     SCI address set for D000. change to suit
000A 1E 10     set number of steps
000C 7D        output L to 8253 counter
000D D3 D9     change D9 for other address of SCI
000F 7C        output H to 8253 counter
0010 D3 D9     change D9 for other address of SCI
0012 C5        Push B to save
0013 01 00 FA  set up a delay
0016 03        increment BC
0017 78        MOV A,B
0018 B1        ORA C    all zeroes yet?
0019 C2 16 00  JNZ      if not, loop
001C C1        POP B    restore BC
001D 09        DAD B    add B to HL
001E 1D        DCR C    decrement step counter
001F C2 0C 00  JNZ      loop until done
0022 C3 00 00  JMP      start all over
```

Try other variations of locations 0000, 000A, and 0013 for different sound effects.

Simple Memory Checker

Using the E command and the M command, a simple check of a block of memory can be made to look for hard errors (Always bad bits). This is a simple, fast memory check. Since it only executes once, it is not always able to find elusive errors, but will pinpoint hard memory failure.

Using the E command, to check and verify entry, enter the following sixteen bytes of data in the first sixteen locations of the block of memory to be tested:
 00 11 22 33 44 55 66 77 88 99 AA BB CC DD EE FF

Hit return and using the Move command, enter:

M ADDR1 ADDR2 ADDR3(CR)

ADDR1 is the beginning address of the sixteen bytes of data, ADDR2 is the ending address of the block of memory, minus 16, and ADDR3 is ADDR1 plus 16.

Example:

A block of unknown memory at 2000 hex to 2FFF is to be tested. First, enter the sixteen test bytes:

E 2000(CR)
 2000 NN 00 00
 2001 NN 11 11
 2002 NN and so on until all 16 bytes are correctly entered. NN above is the present content of the memory location.

Then use the Move command :

M 2000 2FEF 2010(CR)

This command then fills the block of memory with the sixteen bytes of test data and checks for any errors. If any errors do show up, the memory is unusable and should be tested thoroughly to locate the problems.

Interfacing the SCI Monitor to ESP-1

ESP-1 is an Assembler, Editor, and Monitor for an 8080, written for the 8080 by Michael Shrayar. The following patches are for the SCI Monitor version 1.5.

Location	Code before	for SCI	
6C52		CD 06 H0	Output
6CAD		CD 06 H0	Output
70C6	DB 00	C3 1E	Input
70C8	E6 02	H0	
70CA	CA C6 70		
70CD	DB 01	C3 24 H0	Escape Routine
70CF	E6 7F		
70D1	C9		
70DF	DB 00	00 00	Output
70E1	E6 01	00 00	"
70E3	CA DF 70	00 00 00	"
70E6	78	78	"
70E7	D3 01	C3 06 H0	"
70E9	C9		
77E8	26	29	Cassette Read
77EC	26	29	" "
77F0	26	29	" "
77FA	26	29	" "
7815	26	29	" "
781D	CD ED 70	CD 0C H0	" "
7820	21 00 60	CD ED 70	" "
7823	C3 DE 73	21 00 60	" "
7826	CD BD 70	C3 DE 73	" "
7829	DB 6E	CD BD	" "
782B	E6 10	70 C3	" "
782D	C2 26 78	09 H0 78	" "
776C	CD A7 77	C3 74 77	Cassette Write
7776	A7	AA	" "
777A	A7	AA	" "
777E	A7	AA	" "
7782	A7	AA	" "
778C	A7	AA	" "
779A	A7	AA	" "
77A1	21 5F 78	CD 12 H0	" "
77A4	C3 E5 76	21 5F 78	" "
77A7	F5	C3	" "
77A8	CD BD 70	E5 76 F5	" "
77AB	DB 6E	CD BD	" "
77AD	E6 20	70 F1	" "
77AF	C2 A8 77	C3 0F H0	" "

In the Escape routine, if ESC is typed the SCI monitor will take over. This is not a standard character for ESP-1.

In the cassette read routine, if ESP-1 detects an error, the SCI monitor must be reset to turn off the recorder, and reset the cassette port.

The write cassette routine takes full advantage of the SCI monitor to write a tape and control the recorder.

In the above, H stands for the 4k memory block of the SCI (D0, E0, etc.).

Patches for Cromemco 3k Control Basic

Cromemco 3k Control Basic is a simple Basic modelled after Palo Alto Tiny Basic. It has integer arithmetic, and can call its programs located anywhere in memory. Its greatest utility is in control applications, such as Data Acquisition, and process control.

Location	Code Before	Code for SCI	
EE9D	DB 00	F1 E5	Output routine
EE9F	E6 80	F5 E6	"
EEA1	CA 9D EE	7F CD 06	"
EEA4	F1	H0	"
EEA5	E5	00	"
EEA6	F5	00	"
EEA7	E6 7F	00 00	"
EEA9	D3 01	00 00	"
EEEE	DB 00	CD 1B	Input routine
EEF0	E6 40	H0 00	"
EEF2	C8	C8	"
EEF3	DB 01	00 00	"

The SCI input routine checks status of the selected input device, and returns with the zero flag set if no data is available. If data was available, the zero flag is not set, and the accumulator contains the data input.

In the above, H0 represents the memory block of the SCI monitor, such as D0, E0, etc.

MICROCHESS by MicroWare Limited

An aggressive game of chess, a challenge for any player.

Location	Original Code	SCI	
0DF1	DB 00	CD 03	Input Routine
0DF3	E6 40	H0 00	
0DF5	CA F1 0D	00 00 00	
0DF8	DB 01	00 00	
0DE6	DB 00	C3 21	Output Routine, Character
0DE8	E6 80	H0 80	is in B register.
01D7	C3 00 E0	C3 00 H0	Return linkage to monitor

The game of CHASE

01A9	DB 00	CD 03	Input Routine
01AB	E6 40	H0 00	
01AD	CA A9 01	00 00 00	
01B0	DB 01	00 00	

Output is always to the video display memory located at CC00 to CFFF hex. (Normally a VDM-1)

TREK-80

The best game of STAR TREK to hit the market. A live-action game, it's a challenge to win. Output is always to a video display memory which must be equivalent to a VDM-1. TREK-80 is from Processor Technology.

01B0	DB 00	CD 1B	Input Routine
01B2	00	H0	
01B3	E6 40	00 00	
01B5	C8	C8	
01B6	DB 01	00 00	
01B8	E6 7F	E6 7F	

This is a typical Processor Technology input routine and is applicable to most of their software.

D0'00		0005	*****SCI	MONITOR	VERSION	1.6*****
D0'00		0010	PORT	EQU	ODOH	PORT LOCATION
D0'00		0015	STACK	EQU	CDFOH	STACK LOCATION
D0'00		0020	STK0	EQU	STACK+4	INP DEV CODE
D0'00		0025	STK1	EQU	STACK+5	OUT DEV CODE
D0'00		0030	STK2	EQU	STACK+6	SCROLL SPEED
D0'00		0035	STK3	EQU	STACK+7	CASS READ SPD
D0'00		0040	STK5	EQU	STACK+9	CASS WRITE SPD
D0'00		0045	STK7	EQU	STACK+11	SERIAL SPEED
D0'00		0050	STK9	EQU	STACK+13	TEMP STORE
D0'00		0055	STK10	EQU	STACK+14	VDM CHARACTER
D0'00		0060	STK11	EQU	STACK+15	VDM POINTER
D0'00		0065	STK13	EQU	STACK+17	TEMP STORE
D0'00		0070	STK15	EQU	STACK+19	TEMP STORE
D0'00		0075	STK16	EQU	STACK+20	TEMP STORE
D0'00		0080	STK17	EQU	STACK+21	INPUT BUFFER
D0'00		0085	PORT0	EQU	PORT+0	PAR INF
D0'00		0090	PORT1	EQU	PORT+1	CONTROL REG
D0'00		0095	PORT2	EQU	PORT+2	CASSETTE CONTROL
D0'00		0100	PORT3	EQU	PORT+3	CONTROL
D0'00		0105	PORT4	EQU	PORT+4	KEYBD IN
D0'00		0110	PORT5	EQU	PORT+5	CONTROL
D0'00		0115	PORT6	EQU	PORT+6	PAR OUT
D0'00		0120	PORT7	EQU	PORT+7	CONTROL
D0'00		0125	PORT8	EQU	PORT+8	CASS READ CLOCK
D0'00		0130	PORT9	EQU	PORT+9	CASS WRITE CLOCK
D0'00		0135	PORTA	EQU	PORT+10	SERIAL CLOCK
D0'00		0140	PORTB	EQU	PORT+11	CONTROL REG
D0'00		0145	PORTC	EQU	PORT+12	UART CONTROL
D0'00		0150	PORTD	EQU	PORT+13	UART DATA
D0'00		0155	PORTE	EQU	PORT+14	CASS SEDA CONT
D0'00		0160	PORTF	EQU	PORT+15	CASS SEDA DATA
D0'00		0165	**CODE	STARTS	HERE**	
DC0C	C3 27 C0	0170	SCI	JMP	INIT	INIT PORTS
D003	C3 64 C2	0175		JMP	INPUT	INPUT
D006	C3 99 C2	0180		JMP	WRITE	WRITE
D009	C3 D1 C3	0185		JMP	CASR0	CASS INPUT
D00C	C3 D6 C4	0190		JMP	END	TURN OFF RELAY
D00F	C3 9D C5	0195		JMP	CASW0	CASS WRITE
D012	C3 EE C5	0200		JMP	CASW2	END OF WRITE
D015	C3 7C C2	0205		JMP	PIN	PAR INPUT
D018	C3 80 C2	0210		JMP	POUT	PAR OUTPUT
D01E	C3 52 C2	0215		JMP	ISTAT	INP STATUS
DC1E	C3 5E C2	0220		JMP	INFM	INP MASKED
D021	C3 98 C2	0225		JMP	WRITE	B OUT
D024	C3 58 C2	0230		JMP	ICHAR	ESCAPE
D027	31 C0 CF	0235	INIT	LXI	SP,STACK	SET STACK
D02A	3E 0C	0240		MVI	A,0CF	ERASE VIDEO
DC2C	CD BC C2	0245		CALL	VDM+1	
D02F	3E 30	0250		MVI	A,30F	INIT PARALLEL PORTS
D031	C3 D1	0255		OUT	PORT1	
D033	C3 D3	0260		OUT	PORT3	
D035	C3 D5	0265		OUT	PORT5	
D037	C3 D7	0270		OUT	PORT7	
D039	C3 DB	0275		OUT	PORTE	CLOCK REG
D03E	57	0280		SUB	A	SET INPUT PORTS
D03C	C3 D4	0285		OUT	PORT4	

DC3E	C3	'D0	0290	OUT	PORTC	PAR IN	
DC40	3E	'00	0295	MVI	A,00	RESET VDM	
DC42	C3	'C8	0300	OUT	CC8H		
DC44	00	'00	0305	CW	C	CUSTOM	
DC46	00	'00	0310	CW	C		
DC48	00	'00	0315	CW	C		
DC4A	3E	'FF	0320	MVI	A,0FFH	OUT PORT	
DC4C	C3	'D6	0325	OUT	PORT6		
DC4E	3E	'0F	0330	MVI	A,0FF	CASS CONTROL	
DC50	C3	'D2	0335	OUT	PORT2		
DC52	3E	'2C	0340	MVI	A,2CH	ENABLE PORTS	
DC54	C3	'D1	0345	OUT	PORT1	2C=NEG STROBE	
DC56	C3	'D3	0350	OUT	PORT3	2E=POS STROBE	
DC58	C3	'D7	0355	OUT	PORT7		
DC5A	11	'C4	0360	INIT1	LXI	C,STK0	SW ON=K AND V
DC5C	06	'07	0365	MVI	E,07H	KEYBD-VIC	
DC5E	CB	'D2	0370	IN	PORT2	SW OFF=SERIAL	
DC61	07		0375	RLC		IN AND OUT	
DC62	07		0380	RLC			
DC63	07		0385	RLC			
DC64	67		0390	MOV	F,A	SAVE A	
DC6E	E6	'02	0395	ANI	02	MASK SWITCH	
DC67	12		0400	STAX	C	INP DEVICE	
DC68	13		0405	INX	C		
DC69	12		0410	STAX	C	OUT DEVICE	
DC6A	7C		0415	MOV	A,H	GET A	
DC6E	07		0420	RLC	GET	OTHER SW	
DC6C	E6	'02	0425	ANI	C2H	MASK SW	
DC6E	C6	'2C	0430	ADI	2CH	ADD FOR STR	
DC7C	C3	'D5	0435	OUT	PORT5	SET STROBE POL	
DC72			0440	*STROBE	SW ON=NEG , SW OFF=POS**		
DC72	21	'B6	0445	INIT2	LXI	F,TABL2	SET OTHER OPTIONS
DC7E	13		0450	INIT2	INX	C	
DC7E	7E		0455	MOV	A,M	GET DATA	
DC77	12		0460	STAX	C		
DC7E	23		0465	INX	H		
DC75	05		0470	DCR	6		
DC7A	C2	'75	0475	JNZ	INIT2		
DC7E	57		0480	SUB	A	TURN OFF RELAYS	
DC7E	C3	'D2	0485	OUT	PORT2		
DC8C	3E	'03	0490	MVI	A,03H	SET UP SERIAL PORT	
DC82	C3	'DC	0495	OUT	PORTC		
DC84	3E	'11	0500	MVI	A,11H		
DC8C	C3	'DC	0505	OUT	PORTC		
DC8E	3E	'B6	0510	MVI	A,0E6H	SET UP CLOCKS	
DC8A	C3	'DB	0515	OUT	FORTE		
DC8C	3E	'70	0520	MVI	A,70H		
DC8E	C3	'DE	0525	OUT	FORTE		
DC90	1B		0530	DCX	C		
DC91	1A		0535	LDAX	C		
DC92	C3	'DA	0540	OUT	PORTA		
DC94	13		0545	INX	C		
DC95	1A		0550	LDAX	C		
DC96	C3	'DA	0555	OUT	PORTA		
DC9E	21	'D5	0560	STRT	LXI	F,STK17	INITIALIZE INPUT BUFFER
DC9E	36	'0C	0565	MVI	F,0DH		
DC9C	23		0570	INX	F		
DC9E	97		0575	SUB	A		
DC9F	ED		0580	CMP	L		

DCAC	C2 9E	C0	0585	JNZ	STRT+3	
DCA3	31 C0	CF	0590	LXI	SP,STACK	
DCA6	21 E7	C7	0595	LXI	H,CMNTC	
DCA9	CD 31	E2	0600	CALL	COMNT	INITIAL COMMENT
DOAC	0E 28		0605	COMMD	MVI	C,28H
DCAE	21 D5	CF	0610	LXI	F,STK17	BUFF LENG
DOB1	CD 5E	C2	0615	CALL	INPM	GET COMMAND
DGB4	FE 08		0620	CPI	C8H	A BACKSPACE?
DGB6	CA D4	C0	0625	JZ	DELET	
DOB9	FE 7F		0630	CPI	7FH	A RUBOUT?
DGBE	CA D4	C0	0635	JZ	DELET	IF SO, ERASE IT
DGBE	FE 1B		0640	CPI	1BH	ESCAPE CHAR ?
DCCC	CA D4	C0	0645	JZ	DELET	GET RID OF IT
DGC3	FE 0D		0650	CPI	CDH	A CARRIAGE RETURN?
DCC5	CA FA	C0	0655	JZ	CMD1	IF SO, EXECUTE COMMAND
DCC8	77		0660	MOV	M,A	PUT INTO BUFFER
DCC9	CD 99	C2	0665	CALL	WRITE	ECHO CHARACTER
DGCC	23		0670	INX	H	
DGCC	0D		0675	DCR	C	END OF INPUT BUFFER?
DGCE	C2 B1	C0	0680	JNZ	COMMD+5	NO, LOOP
DGD1	C3 CD	C4	0685	JMP	ERROR	YES, TOO MUCH
DOD4	79		0690	DELET	MOV	A,C
DGD5	FE 28		0695	CPI	28H	END OF BUFFER?
DGD7	CA AC	C0	0700	JZ	COMMD	YES, RETURN
DOD7	0C		0705	INR	C	NO, INCREMENT C
DODE	2B		0710	DCX	H	DECREMENT POINTER
DODC	36 0D		0715	MVI	M,0DH	ERASE CHARACTER
DCDE	3E 08		0720	MVI	A,08H	A BACKSPACE
DDEC	CD 99	C2	0725	CALL	WRITE	
DOE3	C3 B1	C0	0730	JMP	COMMD+5	
DOE6	7E		0735	CHK	MOV	A,M
DOE7	23		0740	INX	H	GET CHARACTER
DOE8	C6 20		0745	SUI	20H	POINT NEXT
DCE7	C8		0750	RZ		A SPACE ?
DOEE	C6 20		0755	ADI	20H	RESTORE
DCEC	CD 7E	C1	0760	CALL	CONV4	CONVERT
DOFO	CA CD	C4	0765	JC	ERROR	CARRY SET
DCF3	C6 0A		0770	SUI	CAH	LETTER ?
DOF5	CA CD	C4	0775	JC	ERROR	NO
DOF8	3C		0780	INR	A	
DOF9	C9		0785	RET		
DGFA	21 D5	CF	0790	CMD1	LXI	F,STK17
DCFD	CD 8B	C3	0795	CALL	CRLF	START OF INPUT BUFFER
D100	CD E6	C0	0800	CALL	CHCK	RET AND LINE FEED
D103	17		0805	RAL		CHECK FIRST LETTER
D104	17		0810	RAL		MULTIPLY BY 8
D105	17		0815	RAL		
D106	47		0820	MOV	E,A	SAVE IT IN B
D107	CD E6	C0	0825	CALL	CHCK	CHECK 2ND LETTER
D10A	CA 0E	C1	0830	JZ	\$+1	IT WAS A SPACE
D10C	23		0835	INX	H	
D10E	80		0840	ADD	E	ADD FIRST LETTER VALUE
D10F	22 D1	CF	0845	SHLD	STK13	SAVE POINTER
D112	0E E4		0850	MVI	C,0E4H	COMD COUNT
D114	21 62	C7	0855	LXI	H,TABL1	COMMAND LOOK-UP TABLE
D117	EE		0860	CMD2	CMP	M
D118	CA 25	C1	0865	JZ	CMC3	FIND IT?
D11E	23		0870	INX	H	YES
D11C	23		0875	INX	H	NO

D11E	23	0880	INX	F	
D11E	0C	0885	INR	C	
D11F	CA CD C4	0890	JZ	ERROR	INCREMENT COMMAND COUNT
D122	C3 17 C1	0895	JMP	CMD2	COULDN'T FIND IT
D125	23	0900	INX	F	LOOP
D126	5E	0905	MOV	E,M	GET ADDRESS OF COMMAND
D127	23 :	0910	INX	F	SAVE IN D AND E
D128	56	0915	MOV	E,M	
D129	EB	0920	XCHG	FLACE	DE IN FL
D12A	E9	0925	PCHL	FLACE	HL IN FC AND GO
D12E	F5	0930	CONVO	PUSH	F
D12C	11 00 00	0935	LXI	C,00C0F	SAVE HL
D12F	2A D1 CF	0940	LHLD	STK13	ZERO DE
D132	7E	0945	MOV	A,M	GET POINTER TO BUFFER
D133	FE 0C	0950	CPI	0DH	WAS IT A CARRIAGE RET?
D135	CA 70 C1	0955	JZ	CONV2+8	YES
D138	7E	0960	MOV	A,M	
D139	FE 20	0965	CPI	20H	A SPACE?
D13E	CA 47 C1	0970	JZ	CONV1	YES
D13E	FE 0C	0975	CPI	0DH	A CARRIAGE RET?
D140	CA 47 C1	0980	JZ	CONV1	YES
D143	23	0985	INX	F	INCREMENT POINTER
D144	C3 38 C1	0990	JMP	CONVO+13	LOOP
D147	23	0995	CONV1	INX	F
D148	22 D1 CF	1000	SHLD	STK13	INCREMENT POINTER
D14E	2B	1005	DCX	F	SAVE PCINTER
D14C	CD 68 C1	1010	CALL	CONV2	GET CHARACTER
D14F	5F	1015	MOV	E,A	GET LOWER NIBBLE
D150	CD 68 C1	1020	CALL	CONV2	SAVE IN E
D153	07	1025	RLC		GET NIBBLE
D154	07	1030	RLC		ROTATE
D155	07	1035	RLC		
D156	07	1040	RLC		
D157	83	1045	ADD	E	GET 1ST HALF
D158	5F	1050	MOV	E,A	NOW HAVE 1ST BYTE
D159	CD 68 C1	1055	CALL	CONV2	GET 2ND BYTE
D15C	57	1060	MOV	C,A	
D15D	CD 68 C1	1065	CALL	CONV2	
D160	07	1070	RLC		
D161	07	1075	RLC		
D162	07	1080	RLC		
D163	07	1085	RLC		
D164	82	1090	ADD	C	
D165	57	1095	MOV	C,A	
D166	E1	1100	POP	F	
D167	C9	1105	RET		
D168	2B	1110	CONV2	CCX	F
D169	7E	1115	MOV	A,M	GET DATA
D16A	FE 20	1120	CPI	20H	DONE?
D16C	C2 72 C1	1125	JNZ	CONV3	NO
D16F	E1	1130	POP	F	GET RIC OF LAST CALL
D170	E1	1135	POP	F	
D171	C9	1140	RET		
D172	CD 7E C1	1145	CONV3	CALL	CONV4
D175	CA CD C4	1150	JC	ERROR	CONVERT
D178	FE 10	1155	CPI	10H	CARRY SET
D17A	C2 CD C4	1160	JNC	ERROR	A NUMBER ?
D17C	C9	1165	RET		NO
D17E	C6 30	1170	CONV4	SUI	30H
					ASC BIAS

D180	C8	1175		RC		NOT LET OR NUM
D181	FE 0A	1180		CPI	CAH	
D183	3F	1185		CMC		
D184	C0	1190		RNC		A NUMBER
D185	FE 2E	1195		CPI	2BH	A LOW CASE ?
D187	C4 92 C1	1200		CNC	LCL	
D18A	3F	1205		CMC		
D18E	C8	1210		RC		NO GOOD
D18C	FE 11	1215		CPI	11H	
D18E	C8	1220		RC		NO GOOD
D18F	C6 07	1225		SUI	C7H	A LETTER
D191	C9	1230		RET		
D192	C6 20	1235	LCL	SUI	20H	CONV LOW TO UP
D194	FE 2B	1240		CPI	2BH	NOT LET ?
D196	C9	1245		RET		
D197	CD 2B C1	1250	GO	CALL	CONVC	GET ADDRESS
D19A	FB	1255		XCHG		PUT IN HL
D19E	E9	1260		PCHL		PUT IN PC AND GO
D19C	CD 2B C1	1265	EM0	CALL	CONVC	GET ADDRESS
D19F	EB	1270		XCHG		SAVE IN HL
D1A0	CD B9 C3	1275		CALL	RTHL	WRITE ADDRESS
D1A3	7E	1280		MOV	A,M	
D1A4	CD 9C C3	1285		CALL	RTHL	WRITE BYTE
D1A7	CD 96 C3	1290		CALL	SPACE	
D1A7	CD 5E C2	1295		CALL	INPM	GET CHAR
D1AC	CD 99 C2	1300		CALL	WRITE	ECHO IT
D1BC	FE 20	1305		CPI	20H	A SPACE ?
D1B2	CA 8D C1	1310		JZ	EM1	YES
D1B5	FE 08	1315		CPI	C8H	A BACKSPACE?
D1B7	CA C8 C1	1320		JZ	EM2	YES
D1BA	CD E9 C1	1325		CALL	EM4	
D1BC	7E	1330	EM1	MOV	A,M	GET MEM BYTE
D1BE	CD 9C C3	1335		CALL	RTHL	WRITE IT
D1C1	23	1340		INX	F	
D1C2	CD 8E C3	1345		CALL	CRLF	
D1C5	C3 A0 C1	1350		JMP	EM0+4	
D1C8	2B	1355	EM2	DCX	F	DECREMENT FL
D1C9	C3 C2 C1	1360		JMP	EM1+5	
D1CC	CD 2B C1	1365	EM3	CALL	CONVC	GET ADDR
D1CF	EB	1370		XCHG	FUT	IN HL
D1D0	0E 10	1375		MVI	C,10H	BYTE COUNT
D1D2	CD B9 C3	1380		CALL	RTHL	
D1D5	CD 5E C2	1385		CALL	INPM	
D1D8	CD 99 C2	1390		CALL	WRITE	
D1DE	CD E9 C1	1395		CALL	EM4	
D1DE	23	1400		INX	F	
D1DF	0D	1405		DCR	C	DEC COUNT
D1E0	C2 D5 C1	1410		JNZ	EM3+9	
D1E3	CD 8E C3	1415		CALL	CRLF	
D1E6	C3 D0 C1	1420		JMP	EM3+4	
D1E9	CD 72 C1	1425	EM4	CALL	CONVC	CONVERT BYTE
D1EC	07	1430		RLC	ROTATE	NIBBLE
D1EC	07	1435		RLC		
D1EE	07	1440		RLC		
D1EF	07	1445		RLC		
D1FC	47	1450		MOV	E,A	SAVE IN B
D1F1	CD 5E C2	1455		CALL	INPM	
D1F4	CD 99 C2	1460		CALL	WRITE	
D1F7	CD 72 C1	1465		CALL	CONVC	

D1FA	E0			1470	ADC	E	GET NIBBLE
D1FE	77			1475	MOV	M,A	STORE
D1FC	C3	96	[3	1480	JMP	SPACE	
D1FF	CD	2B	[1	1485	PROG0	CALL	CONVC
D202	EB			1490		XCHG	PROGRAM 2708
D203	CD	2B	[1	1495		CALL	CONVC
D206	3E	A0		1500		MVI	A,0A0F
D208	32	CD	[F	1505	PROG1	STA	STK9
D20E	E5			1510		PUSH	[
D20C	E5			1515		PUSH	F
D20C	01	00	04	1520		LXI	E,04C0F
D21C	CD	C5	[3	1525		CALL	ESCAP
D213	7E			1530	PROG2	MOV	A,M
D214	12			1535		STAX	[
D215	13			1540		INX	[
D216	CD	2B	[2	1545		CALL	[ONE
D219	C2	13	[2	1550		JNZ	PROG2
D21C	E1			1555		POP	F
D21C	[1			1560		POP	[
D21E	3A	CD	[F	1565		LDA	STK9
D221	3D			1570		DCR	A
D222	C2	08	[2	1575		JNZ	PROG1
D225	01	00	04	1580	VERO	LXI	E,C4C0F
D228	C3	26	[5	1585		JMP	VERFY+6
D22E	23			1590	DONE	INX	F
D22C	0B			1595		CCX	E
D22C	97			1600		SUB	A
D22E	F0			1605		ORA	B
D22F	E1			1610		ORA	C
D230	C9			1615		RET	
D231	7E			1620	COMNT	MOV	A,M
D232	CD	99	[2	1625		CALL	WRITE
D235	23			1630		INX	F
D236	F7			1635		ORA	A
D237	F2	31	[2	1640		JP	COMNT
D23A	C9			1645		RET	
D23E	CD	3E	[2	1650	DELA2	CALL	[ELAY
D23E	C5			1655	DELAY	PUSH	E
D23F	01	00	70	1660		LXI	E,70C0F
D242	03			1665		INX	E
D243	97			1670		SUB	A
D244	E0			1675		ORA	B
D245	E1			1680		ORA	C
D246	C2	42	[2	1685		JNZ	[ELAY+4
D249	C1			1690		POP	E
D24A	C9			1695		RET	
D24E	C5			17000	DELAS	PUSH	B
D24C	01	00	E8	1705		LXI	E,0B80CH
D24F	C3	42	[2	1710		JMP	[ELAY+4
D252	CD	86	[2	1715	ISTAT	CALL	CHKST
D255	E6	80		1720		ANI	80H
D257	C8			1725		RZ	
D258	CD	6A	[2	1730	ICHAR	CALL	INPUT+6
D25E	E6	7F		1735		ANI	7FH
D25C	C9			1740		RET	
D25F	CD	64	[2	1745	INPM	CALL	INPUT
D261	E6	7F		1750		ANI	7FH
D263	C9			1755		RET	
D264	CD	52	[2	1760	INPUT	CALL	ISTAT

D267	CA 64	C2	1765	JZ	INPUT	LOOP TIL READY
D26A	3A C4	CF	1770	LDA	STK0	INPUT DEVICE
D26C	E7		1775	ORA	A	
D26E	CA 78	C2	1780	JZ	FIN0	PRIMARY PARALLEL INPUT
D271	3D		1785	DCR	A	
D272	CA 82	C2	1790	JZ	FIN1	OTHER PARALLEL INPUT
D275	CB DD		1795	IN	PORTC	INPUT FROM SERIAL
D277	C9		1800	RET		
D278	CB D4		1805	PINO	IN PORT4	
D27A	00		1810	NOP		CMA IF INV DATA
D27E	C9		1815	RET		
D27C	CB D1		1820	PIN	IN PORT1	CHECK STATUS
D27E	E7		1825	ORA	A	CHECK BIT 7
D27F	F2 7C	C2	1830	JP	PIN	LOOP
D282	CB D0		1835	PIN1	IN PORT0	
D284	00		1840	NOP		CMA IF INV DAT
D285	C9		1845	RET		
D286	3A C4	CF	1850	CHKST	LDA STK0	CHECK STATUS
D289	E7		1855	ORA	A	
D28A	CA 95	C2	1860	JZ	PINS0	PAR STAT
D28C	3D		1865	DCR	A	
D28E	CB D1		1870	IN	PORT1	STATUS PORT
D290	C8		1875	RZ		
D291	CB DC		1880	IN	PORTC	SERIAL STATUS
D293	0F		1885	RRC		GET BIT 0
D294	C9		1890	RET		
D295	CB D5		1895	PINS0	IN PORT5	STATUS PORT
D297	C9		1900	RET		
D298	78		1905	WRITB	MOV A,B	GET DATA
D299	F5		1910	WRITE	PUSH PSW	SAVE A
D29A	3A C5	CF	1915	LDA	STK1	OUT DEVICE
D29C	E7		1920	ORA	A	
D29E	CA BB	C2	1925	JZ	VDM	VIDEO ROUTINE
D2A1	3D		1930	DCR	A	
D2A2	CA B1	C2	1935	JZ	POUT+1	
D2A5	CB DC		1940	SOUT	IN PORTC	
D2A7	E6 D2		1945	ANI	C2H	READY ?
D2AA9	CA A5	D2	1950	JZ	SOUT	LOOP
D2AC	F1		1955	POP	PSW	GET A
D2AC	C3 D0		1960	OUT	PORRD	
D2AF	C9		1965	RET		
D2B0	F5		1970	POUT	PUSH PSW	SAVE A
D2B1	CB D7		1975	IN	PORT7	CHECK STATUS
D2B3	E7		1980	ORA	A	BIT 7 HIGH ?
D2B4	F2 B1	C2	1985	JP	POUT+1	
D2B7	F1		1990	POP	FSW	GET A
D2B8	C3 D6		1995	OUT	PORT6	
D2BA	C9		2000	RET		
D2BE	F1		2005	VCM	POP FSW	GET A
D2BEC	C5		2010	PUSH	B	SAVE REG'S
D2BC	C5		2015	PUSH	C	
D2BE	E5		2020	PUSH	F	
D2BF	F5		2025	PUSH	FSW	
D2CC	2A CF	CF	2030	LHLD	STK11	GET VDM POINTER
D2C3	FE DC		2035	CPI	CH	ERASE SCREEN ?
D2C5	CA 44	C3	2040	JZ	FF	YES
D2C8	FE DC		2045	CPI	GDH	CARRIAGE RETURN ?
D2CA	CA 54	C3	2050	JZ	CR	
D2CC	FE 0A		2055	CPI	0AH	LINE FEED ?

D2CF	CA 6E	[3	2060	JZ	LF	
D2D2	FE 08		2065	CPI	08H	A BACKSPACE ?
D2D4	CA 7D	[3	2070	JZ	ES	A RUB OUT ?
D2D7	FE 7F		2075	CPI	7FH	
D2D9	CA 7D	[3	2080	JZ	ES	
D2DC	FE 0E		2085	CPI	0BH	CTRL K, HOME ?
D2DE	CA 83	[3	2090	JZ	HOME	
D2E1	E6 7F		2095	ANI	7FH	POLY-F6 80
D2E3	77		2100	MOV	M,A	PUT ON SCREEN
D2E4	23		2105	INX	F	
D2E5	CD 3CC	D3	2110	CALL	VD3	END OF SCREEN?
D2E8	CA 32	[3	2115	JC	VD2	
D2EE	3A C6	[F	2120	SC1	LDA	STK2
D2EE	57		2125	MOV	C,A	GET SCROLL SPEED
D2EF	1E FF		2130	MVI	E,OFFH	
D2F1	13		2135	INX	C	
D2F2	97		2140	SUB	A	
D2F3	E2		2145	ORA	C	
D2F4	E3		2150	ORA	E	DONE ?
D2F5	C2 F1	[2	2155	JNZ	SC1+6	LOOP
D2F8	CD 52	[2	2160	SC2	CALL	1STAT
D2FE	CA 19	[3	2165	JZ	SC3	CHANGE SPEED?
D2FE	FE 20		2170	CPI	20H	NO
D300	C2 06	[3	2175	JNZ	\$+3	A SPACE?
D303	CD 5E	[2	2180	CALL	INPM	WAIT FOR CHAR
D306	FE 3A		2185	CPI	3AH	GREATER THAN 9 ?
D308	C2 19	[3	2190	JNC	SC3	YES
D30E	C6 30		2195	SUI	30H	SUB ASCII BIAS
D30F	CA 19	[3	2200	JC	SC3	NOT 0-9
D310	17		2205	RAL		MULTIPLY BY 16
D311	17		2210	RAL		
D312	17		2215	RAL		
D313	17		2220	RAL		
D314	C6 6C		2225	ADI	6CH	
D316	32 C6	[F	2230	STA	STK2	STORE SPEED
D319	21 40	CC	2235	SC3	LXI	H,00C40H
D31C	11 00	CC	2240	LXI	C,00C0CH	START SCROLL
D31F	7E		2245	MOV	A,M	START OF SCREEN
D320	12		2250	STAX	C	GET BYTE
D321	13		2255	INX	C	MOVE IT
D322	23		2260	INX	F	
D323	CD 3C	[3	2265	CALL	VD3	DONE?
D326	CA 1F	[3	2270	JC	SC3+6	
D329	2B		2275	DCX	F	
D32A	36 20		2280	MVI	M,20H	POLY-20
D32C	7D		2285	MOV	A,L	
D32C	FE C0		2290	CPI	COH	DONE ?
D32F	C2 29	[3	2295	JNZ	SC3+16	
D332	36 A0		2300	VI.2	MVI	M,0A0H
D334	22 CF	[F	2305	SHLD	STK11	POLY-OFFH
D337	F1		2310	POP	PSW	SAVE PCINTER
D338	E1		2315	POP	F	RESTORE REG'S
D339	C1		2320	POP	C	
D33A	C1		2325	POP	E	
D33E	C9		2330	RET	CONE	
D33C	7C		2335	VI.3	MOV	A,H
D33C	FE D0		2340	CPI	CD0H	C7-80X24
D33F	C9		2345	RET		RC-80X24
D340	7D		2350	MOV	A,L	GET L

D341	FE	80	2355	CPI	80H	END OF LINE
D343	C9		2360	RET		
D344	21	FF CF	2365	FF LXI	F,0CFFFH	END OF SCREEN
D347	36	20	2370	MVI	M,20H	POLY-AC
D349	2B		2375	DCX	F	
D34A	7C		2380	MOV	A,H	
D34E	FE	CB	2385	CPI	CCBH	DONE ?
D34E	C2	47 C3	2390	JNZ	FF+3	
D350	23		2395	INX	F	
D351	C3	32 C3	2400	JMP	VD2	
D354	36	20	2405	CP MVI	M,20H	POLY-AC
D356	7D		2410	MOV	A,L	
D357	E6	00	2415	ANI	COH	
D359	6F		2420	MOV	L,A	
D35A	7E		2425	MOV	A,M	SAVE BYTE
D35E	32	CE CF	2430	STA	STK10	
D35E	C3	32 C3	2435	JMP	VD2	
D361			2440	***THE FOLLOWING	FCR 80X24***	
D361	7A		2445	MOV	A,C	
D362	9C		2450	SBB	F	
D363	C1		2455	POP	C	
D364	CA	5D C3	2460	JC	CR+9	
D367	7E		2465	MOV	A,M	
D368	32	CE CF	2470	STA	STK10	SAVE CHAR
D36E	C3	32 C3	2475	JMP	VD2	
D36E	3A	CE CF	2480	LF LDA	STK10	GET BYTE
D371	77		2485	MOV	M,A	PUT ON SCREEN
D372	11	40 00	2490	LXI	C,0040H	
D375	19		2495	CAC	C	LINE-FEEDS HL
D376	7E		2500	MOV	A,M	GET BYTE
D377	32	CE CF	2505	STA	STK10	
D37A	C3	E5 C2	2510	JMP	VD1	
D37C	36	20	2515	BS MVI	M,20H	POLY-AC
D37F	2B		2520	DCX	F	
D380	C3	E5 C2	2525	JMP	VD1	
D383	36	20	2530	HOME MVI	M,20H	POLY-AC
D385	21	00 00	2535	LXI	F,0000CH	START OF SCREEN
D388	C3	32 C3	2540	JMP	VD2	
D38E	3E	00	2545	CRLF MVI	A,0DH	CARRIAGE RETURN
D38E	CD	99 C2	2550	CALL	WRITE	
D390	3E	0A	2555	MVI	A,0AH	LINE FEED
D392	CD	99 C2	2560	CALL	WRITE	
D395	C9		2565	RET		
D396	3E	20	2570	SPACE MVI	A,20H	SPACE
D398	CD	99 C2	2575	CALL	WRITE	
D39E	C9		2580	RET		
D39C	F5		2585	RTHX PUSH	PSW	
D39C	1F		2590	RAR		GET UPPER NIBBLE
D39E	1F		2595	RAR		
D39F	1F		2600	RAR		
D3A0	1F		2605	RAR		
D3A1	CD	AF C3	2610	CALL	EINAS	
D3A4	CD	99 C2	2615	CALL	WRITE	
D3A7	F1		2620	POP	PSW	GET BYTE AGAIN
D3A8	CD	AF D3	2625	CALL	BINAS	
D3AE	CD	99 C2	2630	CALL	WRITE	
D3AE	C9		2635	RET		
D3AF	E6	0F	2640	BINAS ANI	0FH	BIN TO ASCII
D3B1	C6	30	2645	ADI	30H	

D3B3	FE 3A	2650	CPI	3AH	OK?
D3B5	C8	2655	RC	YES	
D3B6	C6 07	2660	ADI	07H	
D3B8	C9	2665	RET		NOW ITS DONE
D3B9	7C	2670	RTHL MOV	A,H	WRITE FL
D3BA	CD 9C [3	2675	CALL	RTHL	
D3BC	7D	2680	MOV	A,L	
D3BE	CD 9C [3	2685	CALL	RTHL	
D3C1	CD 96 [3	2690	CALL	SPACE	
D3C4	C9	2695	RET		
D3C5	CD 58 [2	2700	ESCAP CALL	ICHAR	GET CHAR
D3C8	FE 1B	2705	CPI	1BH	ESCAPE ?
D3CA	C0	2710	RNZ		
D3CE	21 8D [7	2715	LXI	F,CMNT6	
D3CE	C3 05 [5	2720	JMP	CMPLT+3	
D3D1	CB D2	2725	CASR0 IN	PORT2	IS RELAY ON ?
D3D3	E6 01	2730	ANI	C1H	
D3D5	C2 1A [4	2735	JNZ	CASR1	
D3D8	CB D2	2740	IN	PORT2	GET DATA AT PORT2
D3DA	F6 01	2745	ORI	01H	TURN ON READ RELAY
D3DC	C3 D2	2750	OUT	PORT2	
D3DE	3E 32	2755	MVI	A,32H	SET UP READ CLOCK
D3EC	C3 DE	2760	OUT	PORT8	
D3E2	3A C7 [F	2765	LDA	STK3	GET READ SPEED
D3E5	C3 D8	2770	OUT	PORT8	
D3E7	3A C8 [F	2775	LDA	STK3+1	
D3EA	C3 D8	2780	OUT	PORT8	
D3EC	CD C5 [3	2785	CALL	ESCAP	WANT TO QUIT ?
D3EF	CB D2	2790	IN	PORT2	LEVEL DETECTION
D3F1	E7	2795	ORA	A	BIT 7 HIGH ?
D3F2	F2 EC [3	2800	JP	CASR0+27	LOOP TIL TONE
D3F5	CD 3E [2	2805	CALL	DELAY	
D3F8	CB D2	2810	IN	PORT2	CHECK LEVEL AGAIN
D3FA	E7	2815	ORA	A	BIT 7 HIGH ?
D3FE	F2 EC [3	2820	JP	CASR0+27	LOOP TIL TONE
D3FE	3E 80	2825	MVI	A,80H	SET UP SSDA
D400	D3 DE	2830	OUT	PORT8	RESET RECEIVER
D402	3E B8	2835	MVI	A,0B8H	8-BIT WORD, SM, 1 BYTE
D404	C3 DF	2840	OUT	PORTF	
D406	3E 82	2845	MVI	A,82H	WRITE TO CGN REG 3
D408	D3 DE	2850	OUT	PORT8	
D40A	3E 70	2855	MVI	A,70H	INT, ONE SYNC CLR STAT
D40C	C3 DF	2860	OUT	PORTF	
D40E	3E 81	2865	MVI	A,81H	WRITE TO SYNC REG
D410	D3 DE	2870	OUT	PORT8	
D412	3E E6	2875	MVI	A,0E6H	SYNC CODE
D414	C3 DF	2880	OUT	PORTF	
D416	3E 03	2885	MVI	A,03H	ENABLE X-MIT
D418	D3 DE	2890	OUT	PORT8	
D41A	CD C5 [3	2895	CASR1 CALL	ESCAP	WANT TO QUIT ?
D41C	DB DE	2900	IN	PORT8	CHECK STATUS
D41F	E7	2905	ORA	A	BIT 7 HIGH ?
D420	F2 1A [4	2910	JP	CASR1	NOT READY
D423	CB DF	2915	IN	PORTF	GET DATA
D425	C9	2920	RET		
D426	CD D1 [3	2925	CASR2 CALL	CASR0	GET SA AND LEN
D429	06 00	2930	MVI	E,00H	ZERO CHECKSUM REG
D42E	6F	2935	MOV	L,A	PUT ADDRESS IN HL
D42C	47	2940	MOV	E,A	

D42C	CD	1A	C4	2945	CALL	CASR1	
D430	67			2950	MOV	F,A	
D431	80			2955	ADC	E	
D432	47			2960	MOV	E,A	
D433	CD	1A	C4	2965	CALL	CASR1	
D436	57			2970	MOV	C,A	PUT BLOCK LEN IN DE
D437	80			2975	ADC	E	
D43E	47			2980	MOV	E,A	
D439	CD	1A	C4	2985	CALL	CASR1	
D43C	5F			2990	MOV	E,A	
D43D	80			2995	ADC	E	
D43E	47			3000	MOV	E,A	
D43F	C9			3005	RET		
D44C	CD	1A	C4	3010	CASR3 CALL	CASR1	GET DATA NOW
D443	77			3015	MOV	M,A	PUT IN MEMORY
D444	80			3020	ADC	E	
D445	47			3025	MOV	E,A	
D446	23			3030	INX	F	
D447	1B			3035	DCX	C	
D448	97			3040	SUB	A	ZERO A
D449	E2			3045	ORA	C	IS D ZERO ?
D44A	E3			3050	ORA	E	IS E ZERO ?
D44E	C2	40	C4	3055	JNZ	CASR3	NO, LOOP
D44E	CD	1A	C4	3060	CALL	CASR1	GET CHECKSUM
D451	90			3065	SUB	B	COMPARE WITH B
D452	57			3070	MOV	C,A	SAVE RESULT IN D
D453	CD	D6	C4	3075	CALL	END	
D456	97			3080	SUB	A	
D457	EA			3085	CMP	C	CHECKSUM OK ?
D458	21	D8	C7	3090	LXI	F,CMNT2	TAPE ERROR
D45E	CC	64	C4	3095	CZ	CASR4	TAPE OK
D45E	CD	31	C2	3100	CALL	COMNT	
D461	C3	98	C0	3105	JMP	STRT	
D464	21	CA	C7	3110	CASR4 LXI	H,CMNT4	COMPLETE
D467	C9			3115	RET		
D468	CD	2B	C1	3120	CASR5 CALL	CONVC	READ AND SPECIFY
D46E	EB			3125	XCHG		SAVE IN H
D46C	E5			3130	PUSH	F	
D46C	2A	D1	CF	3135	LHLD	STK13	
D470	7E			3140	MOV	A,M	
D471	FE	00		3145	CPI	CDH	A CARRIAGE RET ?
D473	E1			3150	POP	F	
D474	C2	9A	C4	3155	JNZ	CASR6	GET ANOTHER ADDRESS
D477	CD	D1	C3	3160	CALL	CASR0	
D47A	06	00		3165	MVI	E,00H	ZERO CHECKSUM REG
D47C	77			3170	MOV	M,A	PLACE BYTE IN MEMORY
D47C	80			3175	ADD	E	KEEP CHECKSUM
D47E	47			3180	MOV	E,A	
D47F	23			3185	INX	F	
D480	CD	1A	C4	3190	CALL	CASR1	
D483	77			3195	MOV	M,A	
D484	80			3200	ADD	B	
D485	47			3205	MOV	E,A	
D486	23			3210	INX	F	
D487	CD	1A	C4	3215	CALL	CASR1	
D48A	77			3220	MOV	M,A	
D48E	57			3225	MOV	C,A	
D48C	80			3230	ADD	E	
D48C	47			3235	MOV	E,A	

D48E	23			3240	INX	F	
D48F	CD	1A	[4	3245	CALL	CASR1	
D492	77			3250	MOV	M,A	
D493	5F			3255	MOV	E,A	
D494	80			3260	ADC	E	
D495	47			3265	MOV	B,A	
D496	23			3270	INX	F	
D497	C3	40	[4	3275	JMP	CASR3	
D49A	CD	EA	[4	3280	CASR6	CALL	EKLEN+4
D49C	50			3285	MOV	C,B	GET 2NC ADDR
D49E	59			3290	MOV	E,C	
D49F	CD	D1	[3	3295	CALL	CASR0	
D4A2	06	00		3300	MVI	E,00F	ZERO CHECKSUM FEG
D4A4	C3	43	[4	3305	JMP	CASR3+3	
D4A7	CD	26	[4	3310	CASR7	CALL	CASR2
D4AA	C3	40	[4	3315	JMP	CASR3	RC PROGRAM
D4AC	CD	26	[4	3320	CASR8	CALL	CASR2
D4B0	CD	1A	[4	3325	CALL	CASR1	RV PROGRAM
D4B3	EE			3330	CMP	M	
D4B4	E2	C4	[4	3335	JNZ	VTERR	MEMORY SAME AS TAPE?
D4B7	80			3340	ADD	E	ERROR
D4B8	47			3345	MOV	B,A	
D4B9	23			3350	INX	F	KEEP CHECKSUM
D4BA	1B			3355	DCX	C	
D4BE	97			3360	SUB	A	
D4BC	E2			3365	ORA	C	
D4BE	E3			3370	ORA	E	
D4BE	C2	B0	[4	3375	JNZ	CASR8+3	
D4C1	C3	4E	[4	3380	JMP	CASR3+14	
D4C4	CD	D6	[4	3385	VTERR	CALL	END
D4C7	21	D4	[7	3390	LXI	H,CMNT3	SHUT OFF RELAY
D4CA	CD	31	[2	3395	CALL	COMNT	
D4CC	CD	8B	[3	3400	ERROR	CALL	CRLF
D4DC	21	E0	[7	3405	LXI	H,CCMNT1	ERROR
D4D3	C3	05	[5	3410	JMPP	CMPLT+3	
D4D6	CD	C5	[3	3415	END	CALL	ESCAF
D4D9	EB	D2		3420	IN	PORT2	QUIT ?
D4DE	E7			3425	ORA	A	CHECK LEVEL
D4DC	FA	D6	[4	3430	JM	END	EIT 7 HIGH ?
D4DF	EB	D2		3435	IN	PORT2	LOOP TIL NG LEVEL
D4E1	E6	FE		3440	ANI	CFEH	A GAP
D4E3	C3	D2		3445	OUT	PORT2	MASK RELAY
D4E5	C9			3450	RET		RESTORE
D4E6	CD	2B	[1	3455	BKLEN	CALL	CONVC
D4E9	EB			3460	XCHG	SAVE	IN HL
D4EA	CD	2B	[1	3465	CALL	CONVC	
D4EC	13			3470	INX	C	
D4EE	7B			3475	MOV	A,E	
D4EF	95			3480	SUB	L	CALCULATE LENGTH
D4F0	4F			3485	MOV	C,A	
D4F1	7A			3490	MOV	A,D	
D4F2	9C			3495	SBB	F	
D4F3	47			3500	MOV	E,A	
D4F4	C9			3505	RET		
D4F5	CD	E6	[4	3510	ZERO	CALL	BKLEN
D4F8	CD	2B	[1	3515	CALL	CONVC	ZERO A MEMORY
D4FE	73			3520	MOV	M,E	NO ZERO ?
D4FC	CD	2B	[2	3525	CALL	CONE	
D4FF	C2	FB	[4	3530	JNZ	ZERO+6	LOOP TIL DONE

D502	21	CA	[7	3535	CMPLT	LXI	F,CMNT4	COMPLETE
D505	CD	31	[2	3540		CALL	COMNT	
D508	C3	98	[0	3545		JMP	STRT	
D50E	CD	E6	[4	3550	MOVE	CALL	EKLEN	MOVE A BLOCK OF MEM
D50E	CD	28	[1	3555		CALL	CONVC	GET START ADDR
D511	7E			3560		MOV	A,M	GET BYTE
D512	12			3565		STAX	C	MOVE A BYTE
D513	13			3570		INX	C	
D514	CD	28	[2	3575		CALL	CONE	
D517	C2	11	[5	3580		JNZ	MOVE+6	LOOP TIL DONE
D51A	21	D7	[F	3585		LXI	F,STK17+2	
D51C	22	D1	[F	3590		SHLD	STK13	
D520	CD	E6	[4	3595	VERFY	CALL	EKLEN	VERIFY MEMORY
D523	CD	28	[1	3600		CALL	CONVC	GET ADDRESS
D526	CD	C5	[3	3605		CALL	ESCAP	WANT TO QUIT ?
D529	1A			3610		LDAX	C	
D52A	EE			3615		CMP	M	COMPARE
D52E	C2	38	[5	3620		JNZ	VMERR	ERROR
D52E	13			3625		INX	C	
D52F	CD	28	[2	3630		CALL	CONE	
D532	C2	26	[5	3635		JNZ	VERFY+6	LOOP
D535	C3	02	[5	3640		JMP	CMPLT	
D538	E5			3645	VMERR	PUSH	F	SAVE H
D539	21	D4	[7	3650		LXI	F,CMNT3	
D53C	CD	31	[2	3655		CALL	COMNT	
D53F	21	E0	[7	3660		LXI	F,CMNT1	
D542	CD	31	[2	3665		CALL	COMNT	
D545	E1			3670		POP	F	
D546	CD	B9	[3	3675		CALL	RTHL	WRITE ADDRESS
D549	7E			3680		MOV	A,M	WRITE EYTE.
D54A	CD	9C	[3	3685		CALL	RTHL	
D54C	CD	96	[3	3690		CALL	SPACE	
D550	CD	5D	[5	3695		CALL	RTDE	WRITE OTHER BYTE
D552	1A			3700		LDAX	C	
D554	CD	9C	[3	3705		CALL	RTHL	
D557	CD	8E	[3	3710		CALL	CRLF	
D55A	C3	2E	[5	3715		JMP	VERFY+14	
D55C	7A			3720	RTDE	MOV	A,D	WRITE DE
D55E	CD	9C	[3	3725		CALL	RTHL	
D561	78			3730		MOV	A,E	
D562	C3	BE	[3	3735		JMP	RTHL+5	
D565	CD	E6	[4	3740	WCO	CALL	EKLEN	WC WRITE CASS
D568	7D			3745		MOV	A,L	WRITE ADDRESS
D569	16	00		3750		MVI	C,00H	ZERO CHECKSUM REG
D56E	CD	9DD	D5	3755		CALL	CASHO	
D56E	57			3760		MOV	C,A	CHECKSUM IN D
D56F	7C			3765		MOV	A,H	
D570	CD	9D	[5	3770		CALL	CASWC	
D572	82			3775		ADD	C	
D574	57			3780		MOV	C,A	
D575	78			3785		MOV	A,B	WRITE ELOCK LEN
D576	CD	9D	[5	3790		CALL	CASWC	
D579	82			3795		ADD	C	
D57A	57			3800		MOV	C,A	
D57E	79			3805		MOV	A,C	
D57C	CD	9D	[5	3810		CALL	CASWC	
D57F	82			3815		ADD	C	
D580	57			3820		MOV	C,A	
D581	7E			3825	WC1	MOV	A,M	GET MEMORY BYTE

DE82	CD	9D	C5	3830	CALL	CASW0	OUTPUT
DE85	E2			3835	ADC	C	ADD CHECKSUM
DE86	57			3840	MOV	C,A	SAVE IN C
DE87	CD	2E	C2	3845	CALL	CONE	
DE8AA	C2	81	D5	3850	JNZ	WC1	LOOP TIL CONE
DE8C	7A			3855	MOV	A,D	
DE8E	CD	9D	C5	3860	CALL	CASW0	
DE91	CD	EE	C5	3865	CALL	CASW2	
DE94	21	C3	C7	3870	LXI	H,CMNT5	WRITTEN
DE97	CD	31	C2	3875	CALL	COMNT	
DE9A	C3	98	C0	3880	JMP	STRT	
DE9C	F5			3885	CASW0	PUSH	PSW
DE9E	CB	D2		3890	IN	PORT2	SAVE A
DEAC	E6	D2		3895	ANI	C2H	IS WRITE RELAY ON
DEA2	C2	E0	C5	3900	JNZ	CASW1	
DEA5	CB	D2		3905	IN	PORT2	TURN RELAY ON
DEA7	F6	D2		3910	ORI	C2H	
DEA9	C3	D2		3915	OUT	PORT2	
DEAE	3E	40		3920	MVI	A,40H	SET UP TRANSMIT
DEAC	D3	DE		3925	OUT	PORTE	
DEAF	3E	B8		3930	MVI	A,0B&H	
DEB1	C3	DF		3935	OUT	PORTF	
DEB3	3E	D2		3940	MVI	A,02H	CONT REG 3
DEB5	D3	DE		3945	OUT	PORTE	
DEB7	3E	70		3950	MVI	A,70H	CLEAR CTS 1U
DEB9	C3	DF		3955	OUT	PORTF	
DEBE	3E	03		3960	MVI	A,03H	ENABLE X-MIT
DEBC	D3	DE		3965	OUT	PORTE	
DEBF	CD	3E	C2	3970	CALL	DELAY	
DEC2	3E	76		3975	MVI	A,76H	
DEC4	C3	DB		3980	OUT	PORTE	SET UP CLOCK
DEC6	3A	C9	CF	3985	LDA	STK5	GET SPEED
DEC9	C3	D9		3990	OUT	PORT9	
DECE	3A	CA	CF	3995	LDA	STK5+1	
DECE	C3	D9		4000	OUT	PORT9	
DEDC	CD	3E	C2	4005	CALL	DELA2	
DED3	CD	3E	C2	4010	CALL	DELAY	
DED6	3E	3C		4015	MVI	A,3CH	OUTPUT CLOCK BYTE
DED8	CD	9D	C5	4020	CALL	CASW0	
DEDE	3E	E6		4025	MVI	A,0E6H	OUTPUT SYNC BYTE
DEDC	CD	9D	C5	4030	CALL	CASW0	
DEE0	CD	C5	C3	4035	CASW1	CALL	ESCAP
DEE3	DB	DE		4040	IN	PORTE	STATUS
DEE5	E6	40		4045	ANI	40H	READY ?
DEE7	CA	E0	C5	4050	JZ	CASW1	
DEEA	F1			4055	POP	PSW	GET A
DEEB	C3	DF		4060	OUT	PORTF	OUTPUT
DEEC	C9			4065	RET		
DEEE	CD	4E	C2	4070	CASW2	CALL	DELAS
DEF1	3E	70		4075	MVI	A,70H	WRITE A TRAILER
DEF3	C3	DE		4080	OUT	PORTE	TURN OFF CLOCK
DEF5	CD	3E	C2	4085	CALL	DELAY	
DEF8	CB	D2		4090	IN	PORT2	WRITE A GAP
DEFA	E6	FC		4095	ANI	CFCH	GET PORT DATA
DEFC	C3	D2		4100	OUT	PORT2	TURN OFF RELAY
DEFE	C9			4105	RET		
DEFF	2A	D1	CF	4110	AIO	LHLD	STK13
DE02	CD	E6	C0	4115	CALL	CHCK	SET INPUT DEVICE
DE05	06	00		4120	MVI	E,00H	

D607	FE	0E		4125		CPI	CBH		
D609	CA	18	[6	4130		JZ	AI1		K FOR KEYBD
D60C	04			4135		INR	E		
D60C	FE	10		4140		CPI	10H		P FOR PAR PORT
D60F	CA	18	[6	4145		JZ	AI1		
D612	04			4150		INR	E		
D613	FE	13		4155		CPI	13H		S FOR SERIAL
D615	C2	CD	[4	4160		JNZ	ERROR		NO GOOD
D618	78			4165	AI1	MOV	A,B		
D619	32	C4	[F	4170		STA	STK0		INPUT DEVICE CODE
D61C	C3	98	C0	4175		JMP	STRT		
D61F	2A	D1	[F	4180	AO0	LHLD	STK13		ASSIGN OUTPUT DEVICE
D622	CD	E6	C0	4185		CALL	CHCK		
D625	06	00		4190		MVI	E,00H		ZERO B
D627	FE	16		4195		CPI	16H		V FOR VDM
D629	CA	38	[6	4200		JZ	A01		
D62C	04			4205		INR	E		
D62C	FE	10		4210		CPI	10H		P FOR PAR PORT
D62F	CA	38	[6	4215		JZ	A01		
D632	04			4220		INR	B		
D633	FE	13		4225		CPI	13H		S FOR SERIAL
D635	C2	CD	[4	4230		JNZ	ERROR		NO GOOD
D638	78			4235	A01	MOV	A,B		
D639	32	C5	[F	4240		STA	STK1		OUTPUT DEVICE CODE
D63C	C3	98	C0	4245		JMP	STRT		
D63F	CD	2E	C1	4250	SR	CALL	CONVC		CASS READ SPEED
D642	EB			4255		XCHG	PUT		IN HL
D643	22	C7	[F	4260		SHLD	STK3		
D646	C3	98	C0	4265		JMP	STRT		
D649	CD	2E	C1	4270	SW	CALL	CONVC		CASS WRITE SPEED
D64C	EB			4275		XCHG	PUT		IN HL
D64C	22	C9	[F	4280		SHLD	STK5		
D650	C3	98	C0	4285		JMP	STRT		
D653	CD	2E	C1	4290	SS	CALL	CONVC		SERIAL SPEED
D656	78			4295		MOV	A,E		
D657	C3	DA		4300		OUT	PORTA		
D659	7A			4305		MOV	A,D		
D65A	C3	DA		4310		OUT	PORTA		
D65C	EB			4315		XCHG			
D65C	22	CE	[F	4320		SHLD	STK7		
D660	C3	98	C0	4325		JMP	STRT		
D663	CD	E6	[4	4330	DA0	CALL	EKLEN		GET LENGTH
D666	CD	8E	[3	4335		CALL	CRLF		
D669	16	0E		4340		MVI	C,08H		SET BYTE COUNTER
D66E	CD	B9	[3	4345		CALL	RTHL		WRITE ADDRESS
D66E	CD	96	[3	4350		CALL	SPACE		
D671	CD	96	[3	4355	DA1	CALL	SPACE		
D674	7E			4360		MOV	A,M		GET MEMORY
D675	CD	9C	[3	4365		CALL	RTHL		WRITE IT
D678	23			4370		INX	H		
D679	15			4375		CCR	C		
D67A	C2	71	[6	4380		JNZ	CA1		LOOP
D67C	11	F8	FF	4385		LXI	C,0FFF8H		2'S COMP 9
D680	19			4390		CAC	C		SUB H BY 9
D681	16	08		4395		MVI	C,08H		SET BYTE COUNTER
D683	CD	96	[3	4400		CALL	SPACE		
D686	CD	96	[3	4405	DA2	CALL	SPACE		
D689	7E			4410		MOV	A,M		GET BYTE
D68A	E6	7F		4415		ANI	7FH		MASK BIT 7

D68C	FE 20	4420	CPI	20H	
D68E	CA A0 C6	4425	JC	SKIP	NOT CHAR
D691	FE 5E	4430	CPI	5EH	
D693	CA A2 C6	4435	JC	FRINT	
D696	FE 61	4440	CPI	61H	
D698	CA A0 C6	4445	JC	SKIP	NOT CHAR
D69E	FE 7E	4450	CPI	7BH	
D69C	CA A2 C6	4455	JC	PRINT	STILL ASCII
D6A0	3E 2E	4460	SKIP	MVI	A,'0'
D6A2	CD 99 C2	4465	PRINT	CALL	WRITE
D6A5	CD 2E C2	44700		CALL	DONE
D6A8	CA 02 C5	4475	JZ	CMPLT	DONE
D6AE	15	4480	CCR	[DECREMENT BYTE COUNT
D6AC	C2 86 C6	4485	JNZ	DA2	LOOP
D6AF	CD C5 C3	4490	CALL	ESCAP	WANT TO QUIT ?
D6B2	C3 66 C6	4495	JMP	[A0+3	CONTINUE
D6B5	CD E6 C4	4500	HEX	CALL	EKLEN
D6B8	1B	4505	CCX	[GET ADDR
D6B9	19	4510	DAD	[
D6BA	CD B9 C3	4515	CALL	RTHL	
D6BC	0B	4520	CCX	E	
D6BE	60	4525	MOV	F,B	
D6BF	69	4530	MOV	L,C	
D6C0	CD B9 C3	4535	CALL	RTHL	
D6C3	C3 98 C0	4540	JMP	STRT	
D6C6	CD E6 C4	4545	SERCH	CALL	EKLEN
D6C9	EB	4550	XCHG		PUT H IN D
D6CA	2A D1 CF	4555	LHLD	STK13	GET BUFF
D6CC	E5	4560	PUSH	F	PUT ON STACK
D6CE	EB	4565	XCHG		RESTORE H
D6CF	2B	4570	CMPRO	CCX	F
D6D0	03	4575	INX	E	
D6D1	EB	4580	XCHG		PUT F IN D
D6D2	E1	4585	POP	F	GET BUFF
D6D3	22 D1 CF	4590	SHLD	STK13	STORE
D6D6	E5	4595	PUSH	F	SAVE
D6D7	EB	4600	XCHG		RESTORE H
D6D8	E5	4605	PUSH	F	
D6D9	[1	4610	POP	[PUT F IN D
D6DA	13	4615	INX	[
D6DE	CD 2B C2	4620	CMPR1	CALL	[ONE
D6DE	CA 02 C5	4625	JZ	CMPLT	
D6E1	E5	4630	PUSH	F	
D6E2	2A D1 CF	4635	LHLD	STK13	
D6E5	7E	4640	MOV	A,M	
D6E6	E1	4645	POP	F	RESTORE F
D6E7	FE 0D	4650	CPI	0DH	END OF STRING
D6E9	CA F9 C6	4655	JZ	CMPR2	YES
D6EC	C5	4660	PUSH	[SAVE D
D6EC	CD 2E C1	4665	CALL	CONVO	GET CHAR
D6F0	7B	4670	MOV	A,E	
D6F1	[1	4675	POP	[RESTORE D
D6F2	EE	4680	CMP	M	COMPARE
D6F3	CA DE C6	4685	JZ	CMPR1	GOOD
D6F6	C3 D1 C6	4690	JMP	CMPRC+2	
D6F9	CD C5 C3	4695	CMPR2	CALL	ESCAP
D6FC	EB	4700	XCHG		QUIT ?
D6FC	CD B9 C3	4705	CALL	RTHL	GET H
D70C	CD 8B C3	4710	CALL	CRLF	WRITE ADDR

D703	EB	4715	XCHG	RESTORE H
D704	C3 CF C6	4720	JMP	CMPRG
D707	CD 2B C1	4725	INP0 CALL	CONVC
D707	21 E9 CF	4730	LXI	F,STK17+20
D70F	36 DB	4735	MVI	M,0CBF
D70F	23	4740	INX	F
D710	73	4745	MOV	M,E
D711	23	4750	INX	F
D712	36 C9	4755	MVI	M,0C9H
D714	CD E9 CF	4760	INP1 CALL	STK17+20
D717	CD 9C C3	4765	CALL	RTHX
D717	CD 3E C7	4770	CALL	COAGN
D71C	C3 14 C7	4775	JMP	INP1
D720	CD E6 C4	4780	OUT0 CALL	EKLEN
D723	1D	4785	DCR	E
D724	4D	4790	MOV	C,L
D725	21 E9 CF	4795	LXI	F,STK17+20
D728	36 7E	4800	MVI	M,07EH
D727	23	4805	INX	F
D72E	36 D3	4810	MVI	M,0D3H
D72C	23	4815	INX	F
D72E	71	4820	MOV	M,C
D72F	23	4825	INX	F
D730	36 C9	4830	MVI	M,0C9H
D732	CD E9 CF	4835	OUT1 CALL	STK17+20
D735	CD 3E C7	4840	CALL	COAGN
D738	C3 32 C7	4845	JMP	OUT1
D73E	CD 5E C2	4850	DOAGN CALL	INPM
D73E	FE 20	4855	CPI	20H
D740	C2 02 C5	4860	JNZ	CMPLT
D743	CD 8B C3	4865	CALL	CRLF
D746	C9	4870	RET	
D747	CD 2B C1	4875	DPO CALL	CONVC
D747	EB	4880	XCHG	
D74E	CD 89 C3	4885	CALL	RTHL
D74E	0E 10	4890	MVI	C,10H
D750	7E	4895	MOV	A,M
D751	CD 9C C3	4900	CALL	RTHX
D754	23	4905	INX	F
D755	CD 96 C3	4910	CALL	SPACE
D758	6D	4915	DCR	C
D759	C2 50 C7	4920	JNZ	EM0+9
D75C	CD 3E C7	4925	CALL	COAGN
D75F	C3 4B C7	4930	JMP	EM0+4
D762		4935	***COMMAND LOOK-UP TABLE***	
D762	11	4940	TABL1 DB	11H
D763	FF D5	4945	DW	A10
D765	17	4950	DB	17H
D766	1F D6	4955	DW	A00
D768	20	4960	DB	20H
D769	47 D7	4965	DW	EM0
D76E	21	4970	DB	21H
D76C	63 D6	4975	DW	CA0
D76E	28	4980	DB	28H
D76F	9C D1	4985	DW	EM0
D771	35	4990	DB	35H
D772	CC D1	4995	DW	EM3
D774	30	5000	DB	30H
D775	03	5005	DB	03

D776	C8				5010	DB	PORT+0EH		
D777	38				5015	CB	38H	G	
D778	97	D1			5020	DW	GO		
D77A	40				5025	CB	40H	H	
D77E	55	D6			5030	DW	FEX		
D77C	48				5035	DB	48H	I	
D77E	07	D7			5040	DW	INPO		
D780	68				5045	DB	68H	M	
D781	0B	D5			5050	DW	MOVE		
D783	6B				5055	CB	6BH	MC	
D784	CD	D4			5060	DW	ERROR	NOT IMPLEMENTED	
D786	78				5065	CB	78H	O	
D787	20	D7			5070	DW	OUTO		
D789	80				5075	CB	80H	P	
D78A	FF	D1			5080	DW	FROGC		
D78C	93				5085	CB	93H	RC	
D78C	A7	D4			5090	DW	CASR7		
D78F	94				5095	DB	94H	RD	
D790	CD	D4			5100	DW	ERROR	NOT IMPLEMENTED	
D792	96				5105	CB	96H	RF	
D793	CD	D4			5110	DW	ERROR	NOT IMPLEMENTED	
D795	A3				5115	CB	CA3H	RS	
D796	68	D4			5120	DW	CASR5		
D798	A6				5125	CB	CA6H	RV	
D799	AD	D4			5130	DW	CASR8		
D79E	98				5135	CB	98H	S	
D79C	C6	D6			5140	DW	SERCF		
D79E	AA				5145	CB	CAAH	SR	
D79F	3F	D6			5150	DW	SR		
D7A1	AB				5155	CB	CABH	SS	
D7A2	53	D6			5160	DW	SS		
D7A4	AF				5165	CB	CAFH	SW	
D7A5	49	D6			5170	DW	SW		
D7A7	E0				5175	CB	CBOH	V	
D7A8	20	D5			5180	DW	VERFY		
D7A7	EB				5185	DB	0BBH	WC	
D7AE	65	D5			5190	DW	WCG		
D7AC	EC				5195	DB	CBCH	WD	
D7AE	CD	D4			5200	DW	ERROR	NOT IMPLEMENTED	
D7B0	EE				5205	CB	CBEH	WF	
D7B1	CD	D4			5210	DW	ERROR	NOT IMPLEMENTED	
D7B3	C0				5215	CB	CDOH	Z	
D7B4	F5	D4			5220	DW	ZERO		
D7B6					5225	***INITIAL MOCE TABLE***			
D7B6	F0				5230	TABL2	CB	CF0H	SCROLL SPEED
D7B7	59				5235		DB	59H	CASS READ SPEED
D7B8	02				5240		DB	C2H	2500 BAUD
D7B9	20				5245		CB	20H	CASS WRITE SPEED
D7B7	03				5250		DB	C3H	2500 BAUD
D7BE	70				5255		DB	700H	SERIAL SPEED
D78C	C4				5260		DB	C4H	110 BAUD
D78C	45	53	43	41	5265	CMNT6	ASC	'ESCAP'	
D7C2	C5				5270		CB	CC5H	
D7C3	57	52	49	54	5275	CMNT5	ASC	'WRITTE'	
	45								
D7C9	CE				5280		DB	CCEH	
D7CA	20	20	43	4F	5285	CMNT4	ASC	'COMPLET'	
	50	4C	45	54					
D7D3	C5				5290		CB	CC5H	

D7D4 56 45 52 49 46 59	5295 CMNT3 ASC 'VERIFY'
D7D7 10	5300 DB CA0H
D7DE 54 41 50 45 20	5305 CMNT2 ASC 'TAPE'
D7EC 20 45 52 52 4F 52	5310 CMNT1 ASC 'ERROR'
D7E6 A0	5315 CB CA0H
D7E7 0D	5320 CMNT0 CB 0DH
D7E8 0A	5325 CB CAH
D7E9 3E	5330 CB '>'
D7EA 10	5335 CB CA0H
D7EE	5340 ***END OF PRESENT ASSEMBLY***

SYMBOL TABLE

A10 D5FF	AI1 C618	A00 D61F	A01 D638	BINAS D3AF	BKLEN C4E6
BE D37C	CASR0 C3C1	CASR1 D41A	CASR2 D426	CASF3 D440	CASR4 D464
CASF5 D468	CASR6 C49A	CASR7 D4A7	CASR8 D4AD	CASW0 D59C	CASW1 C5E0
CASW2 D5EE	CHCK C0E6	CHKST D286	CMD1 D0FA	CMD2 D117	CMD3 C125
CMNT0 D7E7	CMNT1 C7E0	CMNT2 D7DE	CMNT3 D7C4	CMNT4 D7CA	CMNT5 D7C3
CMNT6 D7BC	CMPLT C502	CMPRO D6CF	CMPR1 D6CB	CMPE2 D6F9	COMMD C0AC
CCMNT C231	CONVO C12B	CONV1 D147	CONV2 C168	CONV3 D172	CONV4 D17E
CR D354	CRLF C38B	DA0 D663	DA1 C671	DA2 D686	DELA2 C23B
DELAS D24E	DELAY C23E	DELET D0D4	DMO D747	DOAGN D73B	DONE C22B
EM0 D19C	EM1 C1BD	EM2 D1C8	EM3 C1CC	EM4 D1E9	ENC C4D6
ERRCR D4CD	ESCAP C3C5	FF D344	GO D197	HEX D6B5	HOME C383
ICHAR D258	INIT C027	INIT1 D05A	INIT2 C075	INPC D707	INF1 D714
INPM D25E	INPUT C264	ISTAT D252	LCL D192	LF D36E	MOVE C50B
OLTC D720	OUT1 C732	PIN D27C	PINO D278	PIN1 D282	PINS0 C295
PORT1 C0D0	PORT0 C0D0	PORT1 C0D1	PORT2 C0C2	PORT3 C0D3	PORT4 C0D4
PORT5 C0D5	PORT6 C0C6	PORT7 C0D7	PORT8 C0C8	PORT9 C0D9	PORTA C0DA
PORT8 C0DE	PORTC C0DC	PORTD C0DC	PORTE C0CE	PORTF C0DF	FOLT C280
PFRINT D6A2	PROG0 C1FF	PROG1 D208	PROG2 C213	RTDE D55D	RTHEX C39C
RTHL D3B9	SC1 C2EB	SC2 D2F8	SC3 D319	SCI C000	SEARCH C6C6
SKIP D6A0	SOUT C2A5	SPACE D396	SR D63F	SS D653	STACK CFC0
STKC CFC4	STK1 CFC5	STK10 CFC6	STK11 CFCF	STK13 CFC1	STK15 CFC3
STK16 CFC4	STK17 CFC5	STK2 CFC6	STK3 CFC7	STK5 CFC9	STK7 CFCB
STK9 CFC4	STRT C098	SW D649	TABL1 D762	TABL2 D7B6	VD1 C2E5
VC2 D332	VD3 C33C	VCM D2BE	VER0 C225	VERFY D520	VMERR C538
VIEFR D4C4	WC0 C565	WC1 D581	WRITE D298	WRITE D299	ZERO D4F5

