a survey of LARGE-SCALE DIGITAL COMPUTERS AND COMPUTER PROJECTS

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OFFICE OF NAVAL RESEARCH
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Prepared by

the

Computer Branch

Mathematical Sciences Division

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OFFICE OF NAVAL RESEARCH
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FOREWORD

Submitted herewith is a "Survey of Large-Scale Digital Computers and Computer Projects" prepared by Mr. A. E. Smith of the Computer Branch of the Mathematical Sciences Division, with the assistance of Dr. Mina Rees, Head, Mathematical Sciences Division, and Dr. C. V. L. Smith, Head, Computer Branch. This document is a revision of "A Survey of Large-Scale Computers and Computer Projects" dated August 1948, which in turn is a revision of an article in the Monthly Research Report, 1 November 1947. Grateful acknowledgment is made to the directors of various computer projects who have either prepared material descriptive of their machines or who have revised material written by the Computer Branch. In particular, the section on the Aiken Mark II was prepared by the Naval Proving Ground, Dahlgren, Virginia, and those on the National Bureau of Standards computers by National Bureau of Standards personnel. The information on the Bell Computer Model VI and on the General Electric Computer was obtained from papers by Mr. E. G. Andrews and Mr. B. R. Lester, respectively. The information on European computers is, with the exception of that concerning the ACE, the Swiss computer, and BARK, based on papers or notes prepared by Dr. Sherman Lowell of the London Office, ONR. The write-up on BARK was taken from a paper furnished by Goran Kjellberg, that on the Swiss computer from information provided by E. Stiefel, and that on the ACE from "Development of Computing Machines in Great Britain," by J. H. Wilkinson, April 1949.

It is hoped that this report will be of value to various government agencies and their contractors in providing a summary of current and past work on large-scale digital computers.

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1. GENERAL DISCUSSION[1]

This article attempts to outline some of the characteristics of the large-scale digital computers that have been built or have been designed. The performance charcteristics and computing speeds given for those in the design stage are tentative and are the best guesses that can be made at present. Moreover, it is not sufficient to consider the speeds of the arithmetic and transfer operations only in estimating the time for solution, since the nature of the control and type of coding are also significant factors. Providing additional arithmetic, transfer, and other mechanisms, and performing several operations in parallel, speed up the total computing time generally at the expense of added cost of construction and complexity of coding.

Several electronic digital computers have been completed during the past year and are under test, while others are almost entirely assembled. Therefore one can expect during the coming year that many debatable questions concerned with such things as number base, word length, and checking systems will have partial answers as experience is gained in the use of these computers.

For purposes of discussion, developments in this country may be roughly divided into two classes: Electromechanical computers and electronic computers.

2. ELECTROMECHANICAL COMPUTERS

2.1 Harvard Mark I

The Mark I was the first general-purpose sequence-controlled digital computer in operation. Jointly designed by Howard Aiken of Harvard University and International Business Machines' engineers, it was presented to Harvard by IBM. It employs many standard business machine parts and is distinguished by engineering reliability as indicated by the fact that it has been in operation 95% of the time, according to Professor Aiken, supervisor of its operation. As a result of experience in operating the computer, numerous major changes have been made, one of these being a subsidiary sequence-control unit having 10 subsidiary control mechanisms.

Mark I has been used largely in computing tables of functions in the real and complex domains. Employed in solution of systems of simultaneous linear equations and ordinary differential equations, and in summing series, it has also solved certain partial differential equations. A difficult study of a heat-transfer problem has been completed for the Institute for Mathematics and Mechanics, New York University, under an ONR project. It has also been used by the Naval Proving Ground to test out new methods of control for the Harvard Mark II and Mark III.

Input and output information is recorded on IBM cards or punched paper tape. Provision is made for automatically typing out results of computations in a form ready to be photographed for publishing.

The main interior memory unit stores seventy-two twenty-three-decimal digit numbers in mechanical counters, which accumulate as well as store. Although addition time is 0.3 second

[1] Readers unfamiliar with the literature on design of large-scale digital computers should first read the appendix, p. 24.

and multiplication time 5.8 seconds, provision for parallel operations considerably lowers the average time for these processes.

2.2 Harvard Mark II (The Aiken Relay Calculator)

The Aiken Relay Calculator was designed by and constructed under the supervision of Prof. Howard Aiken at Harvard under a Bureau of Ordnance contract and was moved to the Naval Proving Ground, Dahlgren, Virginia, where it has been engaged in productive work since September of 1948.

The Aiken Relay Calculator is a ten-significant-figure machine, that is, numbers with ten significant figures are stored in the memory, and correspondingly the arithmetic unit accepts ten-digit numbers and produces ten significant figures of sum or product. This is accomplished by virtue of the fact that numbers are carried with a so-called floating decimal point with each number represented as a first significant figure followed by a decimal point and 9 more digits with provision for storing or carrying the power of ten (from 10^{-15} to 10^{+15}) appropriate to the true decimal point position. The term significant has reference here to the number of digits carried and not to the physical significance of the numbers involved, that is, all numbers introduced are treated as though they were significant to a full ten digits even though some of the low order (least significant) digits are zero.

Numbers are introduced primarily by means of paper tape (5-hole teletype tape) at the rate of about 1.5 seconds per number, although, for ease in coding, two seconds are usually allowed in practice. Four such tape-reading mechanisms are available, from which numbers must be taken in serial order at times specified by the coding. Numbers may also be introduced manually via switch settings, provision existing for 24 such 10-figure numbers, or by means of four other tape mechanisms—the so-called interpolator mechanisms, which provide for 207 values of each of four function tables. These tables can be searched to provide up to 8 consecutive function values in the neighborhood of a desired argument, to be used for subsequent interpolation. A switch provides an option for reading either 4 such adjacent functional values or 8 such values. Look-up and interpolation time, assuming multipliers are available when needed, is about 8 seconds at worst and slightly less for low-order interpolation.

The interpolator tapes may be regarded as a special type of slow-speed memory. In addition to the high-speed memory of 100 numbers stored in banks of relays, various frequently used constants are wired semipermanently into machine circuits. Although numbers can be read from any part of the high-speed memory to any other available part in 0.067 second, provision has been made for only 12 such transfers per second.

Addition can be performed in 0.2 second, but 2 available adders permit 8 additions per second. Also, although it requires 0.7 second for a multiplication, 4 available multipliers permit 4 multiplications per second. No special divider exists, but division can be performed by a sequence of multiplication and search operations in about 6 seconds. Provision exists for computing the trigonometric and inverse trigonometric functions, logarithms, and exponentials in 8 seconds or less.

The calculator has been wired in such a way that it is capable of operation as 2 separate units. For ease of scheduling and maintenance it has proved expedient in practice to avoid using the calculator as a whole and whenever possible to code problems for one half only. Used as 2 separate machines, 2 number tapes, 12 sets of constant switches, 50 storage registers, 1 transfer register, 1 adder, and 2 multipliers are available per each half. Operations can be performed on each half at the rate of 6 transfers, 4 additions, and 2 multiplications per second.

The operation of the calculator is controlled by 4 sequence mechanisms (2 for each half) which read instructions punched in code on 6-hole teletype tapes. These tapes may, on appropriate code conditions, transfer control from 1 to the other. Although only one mechanism operates at one time (one on either half in split operation) control may be switched between the various tapes or different locations on the same tape as required by the problem. Since the problems requiring automatic computation usually involve certain basic subsequences of operations to be repeated in some fixed cycle, subject possibly to the character or value of numerical results obtained, the sequence tapes are usually prepared in closed loops permitting

repetition of the cycle as often as desired or until convergence of iteration has been achieved within assigned tolerances. Although problems may be sufficiently complex to require hours or even days of machine operation on one setup, the total length of instruction tapes involved may be no more than would have, without iterations, been sufficient to occupy it for seconds or at most a few minutes.

The principal methods of choice in the calculator hinge on the algebraic signs of particular numerical results. Such signs can be sensed and appropriate action taken, e.g., shift of sequence mechanism, selection of one of two registers, etc., according to whether the control signs are positive or negative.

Numerical output can be obtained in either of 2 ways: (1) Punched on 5-hole teletype tape at the rate of one 10-significant-figure number per 1.5 seconds or (2) typed in tabular form. Four tape punches are available (two on either half), and punched tapes may be read back into the machine concurrently (with a lag of not less than 8 numbers) or in subsequent operations. Four Western Union printers are available (two on either half) with internal checks to verify printing signals thus providing the printed tabulations.

Certain alarm signals exist to warn of specific technical failures, and a system of identity and tolerance checking may be coded into a problem to provide an automatic means of stopping the machine in case of failure of coded mathematical checks. Ideally each small group of steps is either performed twice or preferably carried out two different ways and compared when completed. In practice, fairly long sequences of a few seconds are run by parallel but distinct processes and compared for agreement. In case of failure to meet assigned tolerances, the machine stops and must be "rolled" back to a convenient point of successful check. The roll-back procedure usually requires extensive intervention on the part of the operators to restore the machine to the condition prevailing at the previous check. Insofar as possible all numbers computed between two check points are retained for use in roll-back in case failure occurs. If the failure arises from some intermittent cause, such as certain types of relay failure, a satisfactory check may be obtained on the next try. Otherwise further advance in the problem is suspended until appropriate trouble-shooting has ascertained the cause of failure and remedied it. The problem can then be rolled-back again and resumed. Numbers are stored in the memory units on relays with mechanical latches so that no numbers are lost in case of power failure.

In addition to the trajectory integrations and other exterior ballistic computations incidental to the preparation of firing tables, of ballistic data for fire-control systems, of bombing tables, and of rocket range tables, a number of other problems have been put on the Aiken Relay Calculator. While still at Harvard under test, a set of 38 linear algebraic equations in 38 variables was solved without difficulty. The Proving Ground has successfully completed the solution of a heat conduction problem involving a partial differential equation in one space and one time variable with appropriate boundary conditions. The Calculator has been engaged on an eigenvalue problem relating to microwave attenuation. Other problems now being prepared for machine solution include lead angle determination for air-to-air fire over a variety of target courses and the solution of a system of differential equations fundamental to interior ballistics. Other requests for computing assistance are now under consideration.

An electronic computer with a magnetic memory, the Mark III (to be described later) has been completed at Harvard for BuOrd and work has begun on a Mark IV for the Air Force.

2.3 Bell Telephone Laboratories Ballistic Computer

Bell Telephone Laboratories built for the Naval Research Laboratory at Anacostia, D. C., an automatic electrical mechanism, Computer Mark 22, Mod O (designated by BTL as Model IV) for mathematically evaluating the errors in a control system. In addition to a mathematically skilled person required to obtain numerical results from this equipment, another person, trained in electric circuit maintenance, is necessary in event of electrical troubles, which are infrequent. Computer Mark 22 is of the digital type. Although not an all-purpose machine, modifications have been made to extend its usefulness to a limited field in scientific computations. Another version of the BTL Ballistic Computer (Model III) located at Fort Bliss, Texas, is used for essentially the same purpose as the machine at the Naval Research Laboratory.

The internal memory of this relay machine is ten five-decimal digit numbers, and orders and numbers are introduced from outside by means of coded signals on punched paper tape. Total addition time is 2.4 seconds and total multiplication time[2] is 2.6 seconds. The arithmetic unit is of parallel type.

2.4 Bell Telephone Laboratories Computer (Model V)

One of these machines, designed by G. R. Stibitz and built by Bell Telephone Laboratories under the direction of S. B. Williams, was procured by the Office of the Chief of Ordnance, Department of the Army, and is in operation at Aberdeen. Another was installed at Langley Field for the National Advisory Committee for Aeronautics. The machine's memory consists of 30 "regular" relay registers for numbers, 16 registers for storing signs and 4 "special purpose" registers associated with the arithmetic units, which may be used for storage of numbers under restricted circumstances. The input-output mechanism employs punched paper tape.

The machine employs a "floating decimal point," and a number is then defined to be the algebraic sign, 7 decimal digits, and an exponent (base 10) ranging from -19 to +19 inclusive. According to Franz Alt, formerly of Aberdeen, it requires 2 or 3 months to train a man to code problems for the machine. Even though the machine is an automatically-sequenced machine, of the parallel type, it is limited somewhat by the relatively slow speed of operation. Total addition or multiplication time is two seconds.

A desirable feature is the built-in checking system which causes the machine to stop when a mistake is made and, in many cases, gives an indication as to the cause of the difficulty. The usefulness of the computer is greatly enhanced by the fact that it can be left to run all night, unattended.

2.5 Bell Telephone Laboratories Computer (Model VI)

This computer, built under the supervision of E. G. Andrews, is being operated in the Bell Laboratories, Murray Hill, New Jersey, building. It contains many of the features of the Bell Model V computers originally developed under the direction of Samuel B. Williams. In addition to a small amount of other equipment, it contains about 4300 relays and 86 cold-cathode tubes.

The indicator panel is provided with approximately 600 small lamps for showing the progress of various computing operations and for indicating the numbers in various parts of the computer. Provision is also made on the panel for inserting instructions into the computing program on a manual basis, where necessary to make corrections in the program.

Numbers are in the floating decimal system, being represented by an algebraic sign and 10 decimal digits times a power of 10 ranging from -19 through +19. At present the decimal point is before the first digit, but consideration has been given to a change in design to move the decimal point one place to the right (between first and second digits) in order to simplify the isolation of characteristics of logarithms and to bring the notation into agreement with that commonly used in expressing values in scientific literature. However, this change has been deferred and may not be incorporated.

The built-in automatic checks which have contributed to the great reliability of previous models have been retained, and numerous new features have been added. Perhaps the most important of these features is the provision for wiring in subroutines which occur frequently in calculations. Any one of a possible 200 subroutines can be called for by a single identification code, thus greatly simplifying the coding.

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[2] "Total" addition time or "total" multiplication time represents approximately the time required to order two numbers from the high-speed memory, add or multiply them together, and put the result back in the memory.

At first the Model VI computer was intended principally for the mathematical analysis of the characteristics of complicated networks of telephone and radio circuits. However, it is expected that a considerable portion of the computing will be on problems involving matrix calculation, including integral equations and solution of simultaneous equations, as well as the solution of ordinary and partial differential equations.

3. ELECTRONIC COMPUTERS

3.1 General

The electronic digital computers presently in existence or under design can be divided roughly into four classes, depending on the type of high-speed memory used:

(1) Decade counter rings - The ENIAC, the only one of this class, has no specialized high-speed memory in the strictest sense of the word but is equipped with 20 vacuum-tube accumulators of 10-decimal-digit capacity each. It is now being modified, however.

(2) Acoustic memory - The Moore School EDVAC, the UNIVAC, BINAC, the Raytheon Computers, and the NBS Eastern Computer all employ mercury delay lines.

(3) Electrostatic memory - The major projects for development of an electrostatic memory in this country are the Selectron development at RCA, modifications of the Williams tube development, research at MIT in connection with WHIRLWIND, and a partially completed study at the Raytheon Manufacturing Company under a Bureau of Standards contract on beam deflection tubes employing a holding beam, first demonstrated successfully for a beam deflection tube by A. V. Haeff at NRL. An electrostatic memory of the Williams type is also being added to the NBS Eastern Computer. The University of Illinois and the Eckert-Mauchly Computer Corporation have done research on electrostatic memory and associated circuits for computer application. In an electrostatic memory machine, the digits of a number will generally be transferred in parallel between the high-speed memory and the arithmetic unit, and numbers will be operated upon simultaneously in the arithmetic unit. This is in contrast with serial operation in machines with memories of the acoustic type.

(4) Magnetic drums - The Harvard, Mark III, the Northrop MADDIDA and the G. E. Computer employ magnetic drums, and Engineering Research Associates, Inc. are independently investigating this type of storage. Dr. Paul Morton, of the University of California, Berkeley, is building under ONR contract a simplified digital computer which uses magnetic storage. Some of the computers with electrostatic storage employ auxiliary magnetic drum memories.

Although almost all large-scale electronic machines are called general-purpose computers, the description is not entirely accurate, for engineering economy dictates that the general classes of problems to be solved determine the design of the computer to a great degree. A machine for data reduction, for example, might be relatively slow and require only a limited amount of flexibility of control, whereas a computer to solve some of the complicated equations of mathematical physics should be extremely flexible to provide for complicated coding processes, have a large high-speed memory to store boundary conditions and intermediate results, and perform calculations rapidly so that solutions can be obtained in a reasonable time. If a machine is intended for census problems it should have a fairly large high-speed memory and a very large and flexible auxiliary memory in multiple channels for sorting purposes, and should be capable of transferring data readily in blocks and extracting small items of information from larger words.

3.2 IBM Selective-Sequence Electronic Calculator

The new IBM Selective-Sequence Electronic Calculator, first demonstrated to the public 27 January 1948 at the IBM headquarters in New York, is discussed at this point since it combines both the electromechanical relay and electronic techniques. This general-purpose calculator, which has sufficient memory and flexibility to handle most problems, is available to government agencies, as well as to universities and business concerns. Typical problems for which solutions have been obtained are as follows: (a) In fluid mechanics, investigation of stability of flow, (b) in nucleonics, dynamical analysis of nuclear fission (liquid drop model), (c) in optics, ray tracing through a complex lens system, (d) in mechanics, bending shear and

rotary inertia problems for the David Taylor Model Basin, U. S. Navy, (e) in aerodynamics, a problem involving the integration of 14 simultaneous, first order, nonlinear differential equations, under subcontract for the Office of Naval Research, U. S. Navy, (f) in ballistics, a problem concerning reflection and refraction of shock waves for the Bureau of Ordance, U. S. Navy, and (g) in astronomy, integration of the orbits of the five outer planets.

Numerical information and instructions for the calculating procedure are generally read from holes punched in either IBM cards or continuous card stock tape. The reading speed from cards through two card feeding units is 1500 twenty-decimal digit numbers (19 decimal digits plus algebraic sign) a minute and from the 66 tape-reading units about 7000 numbers a minute. Problem results may be recorded in punched cards or in printed record form or both, the recording speed for cards being about 800 numbers a minute and for printed records about 1200 numbers a minute.

The memory unit comprises three types of storage: Eight numbers in electronic form, 150 in relays, and 20,000 in card stock tape. There are 66 tape-reading stations which can be used interchangeably for numbers or sequencing instructions. Of these, 36 comprise a table look-up unit connected with a searching mechanism which locates whatever particular information is required for reference. The maximum look-up time for a complete search of a 5000-number table is about three seconds.

In the arithmetic unit, which is electronic, multiplication is performed by the method of repeated additions. Division is performed in the same part of the unit as multiplication, but a separate accumulator is provided for addition and subtraction. Addition time of two 19-decimal-digit numbers is 0.3 millisecond. Multiplication (14-digit x 14-digit to 28-digit product) requires 20 milliseconds, and division (14-digit ÷ 14-digit to a 14-digit quotient) takes 26 milliseconds on the average. Sequencing information is introduced through the medium of holes on cards or card stock tape, the instruction unit being a 20-digit, 4-address code. One line of coding contains 2 instruction units; and each line can be introduced to the computer in 40 milliseconds, i.e., 20 milliseconds an order. Since this time is approximately that of multiplication, the computer is so arranged that waiting for orders does not in general slow up this process. Although the arithmetic unit adds very quickly, and the time to get 2 numbers from the relay memory, add them together, and put the result back in the relay memory, is short, the process requires 20 milliseconds on the average because operations cannot take place faster than the orders come in. However, 1 line of coding can be used to order that 5 numbers be added together in sequence.

3.3 The ENIAC

The ENIAC (Electronic Numerical Integrator and Computer), built during the war by the Moore School of Electrical Engineering of the University of Pennsylvania under contract with the War Department, Office of the Chief of Ordnance, was operated at the Moore School until moved to Aberdeen in the fall of 1947.

The ENIAC was the first large-scale high-speed electronic digital computing device. It performs a sequence of operations without manual attention, except for setting up, the operations being: (1) Reading initial data from IBM cards; (2) addition; (3) subtraction; (4) multiplication; (5) division; (6) finding square roots; (7) looking up function values in function tables; and (8) punching the results on IBM cards. Twenty ten-decimal-digit numbers can be stored in electronic counters (accumulators). Addition time is 200 microseconds and multiplication time is about 2800 microseconds for 10-digit by 10-digit multiplication. Even though arithmetic operations are performed rapidly, the relatively slow input speed of thirteen and output speed of sixteen ten-decimal-digit numbers per second from IBM cards considerably increases the time required to solve most problems.

The ENIAC was first designed as a device primarily for solving ordinary differential equations. Since generality of the ENIAC was limited by small internal memory, lack of flexibility, and the relatively slow input and output, changes have been made to make it applicable to a wider class of problems. It has solved problems in nuclear physics, for example. However, it is still most efficiently used for handling fairly simple computations which must be repeated many times, as in the case of calculating firing tables.

When the ENIAC was moved to Aberdeen, the coding was greatly simplified by use of a scheme (proposed by Dr. John von Neumann) for setting up instructions by means of dials on a section of the presently existing function tables instead of by complicated sets of switch settings and cable connections. By adding a small amount of auxiliary equipment, sixty distinct orders were made available. Later, provision was made for the installation of a new panel, the converter, which has made possible the expansion of the sixty-order code to the ninety-odd orders presently available.

Recently, during a month's operation, the ENIAC was available for computation (i.e., free from electrical and mechanical difficulties) 85% of the time. When the loss of time required to set the machine up and that due to programming errors is counted in, the utilization efficiency of the machine was about 67%.

3.4 The EDVAC

This computer was constructed at Moore School of Electrical Engineering under a contract with the Ordnance Department, U. S. Army, some chassis construction and mechanical work having been done under a subcontract with the Reeves Instrument Corporation in New York.

Consisting of 128 eight-word delay lines, the acoustic memory has a total capacity of 1024 forty-four-binary-digit words. Total addition time is about 800 microseconds and total multiplication time is about 2800 microseconds, on the average. The EDVAC is designed with two identical algebraic units, working into a checking system. However, one algebraic unit may be locked out, in which case the checking is inoperative.

The EDVAC employs a four-address code, i.e., an instruction can specify the memory location of the two operands, the disposition of the result of the operation, and the location of the next instruction. Division, addition, and multiplication are built-in processes, with provision for double precision operations. Facilities exist for automatically changing the routine when machine capacity has been exceeded.

The arithmetic element and the mercury delay memory have operated satisfactorily in component tests, and the dispatcher has been made to perform all machine orders. Although magnetic techniques were to be used in the input-output unit, teletype equipment is being provided for the interim period of operation. The computer has been moved to Aberdeen Proving Ground, where testing is being completed.

3.5 The UNIVAC

The UNIVAC, a computer using a mercury memory unit, has been designed by the Eckert-Mauchly Computer Corporation. At the present time the corporation has contracts for six such machines with various government agencies and commercial concerns. Although special features have been incorporated in the design to make it suited to the handling of large quantities of statistical data, the machine is also applicable to the solution of problems of a general nature. The UNIVAC design proceeded in parallel with BINAC testing, and operating experience on the BINAC has lead to some recasting of the UNIVAC design for greater reliability and ease of operation. (See next section for description of BINAC.)

The high-speed memory is composed of 10-word acoustic channels in a cylindrical tank of mercury, total memory capacity being 1000 words of 12 decimal digits each. In order to provide for both numbers and letters, 7 binary digits are employed to represent each character including sign. Thus 91 binary-digit positions are allotted to each word, plus the space (7 binary-digit positions) between words.

For representation of numbers the Eckert-Mauchly Corporation uses the excess-three coded decimal system, originated by Dr. George Stibitz, in which each of the separate decimal digits is represented in terms of a set of 4 binary digits. The presence or absence of a voltage pulse in a particular code group is represented by 1 or 0 respectively. Of the possible 16 combinations in a 4-pulse group, 10 are chosen which permit addition by modified binary processes

and which form nines complements by reversing the coding. For example, the coding for 2 is 0101, and that for 7 is 1010. Each decimal digit (d) is represented by the binary number which is equal to d+3.

Decimal No.	Code
0	0011
1	0100
2	0101
3	0110
4	0111
5	1000
6	1001
7	1010
8	1011
9	1100

By placing the proper digits in combination with the above code, and by proper choice of other symbols, all pulse combinations used have an odd number of pulses (binary "ones"); checking circuits continuously monitor the signals so that any loss or gain of pulses which results in an even number of pulses in a digit group will be detected. Arithmetic operations are checked by duplicate computing circuits.

In order to facilitate sorting and collating, the external memory may employ as many as ten magnetic tapes, any one of which may be instructed to read or record at any time. In a typical case, two tapes may be used for raw data input, two for output, and six for temporary storage of intermediate results. These units are designed to transfer information to and from the internal memory at a rate of 10,000 characters per second. Special registers have been provided to enable the shifting of data between low- and high-speed memories in 60-word blocks and the transfer of data within the high-speed memory in 2- or 10-word blocks.

The machine can carry out 41 different instructions. Addition time is about 525 microseconds and multiplication 2150 microseconds, including the time required on the average to obtain the order from the memory and to transfer a number from the memory and add it to or multiply it by a number in the arithmetic unit. A transfer between the memory and the accumulator requires 315 microseconds on the average.

Since Eckert-Mauchly Computer Corporation became a subsidiary of Remington Rand, Inc., production schedules have been stepped up and two complete systems are being constructed simultaneously. These will be followed by a lot of at least three additional systems. It is anticipated that production of the first lot will be completed and tested this year.

3.6 The BINAC

The BINAC was built by the Eckert-Mauchly Computer Corporation for Northrop Aircraft, Inc., which has a USAF contract. The computer, which operates at a four-mcps repetition rate, was successfully demonstrated to the public during August 1949. Two BINACs were given the same problem and interconnected in such a way as to compare the results of separate operations in the solutions of this problem continuously. In a formal test for the Bureau of Standards, the computer had a down time of 23 minutes during a four-hour run, and it has been reported by company engineers that one sample error-free run was 40 hours long. The machine is capable of performing 3500 additions or subtractions or 1000 multiplications or divisions per second. If access time to the internal memory is included, addition requires about 800 microseconds and multiplication about 1200 microseconds.

The computer operates in the binary number system as its name indicates, but information is introduced to it in octal form. In order to attain programming flexibility, provision is made for 16 instructions including arithmetic processes, data-handling orders, and branching instructions.

The memory is of the mercury acoustic type of special design and contains 18 channels in a cylindrical tank of mercury. Of these, sixteen are used for data storage, one for maintaining constant temperature throughout the mercury tank, and the other as a spare. It is capable of storing 512 words of 30 binary digits each. Initial introduction of numbers and instructions is by means of a keyboard which causes groups of pulses to pass through suitable conversion equipment directly to the acoustic memory without use of tape or card input media. This information or the results of computations can be transferred from the computer to magnetic tapes and reintroduced to the computer if desirable at a later time. Provision is also made for typing out a printed record of the results of computation.

3.7 NBS-ONR-Raytheon Digital Computer

An electronic digital computer was designed for the Office of Naval Research under a National Bureau of Standards contract with the Raytheon Manufacturing Company. Performance requirements set for the machine include handling of such general classes of problems as the solution of nonlinear differential equations, the problem of systematic sorting, and the preparation of statistical data.

Later the development of this computer was coordinated with the purchase of computers for BuAer and USAF under an ONR Special Devices Center contract. The detailed design of the SDC computers will be, in general, used for the NBS-ONR computer.

Although at first an acoustic memory of 32 mercury lines having 32 words per line will be employed, provision is being made for subsequent addition of two or three thousand words without materially altering existing circuits. The repetition rate in the memory is set at 3.7 mcps, and other circuits at 1 mcps. The word length is to be 35 binary digits, all to the right of the binary point. For checking of storage and transfer, a weighted count of the number of binary ones in a number is made and is stored with the number. On transfer, the count is separated out and a new count is made to check that the two counts agree. Arithmetic operations are also checked using an arithmetic weighted count in a process similar to the old method of casting out nines.

The Raytheon computer project group has made a study of typical processes occurring in general mathematical computations. Mathematical processes ranging from polynomial evaluation to the solution of ordinary differential equations have been analyzed. For several of these processes, sets of data have been inserted and the processes carried out in sequence as programmed for machine computation. The main objects of this mathematical study have been to determine: (1) The relative frequency of the basic arithmetical operations; (2) the number of references to and depositions in the memory; (3) the number of transfers, both within the internal memory and between external and internal memory; (4) the frequency of reading in data and reading out final results; and (5) the need for using scale factors (fixed-decimal machine). Results of the study have given desirable relative speeds for the performance by a computing machine of the operations studied.

Four input-output units employing multichannel magnetic tapes, each reel having a capacity of 100,000 words, will be employed. Connected with each unit are two 32-word reservoirs. Reading from the tapes and writing on the tapes are accomplished in blocks of 32 words at a time. In order to enable central control to govern all transfers between the arithmetic unit and the reservoirs, the latter will have special address codes, similar to the formal address codes. The input to the machine is locally controlled by each of the external memory units, the input rate from each of the four units being 500 words per second on the average. As long as this average rate is not exceeded, the access time is 10 microseconds per word.

For the purpose of putting numbers or orders on the magnetic tapes, a problem-preparation unit is supplied with the machine. Orders are written in octal form and numbers in decimal or binary form. By use of a previously prepared sequence of instructions, decimal numbers are converted into binary numbers within the machine.

Total addition time, including checking and memory reference, is approximately 620 microseconds, and multiplication time is approximately 950 microseconds. Since the machine will operate on a variable cycle basis, a new memory selection can begin the moment the

previous one is completed. When the necessary selection of operands has been completed, the arithmetic unit will immediately perform the specified operation; and the disposition of the result, if any, will occur as soon as the operation is completed. Provision has been made for floating operations, in which numbers are represented as a binary fraction times 2^n, where $n = \pm 35$. Work on the NBS-ONR computer has been held up awaiting design and preliminary component research for the SDC computers, the results of which are to be used in this computer. However, the variations of the NBS from the SDC computer have been largely worked out, the memory tank has been constructed, and other components are in the process of construction. The computer should be completed by September 1951.

3.8 Special Devices Electronic Digital Computers

These computers are being built by Raytheon for BuAer and the Air Force under a Special Devices Center contract. The internal mercury acoustic memory has a capacity of 1152 words, each occupying 36 pulse positions, the actual word length being 30 binary digits. The auxiliary storage uses six-channel magnetic tapes, for which efficient tape-handling mechanisms have been prepared. In order to decrease spacing between channels, newly designed thin magnetic heads are employed.

Average total addition time is 530 microseconds and multiplication time is 815 microseconds, average access time to the internal memory being 128 microseconds.

The computer will contain 3600 tubes and eight thousand crystals and will occupy a net floor space of about 800 square feet. It is estimated that two operators, three mathematicians, and three maintenance men will be required. The first computer is nearing completion, and system tests should be completed in the fall of 1950.

3.9 National Bureau of Standards Eastern Automatic Computer

The National Bureau of Standards Eastern Automatic Computer, (formerly "interim"), now completely assembled at the National Bureau of Standards, is a general-purpose electronic digital computer of modest performance characteristics. The construction of this computer was undertaken with the support of the Office of the Air Comptroller. Located on the grounds of the National Bureau of Standards, the computer will provide the Bureau with a tool for the investigation of certain specialized problems pertaining to the work of the Office of the Air Comptroller as well as for the solution of general mathematical problems. In addition, the computer will serve as an instrument for conducting performance tests on various types of supplementary equipment. This dual usage of the computer has led to the adoption of certain special design features intended to facilitate the subsequent annexation of additional equipment. Accordingly, the computer may be treated as a nucleus to which new internal units capable of enhancing its problem-solving ability may be added from time to time.

Initially the computer was provided with a 512-word internal acoustic memory unit, a prototype 32-word electrostatic memory unit (utilizing the Williams technique), and modified teletype input-output equipment. It is intended that a new type magnetic wire-handling mechanism, an experimental high-speed printing device capable of writing 30 lines per second with 50 digits in a line, and magnetic tape input-output mechanisms will be added during the summer and fall of 1950. A 45-tube, 512-word electrostatic memory is being constructed for incorporation and evaluation with the computer. The machine has been so designed that both the serial-type acoustic and parallel-type electrostatic memories can be used simultaneously, and provision has been made for possible increase of the combined memory capacity up to 4096 words.

Basically, the computer is a serial type and operates in the binary system at a one-megacycle pulse repetition rate. Both numbers and instructions are represented by words consisting of 45 binary digits (44 numerical digits and an algebraic sign digit).

The computer has been designed to operate using either of two distinct types of instruction words: (1) A 4-address instruction word, and (2) a 3-address word. Currently, only the 4-address system of operation is available on the computer. However, the computer has been

so laid out that when the 3-address system is completed and incorporated in the computer, the operator will be able to select either mode of operation.

Types of operations and average performance times are listed in the table below:

Operation (With Abbreviation)	Time (in Milliseconds) for Complete Operation (Including Access Time)			
	Mercury Delay Line Memory			Electrostatic Memory
	Max	Min	Average	
1. Addition (A)	1.5	0.2	0.9	0.2
2. Subtraction (S)	1.5	0.2	0.9	0.2
3. Multiplication (a) Major part, unrounded (M) (b) Major part, rounded (R) (c) Minor part (N)	3.6	2.4	3.0	2.4
4. Division (D)	3.6	2.4	3.0	2.4
5. Comparison (A conditional transfer of control based on value of arithmetical result) (a) Algebraic value (C) (b) Absolute value (K)	1.2	0.2	0.7	0.2
6. Logical Transfer (L) (An arbitrary partial word transfer for the purpose of forming composite words)	1.5	0.2	0.9	0.2

During the shakedown period of the machine several small problems have been completed. One such completed test problem is the computation of 31 skew rays through a system of 9 lenses for the Electricity and Optics Division of the National Bureau of Standards.

By the use of transformer-coupled germanium diode gating throughout the high-speed circuitry, the tube complement of the computer has been kept at about 1200, including both the acoustic and electrostatic memories. "Clusterizing" the roughly 19,000 crystals simplifies trouble shooting and replacement in the event of breakdown. The computer occupies approximately 150 square feet of floor space even though accessibility rather than compactness has been stressed in the construction. With all auxiliary equipment comtemplated in use, the power requirement will be approximately 15 kw.

The realization of the computer has been achieved as the result of a joint effort of the Mathematics and Electronics Divisions of the National Bureau of Standards, the detailed design and construction being under the direction of S. N. Alexander and R. J. Slutz of the Electronic Computers Section.

Research on a special-purpose computer for maximization processes arising in logistic planning is also being sponsored by the Air Comptroller's Office.

3.10 Institute for Advanced Study Computer

At the Institute for Advanced Study, Princeton, work goes forward under the direction of Professor J. von Neumann on a very high speed, general-purpose electronic digital

computer embodying the results of previous development in the field. His chief assistant is H. H. Goldstine, and J. H. Bigelow is chief engineer. The intended use for this machine is the mathematical investigation of physical phenomena involving, in particular, the solution of certain nonlinear partial differential equations, for which a means of solution has not heretofore been available. The project is partially supported under a contract with the Research and Development Service, Ordnance Department, U. S. Army. AEC, ONR, and USAF are contributing to the support of this Army contract.

An F. C. Williams type electrostatic memory of 40 tubes, storing a total of 1024 forty-binary-digit numbers is to be employed. The digits are represented as charge distributions appearing as dots and dashes on the face of an ordinary cathode-ray tube. In the design of Professor Williams, information was stored or read serially by means of a television type raster. For reading, he used a pickup plate consisting of metal foil or gauze, attached to the face of the tube, to provide capacitive coupling to an output amplifier. In order to secure permanence of storage, the information was restored sequentially a line at a time between "action" cycles. (During an "action" cycle access is made to the memory in the process of carrying out an instruction.)

About a year ago, Dr. Bigelow spent some time with Professor Williams at Manchester, England, and returned to the Institute to design a memory which operates in a parallel fashion rather than the series mode used by Williams. By transferring all the digits of a number simultaneously to or from corresponding points in all forty tubes, access time is greatly diminished. A number of cathode-ray tubes have been selected for the memory and the construction and wiring of the complete Williams memory has been completed.

The arithmetic element and arithmetic control have been built and tested, and work on the central control is well along. The arithmetic element operates in parallel, i.e., all digits are operated upon simultaneously, thus yielding a considerable speed performance factor over serial arithmetic processes. Not counting access time to the memory, addition requires about 15 microseconds and multiplication about 400 microseconds. Access to the Williams tube memory should be approximately 25 microseconds. Average total addition and multiplication times are approximately 95 microseconds and 500 microseconds, respectively.

Considerable effort has been expended to minimize the number of tubes and amount of other equipment required and to make the units as compact and accessible as possible. A clever 3-dimensional wiring system has been worked out whereby leads cross at right angles to minimize pickup and compactness and accessibility are secured.

Orders and numbers will be punched on paper tape by standard teletype machines and then transferred from the tape to a magnetic wire through a converter. Because of the characteristics of the memory, the machine will be capable of storing and discharging words while the magnetic wire is accelerating or decelerating.

Considerable research has been done in the field of numerical methods, coding of problems and the logical design of electronic computers. Work at the Institute on approximation and error theory is being carried out under ONR contract.

Copies of the IAS computer are under construction at the University of Illinois, Los Alamos Scientific Laboratory, and Argonne National Laboratory.

3.11 WHIRLWIND

A very-high-speed electronic computer, designed primarily for control applications, but capable of use as a general-purpose machine, is nearing completion at MIT under the direction of Mr. Jay W. Forrester. The component research and development and the construction of the computer are being carried on under an Office of Naval Research contract.

Not counting access to the memory, addition time for two 16 binary-digit-numbers is 3 microseconds and multiplication time is between 14 and 22 microseconds. Average addition time, counting memory access, is 175 microseconds, and average multiplication time is 187 microseconds. It is hoped that these average times can be reduced to 48 and 60 microseconds, respectively.

A specially designed electrostatic storage tube, in which permanence of information is attained by use of a holding gun to provide a diffuse beam of low-velocity electrons, has been developed. The storage surface consists of a mosaic of conducting beryllium on mica. In addition, there is a read-write gun, a collector screen which controls the potential to which the storage spot charges, and a signal plate which is necessary for writing negative signals and reading out digits. At present a bank of 16 storage tubes, each storing 256 binary digits, has been installed along with the necessary circuits for transferring information to and from the memory in a parallel fashion. The final memory is expected to be composed of 32 tubes, each storing 1024 binary digits.

In order to decrease the number of errors occurring during operation of the computer, a marginal checking arrangement for detecting deteriorating components has been worked out. In this scheme, voltages are varied in large circuit groups, inducing inferior parts to cause failure, while a test program detects and localizes the potential failure.

In a trial on a 400-tube prototype system, the application of this type of preventive maintenance for half an hour per day appears to have improved reliability 50 to 1. The equipment has made several runs of 3 weeks without computational error, which represents 2.5×10^{10} correct solutions to a simple test problem and about 10^{13} correct flip-flop reversals in 25 flip-flop circuits. The average run without error has been 11 days. A run of 45 days without error was made in early 1950. During this 45-day period, 12 tubes, 7 crystals, and 4 resistors were located during marginal checking periods and replaced because of low margins.

The arithmetic element, central control, and 32 registers of test storage have been operating as a system since September 1949. Although the computer will at first be operated with minimum terminal equipment, including 2 Eastman Kodak Reader Recorder units, perforated paper tape, and typewriters, it is planned that additional photographic film units and Raytheon magnetic tape auxiliary memory units will be added in the near future.

About half of the computer's time during 1951 is to be devoted to a control problem of interest both to the Air Force and the Navy, while the rest of the time will be used on problems of scientific interest.

3.12 The Instititue for Numercial Analysis Computer

In October of 1948 the Applied Mathematics Executive Council of the National Bureau of Standards decided that a high-speed electronic digital calculator should be built at the Institute for Numerical Analysis, a field station of the National Bureau of Standards located at the University of California at Los Angeles. It was decided to construct this computer using approximately $200,000 of the funds which had previously been transferred from the Air Materiel Command of the United States Air Force to the National Applied Mathematics Laboratories of the National Bureau of Standards. The decision was that this machine should be built as quickly as possible and that it should have an electrostatic memory.

Work on this project was begun in January 1949 under the direction of Dr. Harry Huskey. A parallel arithmetic unit was designed, and a 3-digit prototype was built and tested. A contract was let for the production of the 80 chassis required in the arithmetic unit; they have been delivered and have proved satisfactory.

After a Williams tube memory prototype was built and tested and a production model cathode-ray tube chassis constructed, a contract was let for the production of 45 of these units which have now been delivered and incorporated into the computer. A dot-dash method of storing information is being used, and initially only 256 such spots are stored on each tube. This means that the size of the high-speed memory will, at first, be 256 words. Although all the testing has been done on the basis of storing 512 spots in such an area, experiments indicate that as many as 1024 spots could be stored on the tube without changing the relative dot spacing. It was thought that limiting the memory to 256 words in the beginning would simplify the process of "de-bugging" the machine and would make it possible to do useful computation sooner than otherwise.

A 4-5 address command system has been developed. There are 13 commands; eight of these are distinct basic commands, and the other five, termed special commands, are variations of certain of the eight. Three of the addresses refer to the addresses of the operands and to the address of the result. The fourth address provides a method of automatically detecting overflow in the addition and subtraction operations and of doing the proper thing about it. In the case of the special commands, the fourth address in the command will determine the source of the next command. However, normally the next command to be obeyed is determined by a number in the counter in the control unit (the fifth address). The compare command gives a method of transferring control; the result of the subtraction done in the compare operation is put back into the memory in a place determined by the third address. This makes possible a tally, or counting operation, using the compare command.

A system of abbreviated coding has been devised wherein coded commands are used, which are interpreted by a so-called interpretation routine in the computer. This makes it possible, after having prepared the appropriate subroutines, to code the solution of 125, or fewer, simultaneous linear equations by the use of not more than 30 abbreviated commands.

For the purpose of giving a permanently attached auxiliary storage which will hold approximately 8000 words, a magnetic drum has been incorporated in the design of the computer. It will serve as a temporary storage of numbers involved in the computation and also as a semipermanent storage of routines needed in the solution of problems.

Various means of input and output will be attached to the machine. In the beginning, these will consist of an IBM electromatic typewriter and a standard teletype-tape unit. Later, Dr. Huskey expects to attach one or more magnetic-tape units as additional input-output devices for the computer.

The fabrication of all the units of the computer has been completed, and all chassis have been individually checked and operated satisfactorily. Checking and testing of the computer as a whole is being conducted at present, and simple routines, making use of the entire system, have been run on the machine.

3.13 NRL Computer (NAREC)

An automatic electronic digital computer, operating in the parallel mode, has been designed at the Naval Research Laboratory. Prototypes of most of the critical components have been built and are now being checked. A tentative completion date has been set for the summer of 1952.

Employing about 2000 vacuum-tube envelopes and 6000 crystal diodes, this computer will possess 1024 words of electrostatic Williams tube memory and 2048 words of magnetic drum memory. The word length is 45 binary digits. Magnetic tape will be used for the input-output medium.

In order to check transfers and other operations, a built-in functional checking system will be employed. In the electronic circuits, in place of the standard flip flops, a modified Schmidt type trigger circuit is being used. Research on preliminary models of the adder indicates that, not counting memory access time, two 45 binary digit numbers can be added in from 3 to 4 microseconds. Access to the Williams tube memory is expected to be on the order of 10 microseconds.

The control has been designed to employ a one-address order code.

3.14 Aiken Mark III Calculator

The Mark III computer was designed and built by Professor Howard Aiken at Harvard under a contract with the Bureau of Ordnance. It was demonstrated at a combined Harvard Symposium and meeting of the Association for Computing Machinery in September 1949. After further testing, it was moved to the Naval Proving Ground, Dahlgren, Virginia, early in 1950 and should be available for solution of problems in the fall of that year.

The basic considerations in the design were: (1) Meeting the needs of the operators, which included simplification of coding, and (2) attaining greater reliability. Experience with Mark I showed that analysis of the problem and coding in most cases required considerably more time than the machine solution of the problem even on a relatively slow computer. To make coding easier a "coding machine" was constructed. A keyboard was arranged, by means of which instructions could be put on magnetic tape and later transferred to a sequence drum. These instructions are in a form familiar to the coder: A + B = C, A ÷ C = D, etc. The coder can thus call for complicated sequences permanently stored on the drum by pressing 3 buttons.

In order to carry out the various functions of the computer, which include ability to set up the results in a form ready for duplication for publication purposes, about 4000 tubes and 1500 relays are required.

The memory unit comprises 8 magnetic drums of 8-in. diameter on 4 shafts geared together, which rotate at 7200 rpm. Each decimal digit is represented in 4-element coded form by presence or absence of a magnetized point in each of 4 channels, a channel being a circle around the drum. Ten 16-decimal digit numbers together with their algebraic signs are recorded in 4 channels around the drum. The channels are designated as 2′, 4, 2, and 1, the digits having the following coded form:

CHANNEL DIGITS	2′	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1

Five, for example, is represented by pulses in the 2′, 2, and 1 channels (2 + 0 + 2 + 1 = 5). The advantage of this system is that the nines' complement of a number can be indicated by reversing the coding.

The memory is divided into two parts, one, having a capacity of about 350 numbers, being immediately accessible to the computer unit. This part of the memory is equipped with two magnetic heads per channel, each head capable of reading and writing. The slower part of the memory is about 1600 channels wide (storing 4000 16-decimal digit numbers) and has one magnetic head per channel. By use of a relay selection unit, capable of selecting a set of 4 channels, blocks of 20 16-decimal digit numbers can be read from the low- to high-speed memory or 10 from the high- to low-speed memory in 20 milliseconds or less.

Of the approximately 350 numbers in the fast memory, about 150 are constants, some of which are used in the evaluation by interpolation of the elementary functions $1/x$, $1/\sqrt{x}$, cos x, $\tan^{-1}x$, $\log_{10}x$, and 10^x, from which most of the other elementary functions may also be obtained. Thus, there are an additional 200 storage positions available in the high-speed memory for intermediate results.

Of the 4000 instructions in the sequence drum, about 650 are now used for fixed sequences such as division, which can be called for by the coder by pushing the proper buttons on the coding machine. About a quarter of the drum is expected to be used in this way as new routines are shown to be valuable. The use of the drum allows considerable flexibility over sequence tapes. The arithmetic unit contains a serial adder in which numbers to be added are transferred, digit by digit, to the adder, and the sum, digit by digit, from the adder to the storage unit. Although the adder can add two 16-digit numbers in a few hundred microseconds, it requires about 4 milliseconds to read the number from the memory. A multiplier is built into the computer, but division is by an iterative process. Total addition time averages about 4 milliseconds and total multiplication time about 12.5 milliseconds.

3.15 The General Electric Digital Computer

An electronic computer having a magnetic drum memory was designed and is under development under the supervision of B. R. Lester in the laboratory of the General Electric Company, Syracuse, New York. Among the design considerations, accuracy and reliable operation were foremost, and only proven principles are utilized. Operation and maintenance procedures are simplified. Unitized construction, employing about 16 basic circuits as plug-in assemblies, is used to aid design, speed maintenance, and provide for adding future improvements.

By employing a magnetic drum 24 inches in diameter and 30 inches long, 4000 numbers and instructions are stored in 100 tracks around the drum, 40 numbers per track. The drum, which rotates at 1800 rpm, is constructed of aluminum with a magnetic coating. The pulse repetition rate is approximately 48 kilocycles, clock pulses being generated on the drum. The input-output unit employs magnetic tapes which are operated at such a speed that approximately 25 words per second are read into or out of the machine. For number representation a basic word length of 8 decimal digits with a fixed decimal point or a basic word length of 6 decimal digits with a floating point is used. The range of the latter system is 10^{-9} to 10^{9}.

A parallel arithmetic unit is employed, and control signals to this unit are based on a 200-kilocycle oscillator in the control unit. Operation times, not including access to the memory, are as follows:

Operation	Fixed-Point Operation	Floating-Point Operation
Addition	15 Microseconds	350 Microseconds
Subtraction	15 Microseconds	350 Microseconds
Multiplication	450 Microseconds	490 Microseconds
Division	450 Microseconds	530 Microseconds

On the average, time for completion of one operation including access time is equal to the time of one revolution of the memory.

One of the major achievements has been the reduction of the tube complement to less than 1000 vacuum tubes, made possible by use of crystal diodes and careful circuit design. Approximately 4000 diodes are employed.

3.16 California Digital Computer (CALDIC)

The work on this project is under the direction of Professor Paul L. Morton, University of California, Berkeley, and is partially supported by the Office of Naval Research. In the design of this computer the guiding principles are simplification of circuits, minimization of maintenance, and attainment of a control system which provides for ease of coding.

Drawings and design information will be available to small research centers which need an installation on the spot so that scientists can follow the course of their problems through the computer and change the coding in the light of intermediate results.

In line with these objectives, a magnetic drum memory has been completed, having a storage capacity of 10,000 ten-decimal digit numbers, to any one of which access can be gained in a maximum of about 16 milliseconds. This capacity was provided not only to accommodate large problems, but also to simplify the input-output equipment and the coding. Large function tables can be stored if desired, and the need for special skill in programming subroutines is reduced.

The drum, which is 26 inches long and 8.6 inches in diameter, is driven at a speed of 3600 rpm. In order that the drum need not be accurately regulated in speed, there is a timing track around the drum for supplying pulses to control all computer operations. Cell density is approximately 100 binary digits per linear inch. Four channel circuits transmit the binary code for each decimal digit in parallel; the 10 decimal digits of a number and its associated sign are transmitted serially as the drum rotates. In all, 200 simply designed magnetic heads are employed, which are adjusted to have a clearance of between 1 and 2 thousandths of an inch from

the drum surface. The amplifiers for the memory contain only 3 miniature tubes per recording head: One a reading amplifier, one a writing amplifier, and the third a gate tube.

A copy of the drum has been obtained by Dr. Huskey's group at the Institute for Numerical Analysis as an auxiliary memory to the Williams electrostatic storage tubes.

The high-speed, low-cost input and output devices required by the objectives of the CALDIC will be standard electric tape-punching typewriters. The input typewriter will make a punched paper tape which will be read photoelectrically into the computer at approximately 50 words per second. It will therefore require about 3 minutes to load the drum completely. The print-out order will cause a tape to be punched, and page copy will be obtained by running the output tape through a tape-reading electric typewriter.

Use is made of single address orders which are normally taken in sequence from the memory. To take care of conditional subprogramming and also overflow of the accumulator, a special order is used. It is inserted in the program whereever an overflow is possible and is disregarded unless the overflow occurs. If an overflow does occur, the contents of the order counter are changed as specified in this order. Discrimination is achieved by testing for overflow instead of by testing for negative numbers as in some computers. Another instruction used in subprogramming provides for clearing the address part of an order and adding the remainder to the contents of the accumulator. This corresponds to the "extract" order of some computers.

Average addition or multiplication time is approximately 32 milliseconds.

A good part of the construction has been completed and the computer is to be assembled by the end of 1950.

3.17 MADDIDA

MADDIDA (Magnetic Drum Digital Differential Analyzer) was developed by Northrop Aircraft, Inc., in connection with an Air Force contract. A prototype of this computer, which employs a magnetic drum memory combined with a computing unit, has been completed and has demonstrated its ability to handle the ordinary and partial differential equations and the sets of simultaneous linear equations solvable on analog differential analyzers.

Essentially, integration of the equation $z = \int y dx$ is performed by means of repeated addition. However, the block diagram of the solution of a differential equation or system of equations on the MADDIDA is similar to that on an analog differential analyzer.

Four channels of data are recorded on the magnetic drum of MADDIDA. Three of these, called the R, Y, and Z channels, are used for temporary storage, being played back, erased, altered, and recorded each time the drum revolves. The fourth channel is permanently recorded and contains 1300 equally spaced clock pulses. In some cases, the clock pulses are used as the dx pulses.

The integrating device consists of 2 accumulators, Y and R, and a transfer device, T. When a dx pulse is applied to T, y is added to R and the dz outputs are pulses representing overflows from R. Hence the rate of dz pulses overflowing out of R is proportional to y and to the rate of dx; $dz = k y\, dx$. Of course at any time, $y = y_0 + \sum_i dy_i$.

The R and Y channels which hold the data for the R and Y accumulators are each divided into 22 sections, giving the equivalent of 22 integrators. The first half of each section (pulses 1 through 24) is used to hold permanent coded information, which controls the transfer of data from one "integrator" to another. For the purpose of storing numerical data for R and Y, which is operated on once for each revolution of the drum, the second half of each section (the remainder of the 48 digits) is used. The code half of each section prepares the computing center for the operations that are to be performed on the data which follows.

Two attractive features of the MADDIDA are its compactness and accuracy. The present prototype occupies a floor area of only 7-1/2 sq ft and has an accuracy of 22 binary (6 decimal) digits.

A new model is under construction having the capacity of a 44-integrator differential analyzer and 29 binary digit accuracy. The tube complement is expected to be less than 100. A 12-channel input for arbitrary functions and a 12-channel output are being provided.

3.18 Engineering Research Associates Computers

During the past few years, Engineering Research Associates have developed and built several special-purpose computing machines employing magnetic drum storage. The drum system developed by ERA combines the following properties: (1) Alterability of stored data; (2) nonvolatility, or extremely high stability, of the stored data; (3) rapid random access to any storage position, even when the quantity of stored information is large; and (4) large storage capacity in relatively compact form. With a storage density of 80 binary digits per inch, the scanning speed is 1600 inches per second corresponding to the value of 128 digital cells per millisecond. Since there can be 16 tracks per axial inch along the drum, the storage capacity on the surface is 1280 digits per square inch. Each magnetic drum head, which is a specially designed form of electromagnet with an elongated ring shaped core, has a clearance of 0.002 inch from the drum surface. This surface is a smooth sprayed-on coating of magnetic iron oxide protected by a thin over-coating of lacquer.

A typical storage system produced by ERA stores 8192 numbers of 30 binary digits each. In addition to 120 storage tracks, there are 11 angular index tracks and one timing track. The angular index tracks contain the 2048 11-digit angular indices. The timing track serves as a source of timing pulses for precisely marking the instant at which the drum passes through each of its 2048 discrete angular positions. One of these timing pulses, selected on the basis of the desired angular index, denotes the instant at which the desired storage position is available for reading or writing.

This time selection is performed by an 11-fold coincidence detector which continuously compares the desired 11-digit angular index in an "Address Register" with the outputs of the circuits which read the angular index tracks. As long as the scanned angular indices do not match the desired angular index, timing pulses cannot get through the coincidence detector. When the drum passes through the angular position at which a match occurs, a single time pulse is delivered to the storage control circuits for triggering of the appropriate writing or reading operations.

4. COMPUTERS OUTSIDE THE UNITED STATES

4.1 EDSAC - Computing Machine, Cambridge University, England

The EDSAC (Electronic Delay Storage Automatic Calculator), built at Cambridge by Dr. M. V. Wilkes and Mr. W. Renwick, is a serial type binary electronic digital computer, employing mercury delay lines. There are 32 lines, each storing 16 words of 35 binary digits each, including the algebraic sign. Provision is made for splitting a word into 2 shorter numbers. Since the computer operates at a 1/2-megacycle pulse repetition rate, access time to the memory varies from 200 to 1200 microseconds. In the delay lines the pulses are used to modulate a 13.5-megacycle-per-second carrier.

Addition requires about 1.5 milliseconds and multiplication about 7 milliseconds. Multiplication is a built-in process but division and square rooting are carried out by iterative processes.

In order to simplify the preparation of programs on the EDSAC and to reduce errors in programming, Dr. Wilkes has built up a large library of subroutines. These are incorporated into the program of a complicated problem by modifying some of the orders according to their location in the main program at the time the routines are taken into the machine.

Since its completion last June, problems of scientific interest have been solved on the EDSAC concerned with the following topics:

Tabulation of the function,

$$\frac{1}{\Gamma(x+iy)} \qquad \begin{aligned} x &= -0.50\ (0.01)\ 0.50 \\ y &= 0(0.01)\ 1.00, \end{aligned}$$

oscillation of a pendulum in a submarine (gravity survey), ray tracing in an electron lens, solution of a potential equation by the Liebmann process, serial correlation, group and phase velocity of electromagnetic waves in the ionosphere, a matrix problem connected with the wave theory of a molecule, and solution of a differential equation arising in the theory of the constitution of a star.

4.2 Manchester University Digital Computer

Designed and built under the direction of Professor F. C. Williams and Dr. T. Kilburn at Manchester University, England, this computer employs ordinary cathode-ray tubes for high-speed storage and a magnetic drum phased with the fundamental time cycle as auxiliary storage. Input to the machine is teletype tape, and output is on an electronic typewriter.

Professor M. H. A. Newman and Dr. A. M. Turing, who will be the eventual users of the machine, are responsible for logical design and programming. A single address order code is used. Among the ordinary operations are included: Addition, subtraction, multiplication, and the logical processes "and," "or," "not either." Addition takes approximately 1.8 milliseconds and multiplication a maximum time of 40 milliseconds.

Of the 8 cathode-ray tubes employed in the computer, 4 are used for the high-speed memory, which has a total capacity of 128 words, each tube storing 32 words of 40 binary digits. Information is stored serially in binary form as dots and dashes on the cathode-ray tube screen. Since the fundamental digit period is 10 microseconds, it requires 400 microseconds to scan a line. This added to the 50 microseconds required for retrace time makes a total of 450 microseconds per line. In order to assure permanence of information, provision is made for sequential reading and restoring of the lines of information in between times at which access is made to the memory. Thus 900 microseconds is required for an "action" period plus a "scan" period. In the action period, an order involving access to the memory is carried out and in the scan period a line of storage is restored.

A fifth cathode-ray tube, used for control purposes, has 2 lines of 40 digits each, one called CI (control information) and the other PI (present information). The CI line defines the next order to be obeyed. Ordinarily one is added to the contents of CI as each order is carried so that orders in the memory are called for sequentially. However, the contents of CI can be altered by a conditional or branch order, which adds any specified number to the contents of CI to shift control to any desired location in the memory. After the contents of CI are altered by automatically adding one (or some other number if the previous order was a branch order), the order in the memory location specified by CI is transferred to line PI in the control storage tube.

The order in PI is then carried out and the process is repeated. An order consists of 3 parts: One "B" digit, an address specifying a location in the memory, and the code for the one of 32 operations which is to be performed.

Another cathode-ray tube called the "B" box is used to provide a way of changing orders particularly to facilitate the use of subroutines. This tube stores 2 lines designated as B_0 and B_1. If the B digit of an order is 0, the contents of B_0 (normally 0) are added to the information in PI, which contains the order to be obeyed. If the B digit is one, then the contents of B_1 are added to PI. Hence the programmer is able to modify an order just before its execution, yet leaving it unchanged in the memory. As an example of the flexibility afforded by the use of the B-box, a sequence of operations to be performed on various sets of data need be programmed only once (containing the addresses of the first set of data) and the addresses of later sets of data can be inserted without changing the stored orders by inserting a line in B_1.

Two cathode-ray tubes are associated with the arithmetic units, one in the addition and subtraction circuits and the other in the multiplier. In addition to the 8 cathode-ray tubes, about 1400 other vacuum tubes are required in the computer.

A second computer, essentially similar to the one just described, is being built for the University by the Ferranti Company, Ltd. Somewhat larger and more carefully engineered than the present one, it will be housed in a separate building which is now under construction.

The cathode-ray tube storage comprises 16 cathode-ray tubes, each holding 64 numbers of 20 binary digits arranged in 2 parallel rasters, or 82 numbers of 40 binary digits (making a total of 512 numbers of 40 binary digits each). Order length is generally 20 binary digits and number length may be 20, 40, or 80 binary digits. The magnetic drum memory will store about 655,000 digits. Since the B-box has demonstrated considerable usefulness for modifying orders, it has been increased from 2 to 8 forty-digit lines. Multiplication time is 3.36 milliseconds or 2.16 milliseconds when the multiplicand is already in the accumulator.

This computer should be completed by the fall of 1950, after which it is planned to start construction on another computer of the same type.

4.3 Digital Computer, Telecommunication Research Establishment, Malvern, England

This computer, whose design and construction is under the direction of Dr. A. Uttley, is a high-speed parallel-mode binary digital electronic computer employing an F. C. Williams cathode-ray tube memory. The electrostatic storage is supplemented by a magnetic drum, coupled to which is a 2048-tooth phonic reel acting as a master clock for the electronic circuits. Input will be on teletype tape and output on an electromatic typewriter.

An interesting feature of the computer is the use of a 2-wire system in which a positive pulse on one wire indicates unity, while a positive pulse on the other indicates zero. The absence of pulses on both wires, or the presence of 2 positive pulses, indicates an error or machine failure.

The orders, which are specified in a single address code, make up a 20-digit word, which is the standard word length for the computer. Addition takes about 40 microseconds and multiplication, which is programmed, takes about 800 microseconds.

When finished the TRE computer will be mounted on about 10 racks in a sort of Faraday cage which will screen out interference from nearby radar equipment. Four-digit equipment groups will be mounted on a single rack. There will be altogether approximately 2000 tubes, most of which are double triodes, and the power consumption will be about 10 kw. The computer will probably be finished in about 16 months, although it may be possible to do some preliminary numerical problems before then.

4.4 Digital Computers at Birkbeck College

Dr. A. D. Booth of Birkbeck College, University of London, is building three digital computers, ARC, SEC, and APEXC. The ARC, automatic relay computer, as completed, has a magnetic drum memory of 22 tracks around the drum, on each of which can be stored 256 binary digits. One track is used for clock pulses, a second for algebraic sign, and the remaining ones for 20-binary-digit numbers. The operating air gap between the pickup head and the drum surface is about 0.001 inch, and the input current to the single turn coil is about 15 amps. Punched teletype tape is the input-output medium.

Addition, subtraction, multiplication, and division are all automatic operations. The time required for an addition or subtraction is about 20 milliseconds. Multiplication and division take about 1 second, including access time to the magnetic drum memory. Reading out and into the memory takes a maximum of 20 milliseconds and a mean time of 10 milliseconds.

The ARC, which has been completed and operated in several simple problems such as tabulation of prime numbers and factorization of large numbers, is now temporarily dismantled.

Eventually it will be reassembled and the magnetic drum memory will be replaced by several cross-bar type memory units, each storing 32 words of 21 binary digits. Each unit will be 12 x 8 x 2 inches, the total storage capacity remaining unchanged.

The SEC, simple electronic computer, which is an all-electronic calculator operating in the parallel mode, is nearing completion. Since the present design calls for 182 vacuum tubes and since there certainly will be less than 300 in the final model, the total space occupied by the computer is very small.

The magnetic drum memory originally designed for the automatic relay computer is being used. Adding, subtracting, or transferring numbers in the arithmetic unit takes 1.5 milliseconds and multiplication requires a mean time of 0.2 seconds. Division is not automatic but is performed using an iterative procedure based on the sequence $X_{n+1} = X_n(2-aX_n)$, which converges to 1/a. A teletype machine will be used for input and output.

The APEXC, an all-purpose electronic X-ray computer and an evolution of the SEC, will employ about 800 vacuum tubes and will use a magnetic drum memory 5 inches in diameter and 7 inches long rotating at 60,000 rpm. It will store 1024 numbers of 32 binary digits. Reading out and into the memory will require 1 millisecond. Addition and subtraction, not considering memory access, will take 30 microseconds; multiplication and division will take about 1 millisecond. Input will be on magnetic tape and output will be on a magnetic-tape typewriter. Dr. Booth expects that the APEXC will be completed by the summer of 1951. Although it is a general-purpose digital computer, it will probably be used initially for making crystallographic computations.

4.5 The ACE (Automatic Computing Engine)

The National Physical Laboratory, Teddington, England, has completed the construction of a prototype computer under the direction of J. H. Wilkinson and F. M. Colebrook. This machine, a serial device with a mercury delay memory, operates at a pulse repetition rate of 1 megacycle per second.

In each of 8 delay lines are stored 32 words of 32 binary digits each, making a total of 256 words. Each instruction, which is expressed in a 2-address code, is one word in length. Input and output is by means of punched-card equipment. Numbers and instructions may be inserted in pure binary or in coded decimal form; in the latter case they are converted into the binary representation by the machine.

The final model is expected to have a memory of 5000-6000 10-decimal-digit (= 40 binary digits) numbers.

4.6 The Elliott Brothers Computers

The Elliott Brothers Research Laboratories, Boreham Wood (Herts.), England, are engaged in computer developments and have produced several new techniques of considerable interest in the construction of digital computer subassemblies. They are now manufacturing in quantity add/subtract plates and double 1-digit-delay plates which may be connected for use as binary adders or subtractors. Multipliers can be built up from these same elements. It is understood that a prototype computer using these components is nearing completion.

The computer subassemblies consist of thin glass (or hard resin) plates about 4 x 6 inches. Silver circuits are printed on the plates and are fired at a high temperature after application. Cross connections between front and back of the plates are made by rivets through holes drilled in the plates. Wafer condensers, very tiny paper-wound coils, subminiature pentodes and triodes, and germanium crystal rectifiers are connected to the rivets. Carbons resistors are also printed in the circuit and are accurately adjusted up to the final value by scratching with a razor blade. The technique of preparing the printed circuit plates is now so highly developed that Elliott Brothers are able to design and supply special-purpose digital computers for industrial or scientific use.

4.7 Computers in Sweden

The BARK, (Binar Automatisk Rela-Kalykylator), was built by the Swedish State Board of Computing Machinery by a group headed by Dr. Conny Palm. The construction was carried out in the laboratories of the Swedish Telegraph Administration.

The machine, which contains about 5200 relays, has a storage capacity of 50 relay registers and 100 constant registers. Numbers are represented in the form $2^p \times q$, where p is a 6-digit binary number with algebraic sign and q a 24-digit binary fraction with algebraic sign. Thus, 32 binary digits are required for the representation of one number. In the decimal system this corresponds to a range between 10^{-19} and 10^{+19} and an accuracy slightly better than 7 decimal digits.

For programming, essentially a 4-address order code is employed. The instructions are set up by means of plugged connections, which provide for a total of 840 operations to be programmed at one time, forming either one or several independent sequences. Conditional instructions are obtained by the use of "selectors" or relay pyramid circuits; these are units which direct the control to one or another of the plugged connections (order codes) depending on the sign or on the last digit (2-way pyramid) or on the last 6 digits (64-way pyramid) of a number in a special control register. There are 125 two-way and four 64-way pyramids. Each 64-way pyramid can be broken into two 32-way ones, or into four 16-way ones, etc. This arrangement greatly reduces the number of instructions needed in a program.

The BARK has performed satisfactorily during continuous runs up to 8 hours at a speed at about 200 milliseconds per addition and 300 milliseconds per multiplication. It is hoped that the speeds of operation, which are easily adjusted by the use of potentiometers, can be somewhat increased. Also being planned is a large-scale electronic digital computer which will probably employ electrostatic storage tubes.

4.8 Other Projects

A relay computer called the Sequence-Controlled Calculator is under construction by the Royal Aircraft Establishment, Farnsborough. The design of the computer was worked out by E. J. Petherick and Drs. Hollingdale and Eggink. In Holland, a relay computer having both relay and magnetic drum storage is being built at the Mathematisch Centrum at Amsterdam. The designers were A. van Wijngaardn and B. J. Loopstra. A relay computer construction project is under way at the Delft Technical University, Delft, Holland, with A. C. S. van Heel and W. L. van der Poel responsible for the design.

Other computer projects are located at the Laboratoire de Calcul Mechanique, Centre National de la Recherche, Paris, under the direction of L. Couffignal; at the University of Sidney, Australia, under D. M. Meyers; and at the University of Toronto, Canada, under J. Katz, A. G. Ratz, and C. C. Gottlieb. The Australia computer employs a mercury acoustic memory of 32 lines, each storing 32 twenty-binary-digit numbers.

A relay type digital computer will be built soon in the Institute for Practical Mathematics, Technische Hochschule, Darmstadt, by Professor A. Walther and his group. Preliminary models of the adding and multiplying circuits have alreay been constructed. A digital computer project is also under way at the University of Göttingen under the direction of Dr. K. Beyerle of the Max Planck Institut fur Instrumentenkunde.

During the war Dr. Konrad Zuse built a relay digital computer having a very compact type of mechanical storage. He has moved the computer to Neukirchen/Kreis Hunfeld, Germany, where he has organized a small calculating machine firm, the Konrad Zuse Gesellschaft. The memory of the computer has been increased from 16 cells holding 32 binary digits each to 4 times that number. Dr. Zuse is perfecting a new type of mechanical storage which he hopes will eventually replace the older memory.

In July 1950, a sequence-controlled computer was installed at the Institute for Applied Mathematics of the Swiss Federal Institute of Technology at Zurich. It was constructed by

Konrad Zuse in consultation with A. Speiser and E. Stiefel of the Institute. The machine is a relay computer with 2200 telephone relays and 20 stepswitches and with mechanical storage elements developed by Zuse. It operates in the binary system with floating binary point, the binary exponent ranging from 63 to -64. Translation from decimal to binary system and vice versa is fully automatic. Numbers are fed in by means of a 10-keyboard or punched tape (35-mm movie film), whereas the output goes to a typewriter or to punched tape, which can be fed back to the tape reading unit, thus providing external storage. A total of 64 numbers can be stored with an access time of 1/2 second, but the users hope to increase storage capacity to 1024 numbers. The time for addition and subtraction is approximately 1 second, for multiplication 2.5, for division and square root 6 seconds, all including transfers from and to storage. To skip an order takes 0.2 second.

At Oslo, Norway, a relay computer similar to the BARK, but using 2000 Zuse mechanical storage cells each storing 16 words of 16 binary digits, is being built under the direction of Prof. H. Solberg. The computer will be used to solve problems in dynamical meteorology.

5. OUTLOOK FOR THE FUTURE

As can be seen from the preceeding discussion, most of the computers thus far developed are "Goliaths" with complicated circuits containing thousands of separate components. Much of this complication is due to the fact that the builder of digital equipment has aimed at making it almost completely general-purpose, often with many frills to make certain processes possible or easier for the coder. One of the future developments to be expected, then, is a line of simplified special purpose computers for control applications, or for the solution of a particular problem type where the work load warrants it. In this respect, MADDIDA is a harbinger of the future.

As well as the trend toward special-purpose machines, we can expect simplification of present general-purpose computers, possibly by using the same component for more than one function and by development of components especially for computer use. Also, in the future we can look toward improvement in reliability, reduction in space and power requirements, and reduction in cost.

* * *

APPENDIX

A. DIGITAL COMPUTER ORGANIZATION AND CONTROL

A.1 COMPARISON OF DIGITAL AND ANALOG COMPUTERS

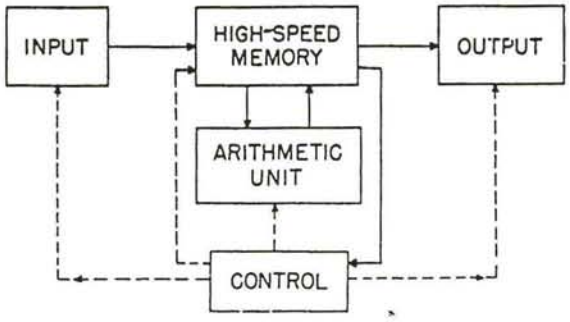
Computers may be of the continuous (also known as analog) or of the digital type. In the former, numbers are represented by proportional physical quantities such as lengths, angular positions of rods, electrical voltages or currents, and forces. The well-known slide rule and the differential analyzer are examples. The digital type represents numbers by elements which vary only in discontinuous or discrete steps, for example, the gear teeth in a desk adding machine or the stages of an electronic counter. Its operation involves step-by-step numerical analysis methods, whereby the solution of a problem is reduced to fundamental arithmetic processes. It should be noted that a single device may combine both digital and analog features.

Accuracy in the continuous type computer depends on the structure and precision of the parts which represent the sizes of the numbers. This accuracy is therefore limited by human capacity in constructing flawless mechanisms and by effects of temperature, air pressure, humidity, and age on such mechanisms. In contrast to this, the accuracy of the digital computer is limited only by space for more and more of the same parts.

One of the important features of presently planned computers of the digital type is their flexibility of logical control. Full use is made of the principle that the machine can set itself up at each step of the operation. Problems enter the machine in coded form through the use of punched cards, tape, or some other prepared medium. Changes in equations representing particular problems can be readily accommodated as well as changes to entirely different types of scientific problems. After coding a general class of differential equations, for example, it would take very little time (one-half to a few hours) to code a particular problem. Moreover, problems and routines of frequent usefulness can be coded on paper tapes or magnetic tapes or wires and stored in libraries for future use. Subroutines that are used in many problems need only be coded once and then inserted at the proper place in each problem.

Speed of calculation of the separate steps in electronic digital computation can be made to be extremely great, although many steps are required. However, it seems probable that the over-all speed of the digital computer can be made considerably greater than that of the analog type. This feature is important in the case of some control applications and in the case of problems too complicated to be attempted by slower machines.

A.2 ORGANIZATION OF A DIGITAL COMPUTER



NOTE: The input and output units may be used also as an auxiliary low speed memory device. They are sometimes combined into a single unit.

Figure 1 - Digital computer, schematic

A.2.1 General

The trend in the last few years has therefore been toward digital calculating machines. A brief explanation of the function and interrelation of the essential components is then in order. A glance at Figure 1 shows these to be an arithmetic (computer) unit, a control, an internal high-speed memory and an input and output unit. The input and output also serve as an auxiliary low-speed memory.

A.2.2 The Arithmetic Unit

The arithmetic unit under guidance of the control performs the fundamental arithmetic processes. An adder is the fundamental component, subtraction being accomplished by adding the complement (essentially equivalent to the negative) of the number. A multiplier almost always and a divider frequently are built into this unit, although multiplication and division can, when it is desired, be programmed by a coded series of orders involving addition and subtraction. Due to the complexity of the added equipment involved, it is usually considered preferable to code rather than build in such processes as interpolation, extracting a root, calculating a logarithm, or computing trigonometric functions.

A.2.3 High-Speed Memory

The high-speed memory stores the numbers and usually the orders to be employed in the problem in a form readily accessible to the arithmetic unit. The existing machines employ either mechanical counters or relays—and their electronic equivalents, decade rings and flip flops—or electrostatic storage tubes, acoustic delay lines, or magnetic media. The latter forms of storage are employed in an essentially binary manner, "0" and "1" being distinguished by opposite states in the memory medium.

In electrostatic storage, information is in the form of charged spots on the dielectric surface of a cathode-ray tube screen. A positive charge might represent a "1" and lack of charge or a negative charge represent a "0." The charge can be put on by directing a beam of the proper electron velocity to the point in question. With proper switching and circuitry the information can be read off by a beam of a different velocity. One advantage of this type of memory is that a parallel procedure for getting words (numbers or orders) out of and into the memory is possible. A battery of 40 tubes each having 1000- to 5000-binary-digit capacity might be operated in parallel. The separate digits of a 40-binary-digit word would be stored in corresponding places in each of the 40 tubes. To read this word from the memory, the electron beams of all the tubes would be directed to these corresponding points (position 100 in each tube, for example) by a switching arrangement.

One form of acoustic storage consists of a number of stainless steel tanks containing mercury and equipped with quartz crystals at each end. Electric pulses, representing binary digital information, are impressed on one of the crystals and are converted by it into acoustical pulses in the mercury. These pulses then travel through the tank with the velocity of sound and are reconverted into electrical pulses by the crystals at the other end. After being corrected for loss of amplitude and definition, the pulses are fed back to the input of the tank. The information can then be recirculated continuously through the tank without loss of synchronism or definition, thus forming a memory device storing a number of pulses corresponding to the length of time required for an acoustical disturbance to travel the length of the tank. A disadvantage is that if only one word is stored in each tank, the switching problem becomes very complicated, while if several words are stored in each, then the computer must wait till the desired word arrives at the output end during its circulation of the tank.

Magnetic storage is ordinarily in the form of magnetized areas on a rotating drum or on a moving wire or tape. Signal strength is greater than in the electrostatic or acoustic devices, but speed of access is limited by mechanical limitations imposed by moving parts.

A.2.4 The Auxiliary Memory

Magnetic wire and tapes are suitable for an auxiliary memory to store intermediate results and to introduce data into and receive data from the internal high-speed memory. Photographic film is also being investigated for this purpose by Eastman Kodak under an ONR contract.

A.2.5 The Control

The control keeps the various units of a computer in synchronism; controls operation of the arithmetic unit, the high-speed memory, and the auxiliary memory; and causes shifts of information between high-speed memory and the arithmetic unit as required by the problem. The control can automatically recognize and act on such orders as to carry out arithmetic operations; to move the auxiliary memory medium; to read, erase, or write information on the auxiliary memory; to extract certain parts of a word; and to choose one of two alternate sequences depending on which of two numbers is the greater.

One way to design the control is to have it start at a point in the high-speed memory and execute sequentially the orders found in successive memory locations. According to another school of thought, each order should include the memory location of the next order to be carried out. The former method requires less circuitry and tends to make more efficient use of the memory space, but the latter is thought to simplify the coding process.

An important feature of the dynamic sequencing and control of the EDVAC and IAS types of computers is the fact that orders and numbers are stored in the high-speed memory in a similar form. This makes it possible to provide means for modifying orders stored in the memory by arithmetic operations on these orders. Thus, a flexibility of control not available in previous machines is achieved.

A simple coding example will illustrate this feature. Suppose it is desired to calculate the values of the polynomial $4x^2 + 7x + 9$ for $x = 2, 3, 4, 5 \ldots$ and to store the results in the memory. We shall assume that the control starts at position "1" in the memory and carries out the order found there, then proceeds to position "2," carries out that order, and so on in sequence until it reaches an order that breaks off the sequence.

We shall need the following orders:

A(m) - add number found at position "m" in the memory[3] to the number already in the accumulator, and leave the result in the accumulator. A(137) then means - add the number found in memory location 137 into the accumulator. The accumulator is a register in the arithmetic unit for temporary storage of a result of an arithmetic process.

M(m) - multiply the number in memory position "m" by the number in the accumulator and leave result in the accumulator.

C(m) - transfer the number in the accumulator to memory position "m," leaving "0" in the accumulator.

T(m) - instead of continuing in sequence, perform the order found in memory position "m" and proceed from there in sequence.

The orders and numbers to be used in this problem, let us say, will be stored on magnetic wire and transferred to the internal memory positions in sequence.

We store the quantities which we will need in memory locations 31 to 35 as shown in Table A.

TABLE A

Memory Locations	Number Stored
31	x (2 stored at start of problem)
32	1
33	4
34	7
35	9

[3]When a number is read from the memory into the accumulator for addition, multiplication, etc., the number is not erased from the memory. Reading a number into the memory erases what is already there.

We rewrite the problem, putting the polynomial into a simpler form for coding purposes: $x(4x+7) +9$.

The orders required are shown in Table B. Orders 1 through 6 are used to evaluate the polynomial for a value of x, and orders 7 through 13 are required to modify x and the first 6 orders and return the control to memory location 1 to evaluate the polynomial for the next and succeeding values of x.

In Table B the first column shows the memory location of the order. This means that the first order to be obeyed by the computer will be stored in memory location 1, the second order in memory location 2, etc. In the second column of Table B, we find the instructions to be obeyed. The result of each order is indicated in the last column. For example, the order in memory location 1 is A 31. Looking back at the list of orders previously given, we see that A(m) means add number in memory location "m" (memory location 31 in this case) into the accumulator. From Table A, we see that x is stored in memory location 31. Hence, as a result of the order A 31, we have x in the accumulator; the first time we evaluate the polynomial, 2 will be in the accumulator; the next time we evaluate the polynomial, 3 will be in the accumulator; and so on.

As another example, we will take the order in memory location 10 of Table B, which is A 6. Looking back in the same table to memory location 6, we see that it contains the order C 50. Order A 6 means then that we are adding the order C 50 into the accumulator where it can be modified by arithmetic processes.

TABLE B

Memory Location of Order	Order	Result of Order
1	A 31	Add number in memory location 31 into accumulator. The quantity x, which is 2 in the first case, is now in accumulator.
2	M 33	Multiply number in accumulator, which is x, by number in memory position 33, which is 4; result: (4x) in accumulator.
3	A 34	4x + 7 now in accumulator, since we have added 7 from memory location 34 to 4x, which was already in the accumulator as a result of the previous order.
4	M 31	x(4x+7) now in accumulator.
5	A 35	x(4x+7) +9 now in accumulator.
6	C 50	The value of the polynomial, x(4x+7) +9, for x = 2 in first case, now in memory location 50; accumulator cleared.
7	A 31	x in accumulator (x = 2 in first case).
8	A 32	1 is added to x; x now will = 3 for the second case, 4 for the third case, etc.
9	C 31	x back in memory location 31; accumulator cleared. Since we have added 1 to the present value of x and put it back in location 31, we are now ready to use it to evaluate the polynomial for the next value of x.
10	A 6	Order in memory location 6, which is C 50, now in accumulator for modification. (See memory location 6 in this group of orders.)
11	A 32	1 is added to order. (Order will read C 51 to point out memory location for result when x = 3, C 52 when x = 4, etc., so that the results of the evaluation of the polynomial for successive values of x will go into successive memory locations.
12	C 6	Order C 51 now back in memory location 6.
13	T 1	Control now returned to memory location 1. The polynomial will be evaluated for x = 3 in second case, result stored in 51, orders modified; control then returned again to location 1; then polynomial evaluated for x = 4, result stored in 52, etc.

As coded above, the machine will continue evaluating the polynomial for successive values of x and placing the result in memory location 50 and successive locations until the memory is filled. Hence, to terminate this sequence of operations, when the highest desired value of x is reached the following conditional order is required:

R(m) - If the number in the accumulator is 0 or positive, continue to the next order in sequence. If the number in the accumulator is negative, shift the control to memory location "m" and perform the order found there and in succeeding memory locations, accumulator cleared.

Suppose that is is desired to evaluate the above polynomial for values of x up to x = 40 and then break off the sequence. We will store the number -41 in memory location 30. The order in memory location 13 above will not be used, and the following will be substituted:

Memory Location	Order	Result of Order
13	A 31	x was stored in memory location 31; hence value of x to be used in next evaluation of polynomial is in accumulator. Remember, as a result of order 8, x was increased by one.
14	A 30	-41 is added to value of x to be used next.
15	R 1	If x < /41/ , say 32, 32 + (-41) = -9, the number in the accumulator is negative and the control as a result of the present order goes back to memory location 1 and evaluates for x = 32. When we reach x = 41, 41-41 = 0 and the control goes on to order 16 to start a new problem.

It can be seen that a relatively small number of orders can suffice for evaluating a polynomial for x = 2, 3, 4...n. Without facility to modify orders, n times as many orders as are needed for one value of x would be required.

This code is called a one-address code because it refers to one memory location. M(a)(b)(c), which means multiply number in memory position (a) by number in memory position (b) and store the result in (c), is an example of an operation using a three-address code. A four-address code might be illustrated by M(a)(b)(c)(d), which says multiply the number in (a) by the number in (b), store the result in (c) and go to (d) for the next order. The choice among these various ways of designing the control will only be resolved as experience is gained in coding and solution of problems.

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