COMPUTER AUTOMATION

PDC 808 PROGRAMMED DIGITAL CONTROLLER T.M.

FEATURES OF THE PDC 808 PROGRAMMED DIGITAL CONTROLLER T.M.

- ☐ ECONOMY
- ☐ 4,096 WORD CORE MEMORY
- ☐ EXPANDABLE MEMORY, PROCESSOR AND I/O
- ☐ PARALLEL PROCESSING
- ☐ LARGE (73) INSTRUCTION SET
- ☐ MULTILEVEL INDIRECT ADDRESSING
- ☐ EIGHT HARDWARE REGISTERS
- ☐ EXTREMELY POWERFUL AND FLEXIBLE I/O SYSTEM EASILY INTERFACED
- ☐ TWO PRIORITY INTERRUPT LINES STANDARD
- ☐ ADDITIONAL PRIORITY INTERRUPT REQUEST LINE
- ☐ PARTY-LINE I/O BUS
- ☐ INTERFACES DIRECTLY TO DTL IC'S
- ☐ DTL AND TTL INTEGRATED CIRCUITS INCLUDING MSI
- ☐ PLUG-IN CORE STACKS
- ☐ COMPACT, 8¾" RACK MOUNTED
- ☐ PORTABLE, LESS THAN 30 LBS.
- ☐ LESS THAN 200 WATTS AC

GP COMPUTER PERFORMANCE

The PDC 808 eliminates expensive, inflexible special purpose logic systems. Designed for control and monitoring applications, the PDC 808 offers the power and flexibility of a general purpose computer at a price far less than special purpose hardware designs. An exceptionally large set of I/O instructions and a straight-foreward I/O interface philosophy make the PDC 808 easily adaptable to a broad range of control applications. For real time applications, the PDC 808 has two priority interrupt lines as a standard feature.

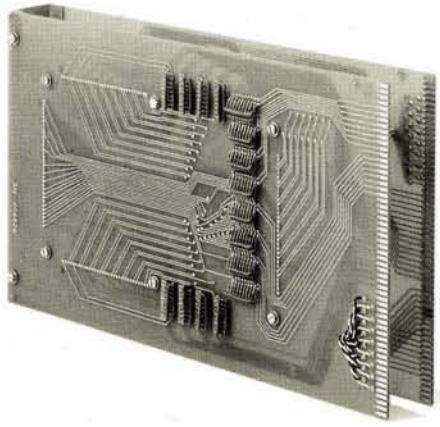
PROCESSOR

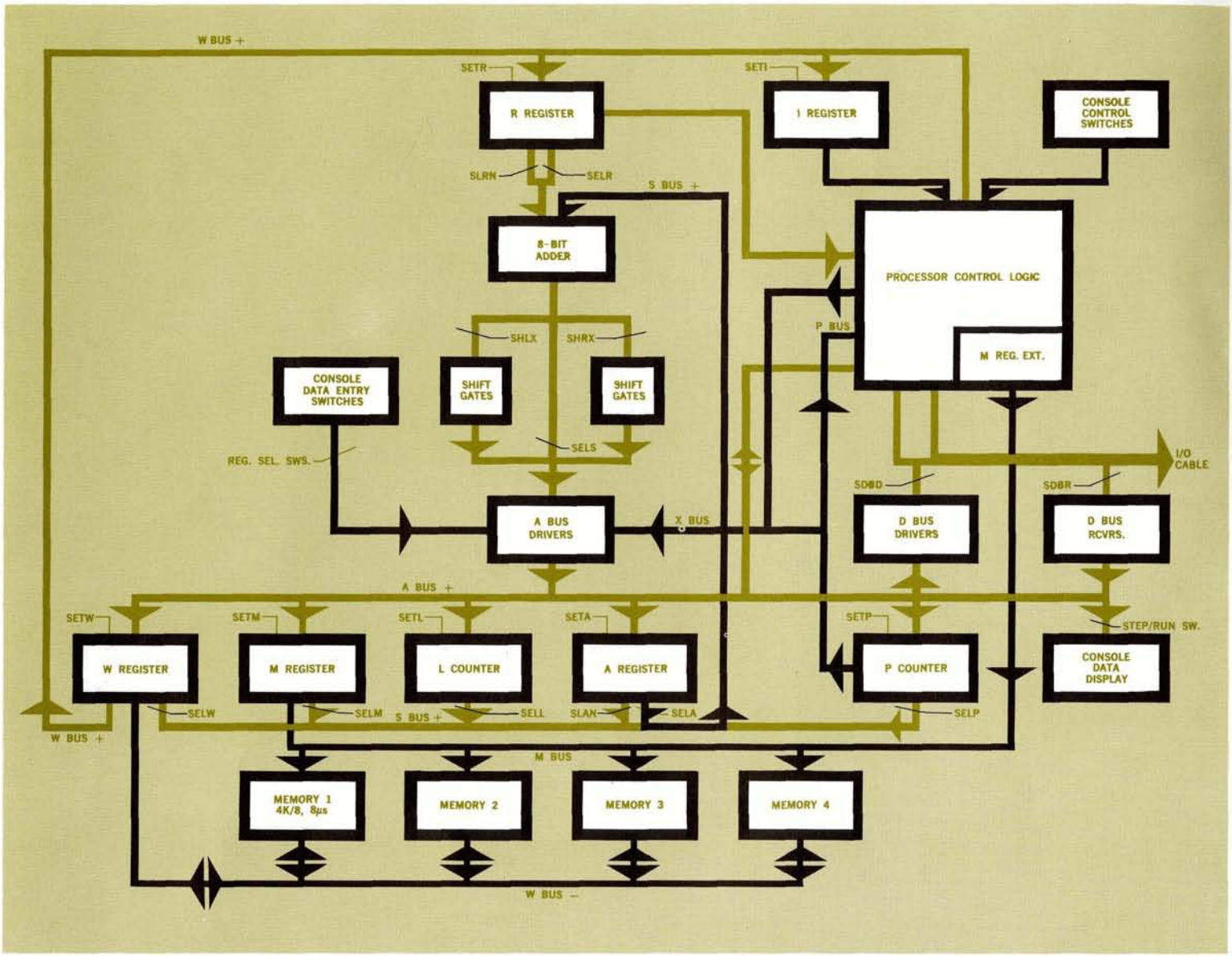
The PDC 808 has 73 standard instructions in four groups: Memory Reference, I/O, Register Change and Skip. The first two groups are double-word instructions. Register Change and Skip are single-word instructions. Parallel organization provides fast execution speeds. Eight hardware registers insure ease of programming and efficient memory utilization. Two priority interrupt lines and a third priority interrupt request line, are standard on the PDC 808. These can be expanded in groups of eight.

MEMORY

The PDC 808 uses a random access 3D core memory for mainframe storage. Full cycle time is eight microseconds. The core stacks are 4,096 word plug-in assemblies. The memory is expandable from 4,096 to 16,384 words. The mainframe can house 8,192 words. A standard feature of the PDC 808 is the block transfer into or out of memory, disturbing only the memory address and word registers without disturbing the program. In addition, the Direct Memory Access option provides the capability of capturing the memory completely for large block or single-word transfers at memory speeds.

Automatic Power Fail Sequence is offered as an option for those applications that require unattended operation.





PDC 808 ORGANIZATION

The PDC 808 is organized as a binary, parallel, single-address computer utilizing a random access core memory, eight hardware registers and a party-line I/O bus. Internal communication within the PDC 808 is via a number of major buses between registers, processor, memory, I/O and console.

A-Bus. Distributes the output of the eight-stage Adder to the W,M,L,P, and A registers, the console display, and the I/O Data Bus drivers.

S-Bus. Distributes the output of the W,M,L,P and A registers to the Adder.

M-Bus. Distributes the output of the memory address register to the memory modules.

W-Bus. One section of the W-Bus transfers data from the memory modules to the W register. Another section transfers the output of the W register to the R, I and ME registers.

Data transfers to or from the PDC 808 are handled in parallel form (8-bits) by transferring between the A-Bus and the D-Bus (in the I/O Cable).

The Processor Control Logic contains the necessary control functions to handle the bus interconnections, register selection and control, memory control and interrupts. The basic PDC 808 processor has a 73 instruction repertoire.

I/O

The I/O facility of the PDC 808 is extremely flexible. Thirteen I/O instructions provide the power and execution speeds to perform a broad range of control and monitoring tasks. Sense-and-Skip instructions can test for true or false response. Programmed transfer instructions can be combined with sense instructions to allow testing prior to transfer in a single instruction execution time.

The block transfer instructions allow up to eight 256-word blocks to be transferred into or out of memory under program control or under interrupt control. A pointer is automatically updated for each transfer.

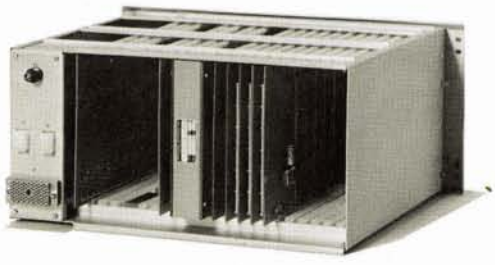
The PDC 808 Party-line I/O bus further enhances flexibility. Thirty-two device addresses are available. Eight functions can be coded at each address. I/O expansion does not require changes to the existing system. The electrical interface to the I/O bus is standard DTL integrated circuits. Five volt logic eliminates special circuits and power supply requirements.

INTERRUPTS

Interrupts are a standard feature of the PDC 808. Two priority interrupt lines as well as a priority interrupt request, are included to increase the I/O flexibility and provide real time capability beyond programmed I/O. Additional interrupt lines are available in groups of eight lines.

Each interrupt line has two unique memory locations assigned to it. Any PDC 808 instruction can be executed under interrupt control, but not all are practical as interrupt instructions. Jump-and-Save can be used as an interrupt instruction to allow an external stimulus to transfer program control and record where the program was when the interrupt occurred. The contents of the program counters are stored at the beginning of the subroutine entered by a Jump-and-Save instruction. The interrupts provided with Real Time Clock and Power Fail Sequencer options are in addition to the two standard interrupt lines.

The PDC 808 comes equipped with internal power sufficient for a 16,384-word memory and all the mainframe options. Only three voltages (+12, −12, +5) are used for simplicity and economy. The power supply is a physically separate package that mounts behind the mainframe. Total power consumption is less than 200 watts.



PERIPHERAL DEVICES

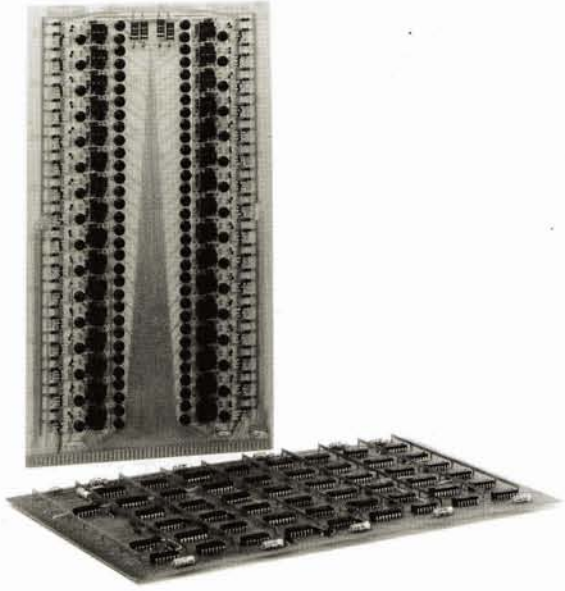
A broad range of peripheral equipment is offered with the PDC 808, including a disc memory, ASR 33 Teletype, high speed paper tape reader and punch, card reader, and magnetic tape units. In addition, I/O module options are available including a utility module with 6 sense lines, 6 external control lines, a gated input 8 bit channel and a buffered 8 bit output channel. Special interfaces to customer requirements are also available.

HARDWARE

Broad operating margins, easy maintenance and reliability (17,000 hours MTBF) are assured through conservative design. High noise immunity dual-in-line DTL and TTL integrated circuits are mounted on two-side printed circuit boards. A standard 7 11/32" x 13" plug-in board is used for all processor, I/O, option and memory electronics as well as the memory stack. Thus all sections of the PDC-808 can be removed for quick examination or replacement. The front panel snaps off for immediate access to all connector pins and the ELCO™ ground plane. The front ground plane, elevated power and ground bus bars on the boards, and adequate decoupling further insure rugged electrical margins.

SOFTWARE

As programming and maintenance aides, the PDC 808 comes with a software package that includes an assembler, maintenance programs for memory, processor, and I/O, and utility programs.



PDC 808 SPECIFICATIONS

TYPE

A digital, stored program, general purpose controller designed for on-line control and monitor applications. Utilizes magnetic core memory, parallel binary single address processing.

MEMORY

Magnetic core, 8 microseconds full cycle. Field expandable from 4096 words to 16,384 words in 4096-word modules without modifications. Optional Direct Memory Access bus allows the memory to be operated independently of processor. Plug-in 4,096 word core stacks.

ARITHMETIC

Parallel, binary, fixed point, 2's complement

WORD LENGTH

8 bits

SPEED

Add or Subtract	24 microseconds
Register Change	8 microseconds
Operate	8 microseconds
Input/Output from A Register	16 microseconds
Block Input/Output from Memory	32 microseconds

REGISTERS (hardware)

A-Register—accumulator, input/output 8 bits
M-Register—memory address register 8 bits
ME-Register—memory page address register 6 bits
L-Register—page location counter 8 bits
I-Register—instruction register 8 bits
R-Register—operand, instruction extension register 8 bits
P-Register—memory page counter 8 bits
W-Register—memory word register 8 bits

CONTROL

Five instruction types—73 instructions
Memory reference — 10
Input/Output — 13
Register change — 16
Control — 4
Skips — 30

Two addressing modes
Direct
Indirect-multilevel

INPUT/OUTPUT

Data transfer
Program control — single word to/from A register unconditional or conditioned on sense response; masked input to A register; automatic block transfer to/from memory; optional DMA channel, 125,000 words/sec.

Program sense and control
Eight sense or control conditions per instruction. Up to 64 external sense lines, and up to 64 external control lines, are available.

Interrupts
Basic interrupt capability includes 2 interrupt lines and a third interrupt request line. Expandable in groups of 8 lines. Individual line arm/disarm and group arm/disarm. Each interrupt has unique memory address.

PHYSICAL

Dimensions
Processor, memory, power supply, and console — 8¾ in. high, 19 in. wide, 22 in. deep.

Weight
Processor, 4K memory, and console — 13 lbs.
Power supply — 15 lbs.

Installation
Mainframe mounts on front rails of equipment cabinet; power supply mounts on rear rails of cabinet.

Construction
Modular, plug-in mainframe and peripheral options. Up to 16,384 words of core storage.

Environment
0°C to 45°C; 0 to 90% relative humidity.

LOGIC SIGNALS

Integrated circuits (DTL and TTL), 5 volt logic. 3 volt transmission busses, standard 5 volt DTL integrated circuits used for interfacing.

SOFTWARE

Package includes assembler, utility, and maintenance.

COMPUTER AUTOMATION, INC.

895 WEST 16TH STREET
NEWPORT BEACH, CALIFORNIA 92660

TELEPHONE (714) 642-9630

PDC 808 CONTROLLER INSTRUCTION SET

MEMORY REFERENCE—Two Word Instructions

Mnemonic	Description	Cycles
ADD	Add to A Register	3
SUB	Subtract from A Register	3
ANA	AND to A	3
IØR	Inclusive OR to A	3
LDA	Load A Register	3
STA	Store A Register	3
IMS	Increment Memory, Skip on Zero	3
JMP	Jump Unconditional	2
JST	Jump and Store L and P counters	4
IMA	Interchange Memory and A	3

SKIPS (If True Test)—One Word Instructions

Mnemonic	Description	Cycles
IFT +	Skip if A is Positive	1
IFT N	Skip if A is Non-zero	1
IFT R	Skip if Overflow is Reset	1
IFT 1	Skip if Sense Switch (SS) is Set	1
IFT +.N	Skip if A is Positive & Non-zero	1
IFT +.R	Skip if A is Positive & ØV Reset	1
IFT +.1	Skip if A is Positive & SS is Set	1
IFT N.R	Skip if A is Non-Zero & ØV Reset	1
IFT N.1	Skip if A is Non-zero & SS is Set	1
IFT R.1	Skip if ØV is Reset & SS is Set	1
IFT +.N.R	Skip if A Positive & Non-zero & ØV Reset	1
IFT +.N.1	Skip if A Positive & Non-zero & SS is Set	1
IFT +.R.1	Skip if A Positive & ØV is Reset & SS is Set	1
IFT N.R.1	Skip if A is Non-zero & ØV Reset & SS Set	1
IFT +.N.R.1	Skip if A is Positive & Non-zero & ØV Reset & SS Set	1
IFT −	Skip if A is Negative	1
IFT Z	Skip if A is Zero	1
IFT S	Skip if ØV is Set	1
IFT O	Skip if Sense Switch is Reset	1
IFT −,Z	Skip if A is Negative or Zero	1
IFT −,S	Skip if A is Negative or ØV is Set	1
IFT −,O	Skip if A is Negative or SS is Reset	1
IFT Z,S	Skip if A is Zero or ØV is Set	1
IFT Z,O	Skip if A is Zero or SS is Reset	1
IFT S,O	Skip if ØV is Set or SS is Reset	1
IFT −,Z,S	Skip if A is Negative or Zero or ØV Set	1
IFT −,S,O	Skip if A is Negative or ØV Set or SS Reset	1
IFT −,Z,O	Skip if A is Negative or Zero or SS Reset	1
IFT Z,S,O	Skip if A is Zero or ØV Set or SS Reset	1
IFT −,Z,S,O	Skip if A is Negative or Zero or ØV Set or SS Reset	1

REGISTER CHANGE—One Word Instructions

Mnemonic	Description		Cycles
ARC D	Decrement A Register	A − 1 → A	1
ARC I	Increment A Register	A + 1 → A	1
ARC 1	Load A with 1	O + 1 → A	1
ARC −1	Load A with −1	O − 1 → A	1
ARC C	Complement A (1's)	O − (A + 1) → A	1
ARC N	Negate A (2's)	O − A → A	1
ARC Z	Clear A (load A with zero)	O + O → A	1
ØRC S	Set Overflow		1
ØRC R	Reset Overflow		1
ØRC C	Complement Overflow		1

SHIFTS—One Word Instructions

Mnemonic	Description	Cycles
SHF L	Logical Shift Left	1
SHF R	Logical Shift Right	1
SHF <	Arithmetic Shift Left	1
SHF >	Arithmetic Shift Right	1
SHF (	Rotate Left	1
SHF)	Rotate Right	1

INPUT/OUTPUT—Two Word Instructions

Mnemonic	Description	Cycles
EXC	External Control	2
SSR	Sense and Skip on Response	2
SSN	Sense and Skip on No Response	2
ØTA	Output from A Register (unconditionally)	2
ØTZ	Output Zero	2
ØAS	Output A and Skip on Response	2
ØZS	Output Zero and Skip on Response	2
INA	Input to A Register (unconditionally)	2
MIA	Masked Input to A Register (unconditionally)	2
IAS	Input to A & Skip on Response	2
MIS	Masked Input to A & Skip on Response	2
INB	Input Block to Memory	4
ØTB	Output Block from Memory	4

CONTROL—One Word Instructions

Mnemonic	Description	Cycles
NØP	No Operation	1
HLT	Halt	1
EIN	Enable Interrupts	1
DIN	Disable Interrupts	1

Notes: 1. Indirect addressing adds 2 cycles per level.
2. In the cases where more than one operation - defining character appears in the address field ordering of these characters is irrelevant.