SCIENTIFIC DATA SYSTEMS

SDS 900 SERIES COMPUTERS

General characteristics

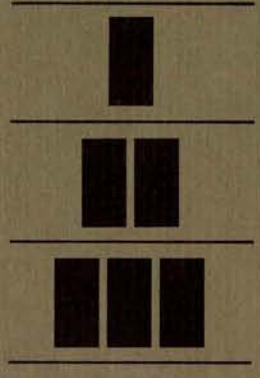
SDS 900 Series computers—the SDS 910, SDS 920, and SDS 930—are a family of compatible general purpose digital computers designed for scientific and engineering computation and for real-time systems integration. High internal computing speeds, powerful instruction lists, and a large number of efficient input/output systems insure maximum speed and flexibility for a wide variety of applications. A large library of programs is available, including FORTRAN II; an Assembly system; a monitor-controlled Meta-Assembler; and a complete library of subroutines, diagnostics, and utility routines. SDS 900 Series computers provide more answers at lower cost, with greater reliability, than any other general purpose digital computers on the market today.

Each of the three 900 Series computers meets a different range of requirements, but all three are compatible logically, electrically, and mechanically. Programs written for any 900 Series computer can be run without modification on any other computer in the series. All 900 Series peripheral equipment can be used without modification on all three machines.

This complete compatibility offers the user many advantages. For example, several different 900 Series computers can be installed within a given facility. If any one of these is unavailable, any of the others can be used directly, without reprogramming; or a particular program can be compiled on one computer and then run on another. As requirements increase, 900 Series computers can be interchanged without changing the interfacing between the computer and the associated equipment.

All SDS 900 Series computers have the following characteristics:

- 24-bit word plus a parity bit
- 48-bit word for floating point arithmetic
- Binary, 2's complement arithmetic
- Single address instructions, that allow multi-level indexing and indirect addressing
- Complete program compatibility among all SDS 900 Series computers
- Automatic parity checking for all input/output operations and memory transfers
- Automatic subroutine handling with Programmed Operators
- Console display of all programmable registers, with extensive manual controls
- Comprehensive software package that includes FORTRAN II, MONARCH Monitor system, Symbolic Assemblers, and a complete set of arithmetic subroutines and utility programs
- A completely automatic priority interrupt system independent of normal input/output channels. Up to 1024 priority levels that can be individually enabled and disabled under program control
- Parallel Word input/output operations completely independent of normal buffered input/output channels
- Low power requirements
- Unique reliability through the use of all-silicon semi-conductors and an efficient logical design which radically reduces the component count



Individual characteristics

SDS 910—$41,000 with 2048 words of memory and Paper Tape Reader.

Basic core memory of 2048 words, expandable to 16,384 words, all directly addressable. Buffered I/O rates to 250,000 characters per second.

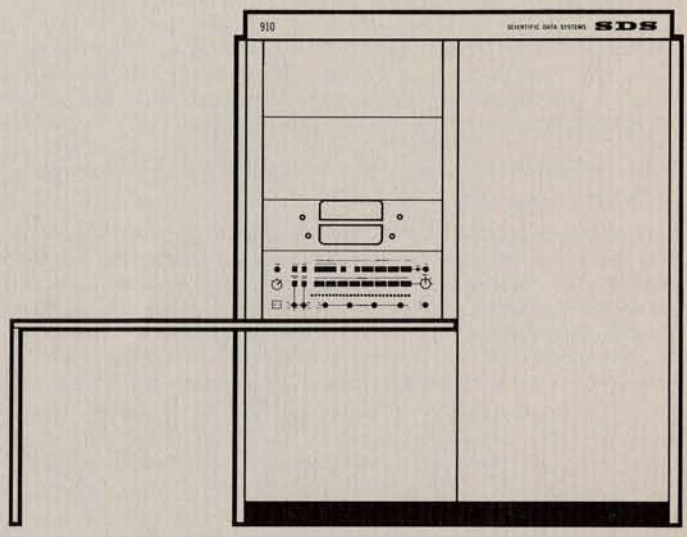
Execution times, including all accesses and indexing.

Fixed Point

16 μsec.	Add
248 μsec.	Multiply

Floating Point

(24-bit fraction, 9-bit exponent)		(39-bit fraction, 9-bit exponent)
440 μsec.	Add	832 μsec.
504 μsec.	Multiply	1696 μsec.



SDS 920—$83,000 with 4096 words of memory, Input/Output Typewriter, and Paper Tape Reader, Spooler, and Punch.

Basic core memory of 4096 words, expandable to 16,384 words, all directly addressable. Buffered I/O rates to 250,000 characters per second.

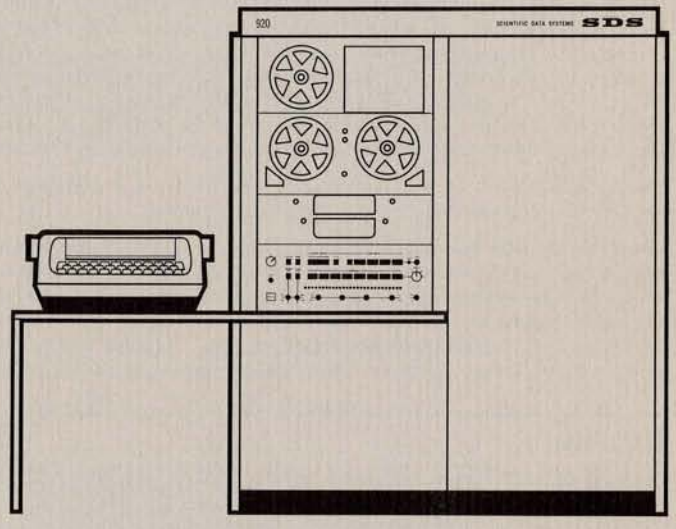
Execution times, including all accesses and indexing:

Fixed Point

16 μsec.	Add
32 μsec.	Multiply

Floating Point

(24-bit fraction, 9-bit exponent)		(39-bit fraction, 9-bit exponent)
292 μsec.	Add	368 μsec.
248 μsec.	Multiply	600 μsec.



SDS 930—$103,000 with 4096 words of memory, Control Console, 6-bit Time Multiplexed Communication Channel, and Input/Output Typewriter.

Basic core memory of 4096 words, expandable to 32,768 words, all directly addressable. Up to eight buffered I/O channels with rates to 2,000,000 characters per second. Input/Output simultaneous with computation, using an independent memory bank.

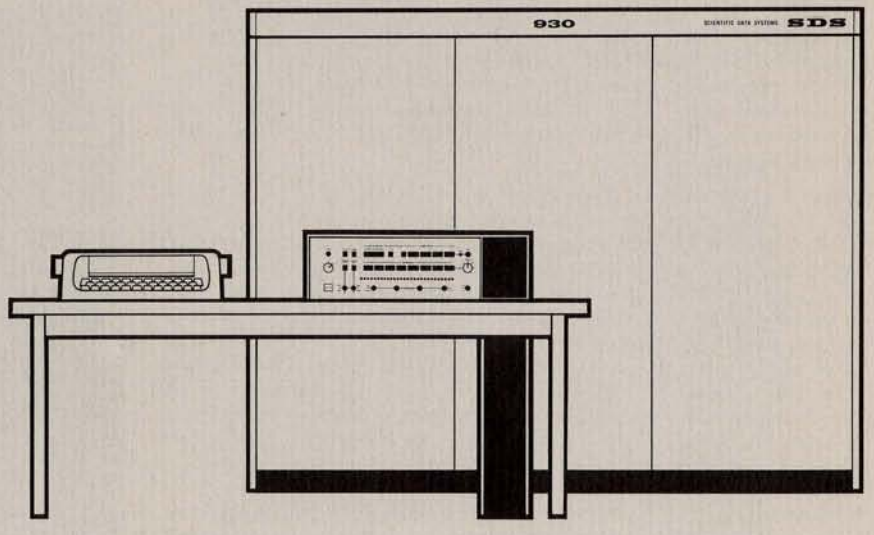
Execution times, including all accesses and indexing:

Fixed Point

3.85 μsec.	Add
7.7 μsec.	Multiply
19.25 μsec.	Divide

Floating Point

(24-bit fraction, 9-bit exponent)		(39-bit fraction, 9-bit exponent)
31 μsec.	Add	91 μsec.
59 μsec.	Multiply	152 μsec.
81 μsec.	Divide	162 μsec.



SDS 900 Series input/output

SDS 900 Series computers have unusually fast and flexible input/output capabilities that permit the user to take full advantage of high internal computing speeds. The various input/output systems are designed so that 900 Series computers can be integrated into systems with a minimum of special hardware and programming. All 900 Series computers have the same types of input/output operation and use the same input/output devices. Programs written for the 910 or 920 will operate on any 900 Series machine; the SDS 930 has certain extended capabilities.

Data can be processed by 900 Series computers in the form of characters, words, or single bits. These three types of I/O plus a comprehensive priority interrupt system permit a virtually unlimited number and variety of peripheral devices to be used.

SDS 910 and 920

Buffered Input/Output: The SDS 910 and SDS 920 include as standard equipment a character-oriented, buffered I/O channel, the W Buffer, which processes 6-bit plus parity bit (IBM format) characters at rates up to 62,500 characters per second under program control. Parity generation and detection and word assembly and disassembly are automatic. Input/Output is time-multiplexed with computation, interrupting the main program each time a new word is to be loaded or unloaded from memory.

An optional Memory Interlace system operates in conjunction with the buffer to provide direct input/output communication with the core memory, without program intervention, at rates up to 62,500 characters per second. This system contains storage for the address of the first word and the number of words to be processed by the I/O operation. After the last word is processed, an interrupt is activated. Two memory cycles are required for each word transferred.

A second, optional channel, the Y Buffer, is available for applications that require simultaneous operation of two channels. It is identical to the W Buffer except that the character register can contain from 6 to 24 bits plus a parity bit. Using both buffers the computer can read a gapless magnetic tape and simultaneously write an IBM format tape. The Y Buffer operates with or without interlace and is capable of transfer rates up to 62,500 characters per second. An extended version of the Y Buffer is available that allows transfer rates up to 250,000 characters per second.

The three following types of input/output operation are completely independent of the I/O Buffers and are standard equipment.

Word Parallel I/O: Two standard instructions permit the input/output of a 24-bit word under program control. The PARALLEL INPUT (PIN) instruction places the information from 24 input lines into a specified memory location without disturbing the contents of any arithmetic register. The PARALLEL OUTPUT (POT) instruction places the information contained in a specified memory location onto 24 output lines. These instructions can be modified by indexing and/or indirect addressing for efficient parallel input/output of blocks of information. Control signals are provided which synchronize all operations. Note that the Word Parallel I/O system is independent of and in addition to the Buffered I/O system, so that the two can be operated simultaneously.

Single Bit Control and Sense: Two instructions provide for single bit, ON/OFF control signals. The first, EOM, transmits a control signal and a 15-bit address to an external connector. The second, SKS, selects an external line and skips as a function of the state of that line. Up to 16,000 different control signals can be transmitted, or up to 16,000 input signals can be sensed.

Priority Interrupt: The priority interrupt system of the 910 and 920 provides up to 1024 channels of interrupt, each with a unique priority and address in memory. Most of the functions of the interrupt system are provided by hardware in order to minimize the programming required to use the system. The number identifying a given channel indicates its priority and the position in memory to which the program jumps when the channel is activated. This results in an extremely fast response time because the program does not have to determine the appropriate response to an interrupt and choose the proper subroutine entry. If a given interrupt has been activated, the activation of a higher priority channel causes the program to jump to the address specified by that channel. When the higher priority has been processed, the program returns to the point in the lower priority processing at which the second interrupt occurred. If a lower priority channel is activated, this event is remembered and the interrupt is processed after the higher order processing is completed. This insures that the most important program is always running. The entire priority interrupt system can be enabled or disabled under program control if a given sequence of instructions is to be protected from interruption. Individual interrupts can be selectively armed or disarmed under program control to permit dynamic re-allocation of priorities as the program runs.

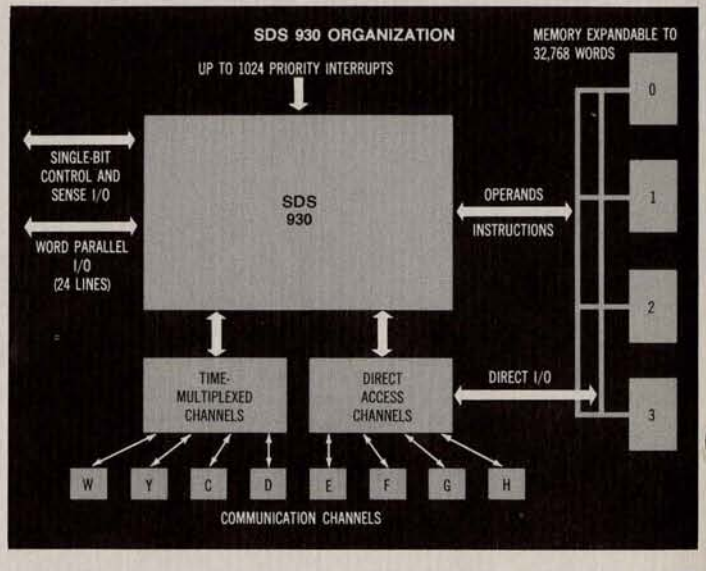
SDS 930

The SDS 930 I/O system includes all of the I/O facilities of the SDS 910 and 920, so that both programming and equipment are fully compatible. However the SDS 930 has additional Buffered I/O capabilitity: up to eight channels as opposed to the two (W and Y) of the 910/920. Of these eight, four may be Time Multiplexed Channels and four may be Direct Access Channels.

Time Multiplexed Channels: One of these is standard equipment with the SDS 930. It is a 6-bit character channel, analogous to the W Buffer on the SDS 910 and SDS 920, and is capable of transfer rates in excess of 250,000 characters per second. Three additional Time Multiplexed Channels can be added to the SDS 930. These channels, like the Y Buffer, can be extended to 12 or 24 bits. Memory interlace is standard with all Time Multiplexed Channels.

Direct Access Channels: These channels provide for higher speed operation. As shown in the diagram, a separate path to the memory is provided so that computation is not interrupted if the address of the I/O information refers to a memory bank other than the one being used by the program. I/O operations, in this case, do not use any of the computer time available to the program proper. If the program and I/O operation access the same memory bank no overlapping occurs, and the I/O operation utilizes a single cycle of the memory for the transferral of information. Direct Access Channels operate either upon words or characters at the option of the programmer. In all other respects, the two types of Buffered I/O channels are identical. Up to four Direct Access Channels are available, each capable of data transmission in excess of 2,000,000 characters (500,000 words) per second.

In some applications, it is efficient for I/O operations to be controlled by an external system rather than by the computer. To meet this requirement, a Direct Memory Access connection is available for the SDS 930, which provides for accepting, from an external source, memory control addresses for the information to be stored into or read from memory. This feature is available as an option with any SDS 930 and is provided at no extra charge with a Direct Access Channel.



Programming

SDS 900 Series computers have numerous hardware features which greatly enhance both the ease and power of machine language programming. These include multi-level indexing and/or indirect addressing, one-cycle inter-register transfers, and automatic interpretation of non-machine instructions. The latter feature is enabled through Programmed Operators (interpret instructions), which automatically initiate any one of 64 subroutines that may vary from time to time. Through Programmed Operators, complete program compatibility exists among all 900 Series Computers.

To exploit this wide spectrum of 900 Series hardware capability, SDS offers a comprehensive, modular software capability. From the basic Utility Programming System, HELP, to the powerful, batch-oriented Monitor, MONARCH, SDS provides a software/hardware balance with built-in growth potential. A large library of programs covering a variety of real-time applications and mathematical functions (such as matrix inversion) are available to the 900 Series user. The components of the standard 900 Series software package include:

HELP: The HELP Utility Programming System aids the small-machine user in the checkout and operation of machine language programs. HELP is completely modular so that the programmer need load only applicable parts. The entire HELP system can be loaded in less than 1800 memory locations.

SYMBOL: This two-pass assembly program provides for input of symbolic programs from typewriter, paper tape, cards, or magnetic tape. In addition to translating standard 900 Series instruction mnemonics and symbolic expressions, SYMBOL recognizes a variety of generative and non-generative directives that aid the user in coding and debugging his programs. Compatible with other 900 Series software components, SYMBOL also includes the capability to assemble machine-language FORTRAN subroutines.

META-SYMBOL: This advanced symbolic processor brings compiler-level capability to the machine-language programmer. A superset of SYMBOL, the META-SYMBOL language includes general expressions, which may consist of one or more (list) items combined by arithmetic and/or Boolean operators. META-SYMBOL also has Function and Procedure capability, which permits the programmer to code in a high level, machine-independent language. Operationally, the assembler consists of an Encoder and a Translator. The Encoder compresses the input language to a fraction of its original size before it is processed by the Translator. The Translator allows source language modification with optional recovery of the resultant updated source code.

FORTRAN: SDS FORTRAN II represents a major breakthrough in the field of automatic programming. Using recursive techniques, SDS FORTRAN combines great speed, flexibility, and efficient object code, even in SDS computer systems with only 4096 words of memory. Although it features multi-level n-dimensional subscripting, mixed mode expressions, and "backward" DO-loops, the compiler occupies only 2500 memory locations. It allows over 300 variables, labels, etc., and compiles more than 200 statements per minute. Where possible, complete syntactic generality is permitted, with the result that the SDS FORTRAN language is a superset of most FORTRAN languages, even large-scale ones.

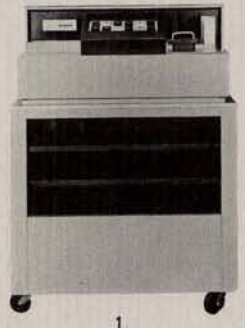
MONARCH: The 900 Series monitor is a batch-oriented operating system that provides large-scale processing power to the 900 Series user. The system requires two magnetic tape units, one of which is devoted to the system; MONARCH, META-SYMBOL, FORTRAN, plus library and utility programs provided with the system or added by the user. MONARCH operates under typewriter or card control and allows for batched assemblies, compilations and executions.

Users' Group: All SDS users are eligible to join the SDS Users' Group. The group provides a meeting ground for its many active members, in addition to a vehicle for program review and exchange.

SDS 900 Series peripheral equipment

A wide range of compatible peripheral equipment is available for use with SDS 900 Series computers. Each unit is controlled by its own coupling electronics and uses the built-in buffering system of the computers. Since interfacing is not required, peripheral devices can be used without modification with different 900 Series computers. Equipment available includes:

Paper Tape I/O Equipment
High and low speed Card Readers
High and low speed Card Punches
High and low speed Line Printers
Multi-density, high and low speed Magnetic Tape Units
Magnetic Drums
Magnetic Discs
Digital Plotters
Display Scopes
MAGPAK Magnetic Tape System



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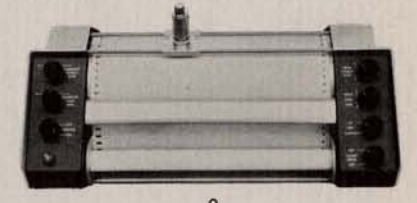

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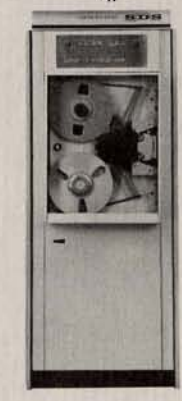
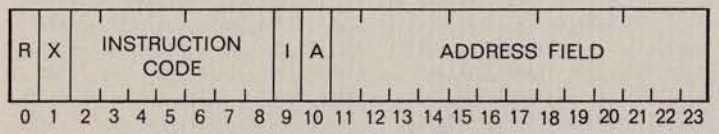


1. **Card Reader,** SDS Model 9151, 200 Cards/min.
2. **Digital Plotter,** SDS Model 9175, 300 increments per second, with an increment size of 0.01 inch.
3. **Line Printer,** SDS Model 91740, 300 lines/min., 132 characters/line, 64 printable characters.
4. **Magnetic Tape Unit,** SDS Model 92453, 96 Kc, 66.7 Kc, and 24 Kc character transfer rates, with recording density of 800, 556, and 200 bits per inch respectively.

SDS 900 Series instruction format

This instruction word format for SDS 900 Series computers is:



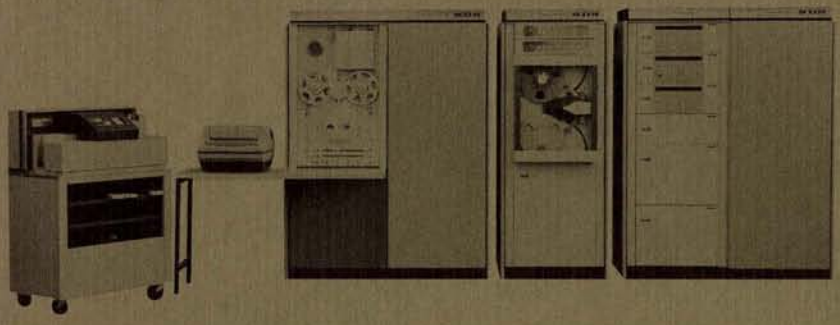
Bit Position	Function
0	**Relative Address Bit**—A "one" in this position causes the standard loading programs to add the assigned instruction location to the address field contents prior to actual storage. This bit position is not sensed by central processor decoding logic.
1	**Index Register Bit**—A "one" in this position causes the contents of positions 10-23 of the index register to be added to the address portion of the instruction prior to execution.
2-8	**Instruction Code**—The contents of these bit positions determine the operation to be performed. Bit position 2 is used with Programmed Operators and is considered a part of the "tag" field (0-2).
9	**Indirect Address Bit**—A "one" in this position causes the computer to interpret the contents of positions 10-23 (possibly modified by indexing) as the address of the memory location where the effective address of the instruction may be found. A "zero" causes the contents of positions 10-23 (possibly modified by indexing) to be interpreted as the effective address of the instruction.
10-23	**Address**—The contents of these positions normally determine the memory address referenced by the instruction code. With the SDS 930, bit position 10 contains the Memory Extension Bit that controls addressing above location 8,191.

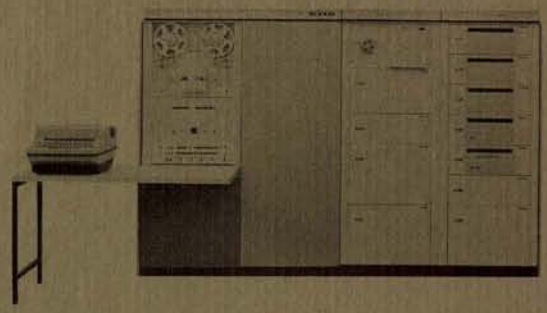
SDS 900 SERIES INSTRUCTION LIST

	Instruction	SDS 910 1 cycle = 8 μsec.	SDS 920 1 cycle = 8 μsec.	SDS 930 1 cycle = 1.925 μsec.
	LOAD-STORE			
LDA	LOAD A	2	2	2
STA	STORE A	3	3	3
LDB	LOAD B	2	2	2
STB	STORE B	3	3	3
LDX	LOAD INDEX	2	2	2
STX	STORE INDEX	3	3	3
XMA	EXCHANGE M AND A		3	3
	ARITHMETIC			
ADD	ADD M to A	2	2	2
ADC	ADD WITH CARRY		2	2
ADM	ADD A to M		3	3
MIN	MEMORY INCREMENT	3	3	3
SUB	SUBTRACT M FROM A	2	2	2
SUC	SUBTRACT WITH CARRY		2	2
MUL	MULTIPLY		4	4
MUS	MULTIPLY STEP	2		
DIV	DIVIDE		28	10
DIS	DIVIDE STEP	2		
	BRANCH-SKIP			
BRU	BRANCH UNCONDITIONALLY	1	1	1
BRX	INCREMENT INDEX AND BRANCH	1,2	1,2	1,2
BRM	MARK PLACE AND BRANCH	2	2	2
BRR	RETURN BRANCH	2	2	2
SKS	SKIP IF SIGNAL NOT SET	1,2	1,2	2,3
SKE	SKIP IF A EQUALS M		2,3	2,3
SKG	SKIP IF A GREATER THAN M	2,3	2,3	2,3
SKR	REDUCE M, SKIP IF NEGATIVE		3	3
SKM	SKIP IF A=M ON B MASK		3	3
SKN	SKIP IF M NEGATIVE	2,3	2,3	2,3
SKA	SKIP IF M and A DO NOT COMPARE ONES	2,3	2,3	2,3
SKB	SKIP IF M and B DO NOT COMPARE ONES		2,3	2,3
SKD	DIFFERENCE EXPONENTS AND SKIP		2,3	2,3
	LOGICAL			
ETR	EXTRACT	2	2	2
MRG	MERGE	2	2	2
EOR	EXCLUSIVE OR	2	2	2
	REGISTER CHANGE			
CLA	CLEAR A		1	1
CLB	CLEAR B		1	1
CLR	CLEAR AB	1	1	1
CAB	COPY A INTO B		1	1
CBA	COPY B INTO A		1	1
XAB	EXCHANGE A AND B	1	1	1
BAC	COPY B INTO A, CLEAR B	1	1	1
ABC	COPY A INTO B, CLEAR A	1	1	1
CXA	COPY INDEX INTO A		1	1
CAX	COPY A INTO INDEX		1	1
XXA	EXCHANGE INDEX AND A		1	1
CBX	COPY B INTO INDEX		1	1
CXB	COPY INDEX INTO B		1	1
XXB	EXCHANGE INDEX AND B		1	1
STE	STORE EXPONENT		1	1
LDE	LOAD EXPONENT		1	1
XEE	EXCHANGE EXPONENTS		1	1
CNA	COPY NEGATIVE INTO A		1	1
	SHIFT			
RSH	RIGHT SHIFT AB	2+N	Even $\frac{2+N}{2}$ Odd $\frac{2+N+1}{2}$	2-7
RCY	RIGHT CYCLE AB	2+N	See RSH	2-7
LSH	LEFT SHIFT AB	2+N	See RSH	2-7
LCY	LEFT CYCLE AB	2+N	See RSH	2-7
NOD	NORMALIZE AND DECREMENT X	2+N	See RSH	2-7
	CONTROL			
HLT	HALT	1	1	1
NOP	NO OPERATION	1	1	1
EXU	EXECUTE	1	1	1
EAX	COPY EFFECTIVE ADDRESS INTO INDEX REGISTER	2	2	2
	INPUT/OUTPUT			
MIW	M INTO W BUFFER WHEN READY	2+wait	2+wait	2+wait
WIM	W BUFFER INTO M WHEN READY	3+wait	3+wait	3+wait
MIY	M INTO Y BUFFER WHEN READY	2+wait	2+wait	2+wait
YIM	Y BUFFER INTO M WHEN READY	3+wait	3+wait	3+wait
POT	PARALLEL OUTPUT	3+wait	3+wait	3+wait
PIN	PARALLEL INPUT	4+wait	4+wait	4+wait
EOM	ENERGIZE OUTPUT M	1	1	1
EOD	ENERGIZE OUTPUT TO DIRECT ACCESS CHANNEL			1

SDS 900 Series systems applications

SDS 900 Series computers are easily integrated into a wide range of real-time data acquisition and control systems. SDS offers a complete line of all-silicon systems building blocks, including: analog-to-digital and digital-to-analog converters, amplifiers, multiplexers, and digital logic circuit modules. These devices are all compatible with SDS 900 Series computers and peripheral equipment so that the construction of a complex system simply requires the inter-connecting of the various elements, without expensive design engineering. Some typical systems are illustrated below.



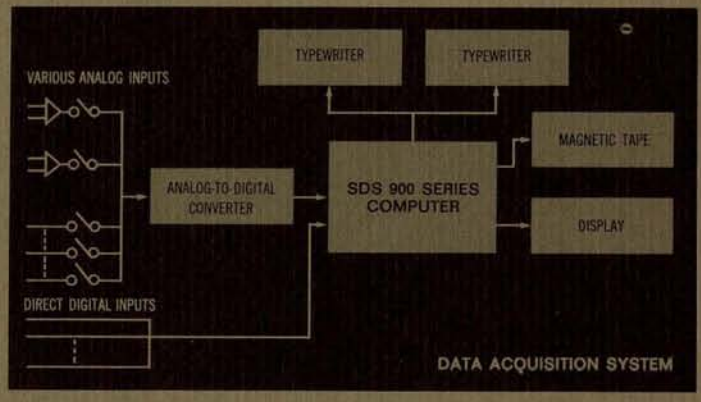


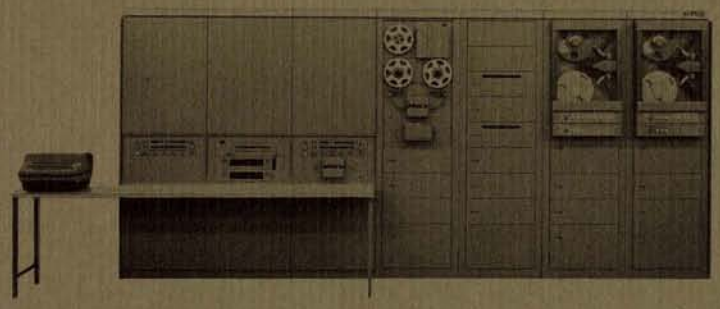
Data acquisition system

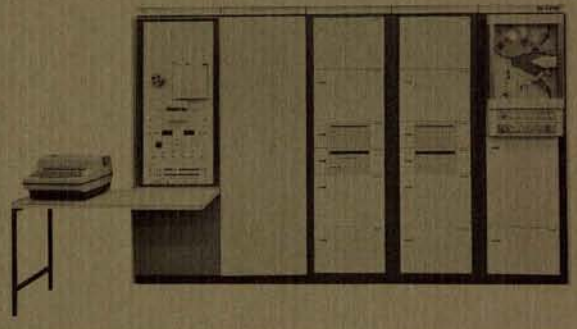
Analog signals of various sorts are multiplexed, under program control, into the analog-to-digital converter. The computer reads the converter output, together with other direct digital inputs, and performs the following functions:

1. Performs zero and full-scale corrections
2. Converts data to engineering units
3. Formats converted data for recording on magnetic tape, and displays selected data points

Typical numbers of inputs that can be processed by the three computers are: SDS 910: 1500/sec.; SDS 920: 3000/sec.; SDS 930: 12,000/sec. These rates are typical and may vary with specific system requirements.







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SCIENTIFIC DATA SYSTEMS

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