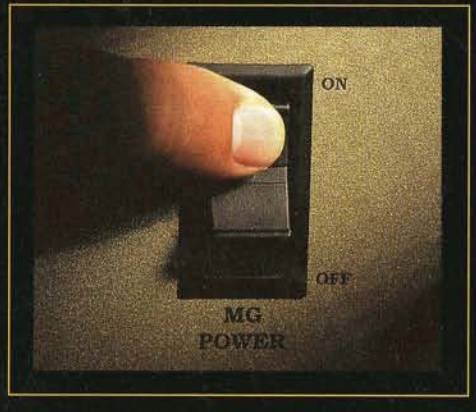
CRAY-3
SUPERCOMPUTER SYSTEMS



CRAY COMPUTER CORPORATION

Corporate Headquarters and Main Facility.

Printed Circuit Board Facility.

Cray Computer Corporation was established as an independent company on November 15, 1989, with corporate headquarters in Colorado Springs, Colorado. The spin-off agreement with Cray Research, Inc. provided for the transfer of currently owned assets, people and initial funding. A transfer of patents and cross-licensing of technology allows each company to pursue its own specific projects unencumbered by patent or technology conflicts. Cray Computer Corporation is a public company listed on the NASDAQ Exchange.

The company's mission is to design, manufacture, sell and support high-performance, general purpose scientific computers. The company's first product is the CRAY-3 supercomputer system.

The main facility in Colorado Springs houses corporate management, hardware and software designers, a gallium arsenide integrated circuit fabrication facility, manufacturing, and system testing. A separate facility, also in Colorado Springs, manufactures the CRAY-3 printed circuit boards.

Introducing the CRAY-3 Supercomputer Systems

The CRAY-3 is the first supercomputer to use gallium arsenide (GaAs) integrated circuits for all of its logic circuitry. The development of GaAs digital circuits was a fundamental step in enabling the CRAY-3 to attain the fastest clock cycle time available in a computer system (two nanoseconds).

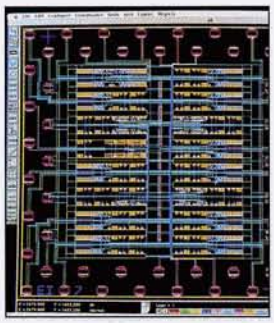
The CRAY-3 offers a balanced combination of high-speed vector processing, very fast scalar processing and the largest directly addressable memory available in a general purpose scientific computer (up to two gigawords). These features, combined with a highly parallel architecture, make the CRAY-3 the most powerful system available to the scientific and engineering communities.

The performance features of the CRAY-3 are a result of a unique synthesis of system architecture and hardware technology.

The CRAY-3 architecture is an evolutionary extension of the CRAY-2 architecture. The system cabinet illustrates the hardware technology required. All the logic and memory circuitry for the machine resides in the top eight inches of an octagon-shaped cabinet only 42 inches wide and 50 inches high. These top eight inches of the system cabinet contain one to 16 computational processors, one system management processor, up to two gigawords of common memory and up to 15 I/O modules.

The logic and memory circuitry are contained in three-dimensional modules only four inches square by one-quarter of an inch thick. Packaging the architecture in this small space allows for short signal paths throughout the system.

The combination of compact packaging and high-performance components was essential to the development of a balanced, powerful and high-speed system required by today's customers. It is unique to the CRAY-3.



CRAY-3 Design

The CRAY-3 achieves its high-performance processing capabilities with the use of GaAs logic circuitry, efficient packaging, liquid immersion cooling, multiple processors and very large common memory. These hardware technologies are then complemented and maximized by the elegant architecture and functional design of the CRAY-3.

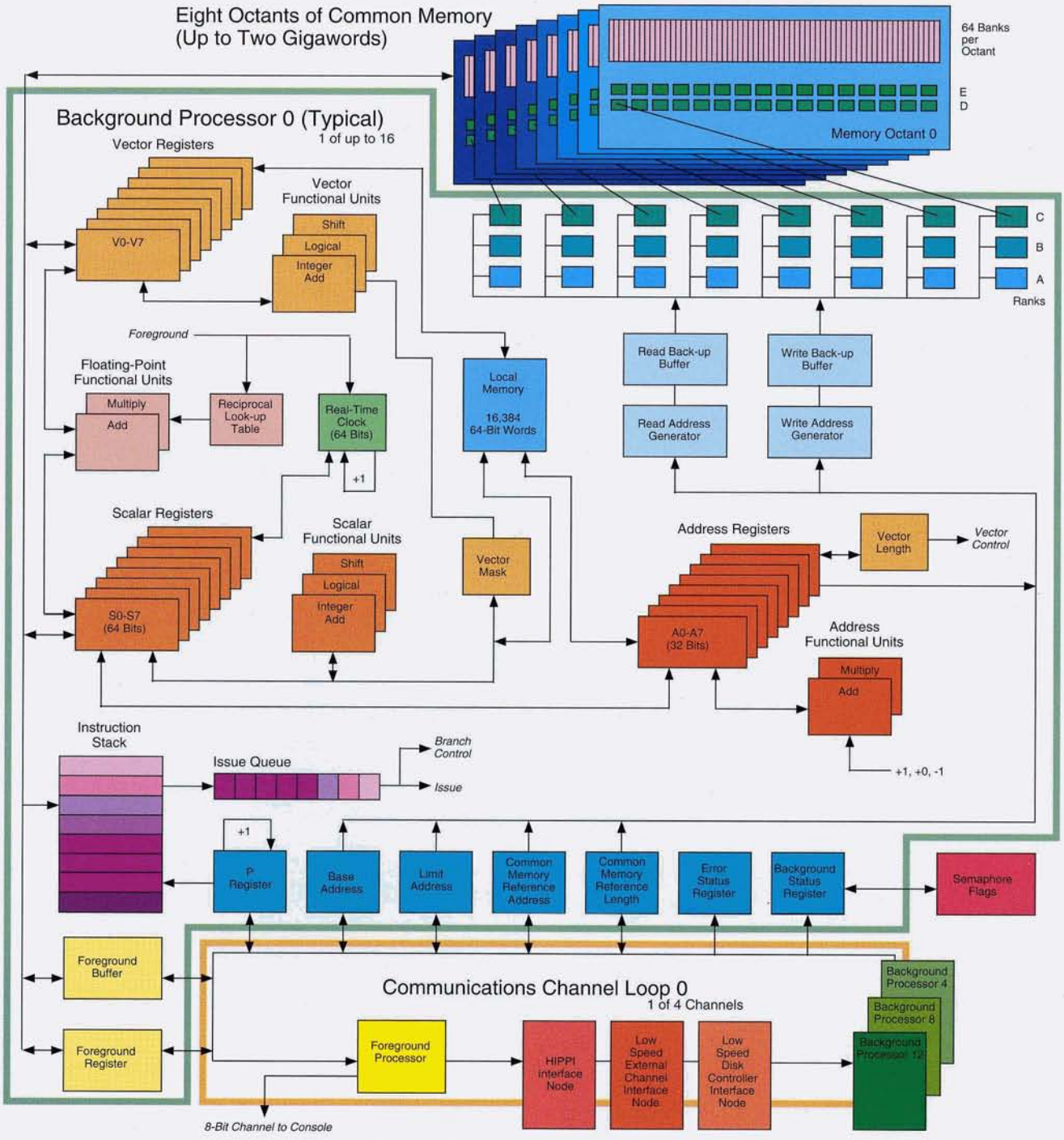
Background Processors

The parallelism in the CRAY-3 extends beyond the multiprocessor features of the system. Each of the background processors consists of three sections: the computation section, the control section and high-speed local memory. A broad mixture of scalar and vector arithmetic and logical operations can take place at the same time in the computation section. Instructions can issue every clock period. Computation instructions execute register-to-register to allow them to operate at the maximum rate possible. The control section supports the parallel operation of the multiple functional units in the computation section. The high-speed local memory is used to temporarily store scalar and vector data during computations. The peak performance of each CRAY-3 background processor is one gigaflop.

The computation section of the background processors contains registers and functional units associated with address, scalar and vector processing. Two integer arithmetic functional units are employed in address processing. Three functional units are dedicated solely to scalar processing, and two floating-point functional units are shared with vector operations. Two additional functional units are dedicated to vector operations allowing CRAY-3 systems to issue one result per clock period in vector mode.

Features of the Computation Section

- Twos complement integer and signed magnitude floating-point arithmetic
- Address and arithmetic registers
  - Eight 32-bit address (A) registers
  - Eight 64-bit scalar (S) registers
  - Eight 64-element vector (V) registers with 64 bits per element
- Address functional units
  - Add/subtract
  - Multiply
- Scalar functional units
  - Logical
  - Shift
  - Integer
    - Add/subtract
    - Population/parity
    - Leading zero count
- Vector functional units
  - Logical
  - Shift
  - Integer
    - Add/subtract
    - Population/parity
    - Leading zero count
    - Compressed iota
- Floating-point functional units
  - Add/subtract
  - Multiply/reciprocal/square root
- Scatter and gather vector operations to and from common memory


Eight Octants of Common Memory
(Up to Two Gigawords)
64 Banks per Octant
E
D
Memory Octant 0
C
B
A
Ranks
Background Processor 0 (Typical)
1 of up to 16
Vector Registers
V0-V7
Vector Functional Units
Shift
Logical
Integer Add
Foreground
Floating-Point Functional Units
Multiply
Add
Reciprocal Look-up Table
Real-Time Clock (64 Bits)
+1
Local Memory
16,384 64-Bit Words
Read Back-up Buffer
Write Back-up Buffer
Read Address Generator
Write Address Generator
Scalar Registers
S0-S7 (64 Bits)
Scalar Functional Units
Shift
Logical
Integer Add
Vector Mask
Address Registers
A0-A7 (32 Bits)
Vector Length
Vector Control
Address Functional Units
Multiply
Add
+1, +0, -1
Instruction Stack
Issue Queue
Branch Control
Issue
+1
P Register
Base Address
Limit Address
Common Memory Reference Address
Common Memory Reference Length
Error Status Register
Background Status Register
Semaphore Flags
Foreground Buffer
Foreground Register
Communications Channel Loop 0
1 of 4 Channels
Foreground Processor
HIPPI interface Node
Low Speed External Channel Interface Node
Low Speed Disk Controller Interface Node
Background Processor 4
Background Processor 8
Background Processor 12
8-Bit Channel to Console