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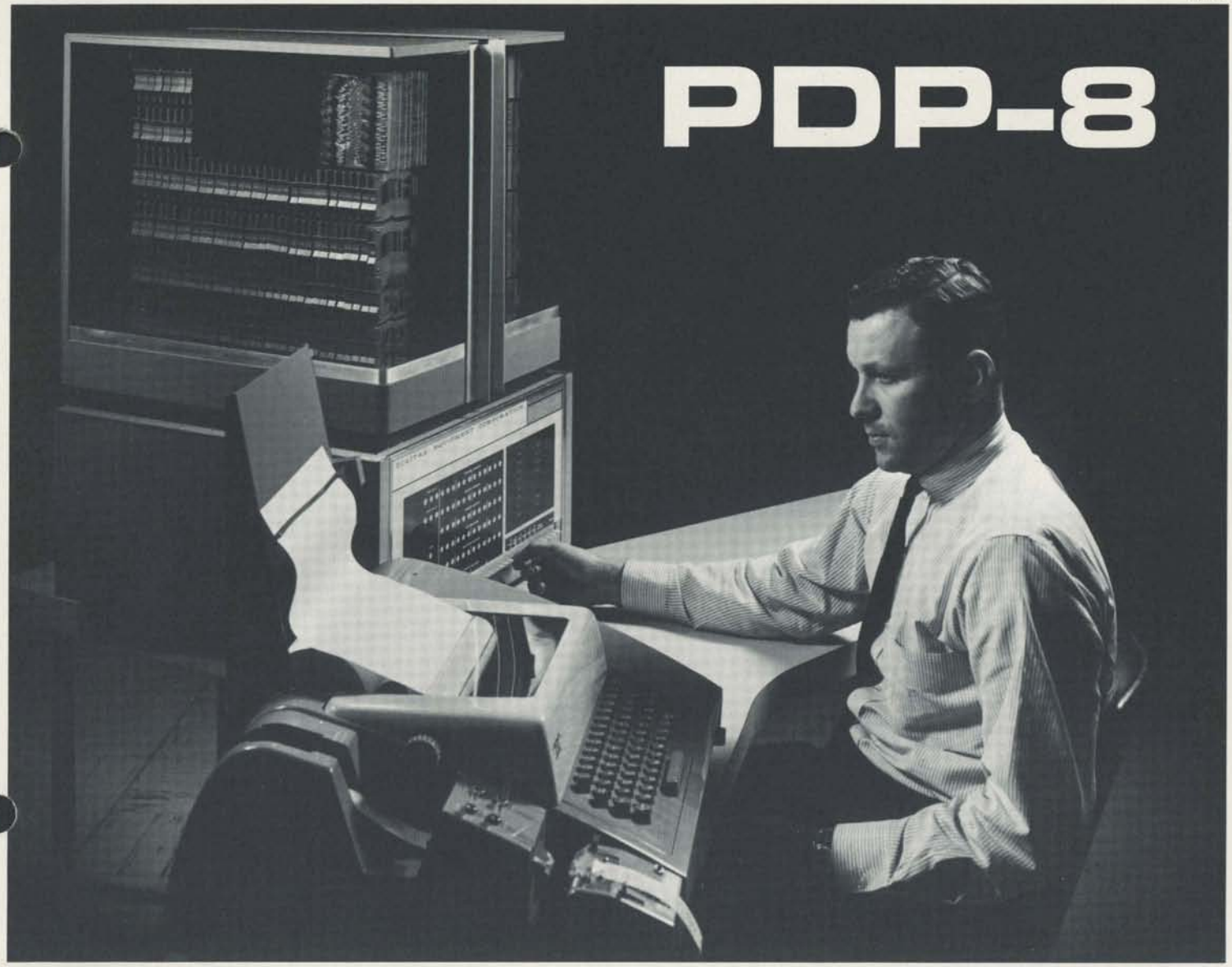
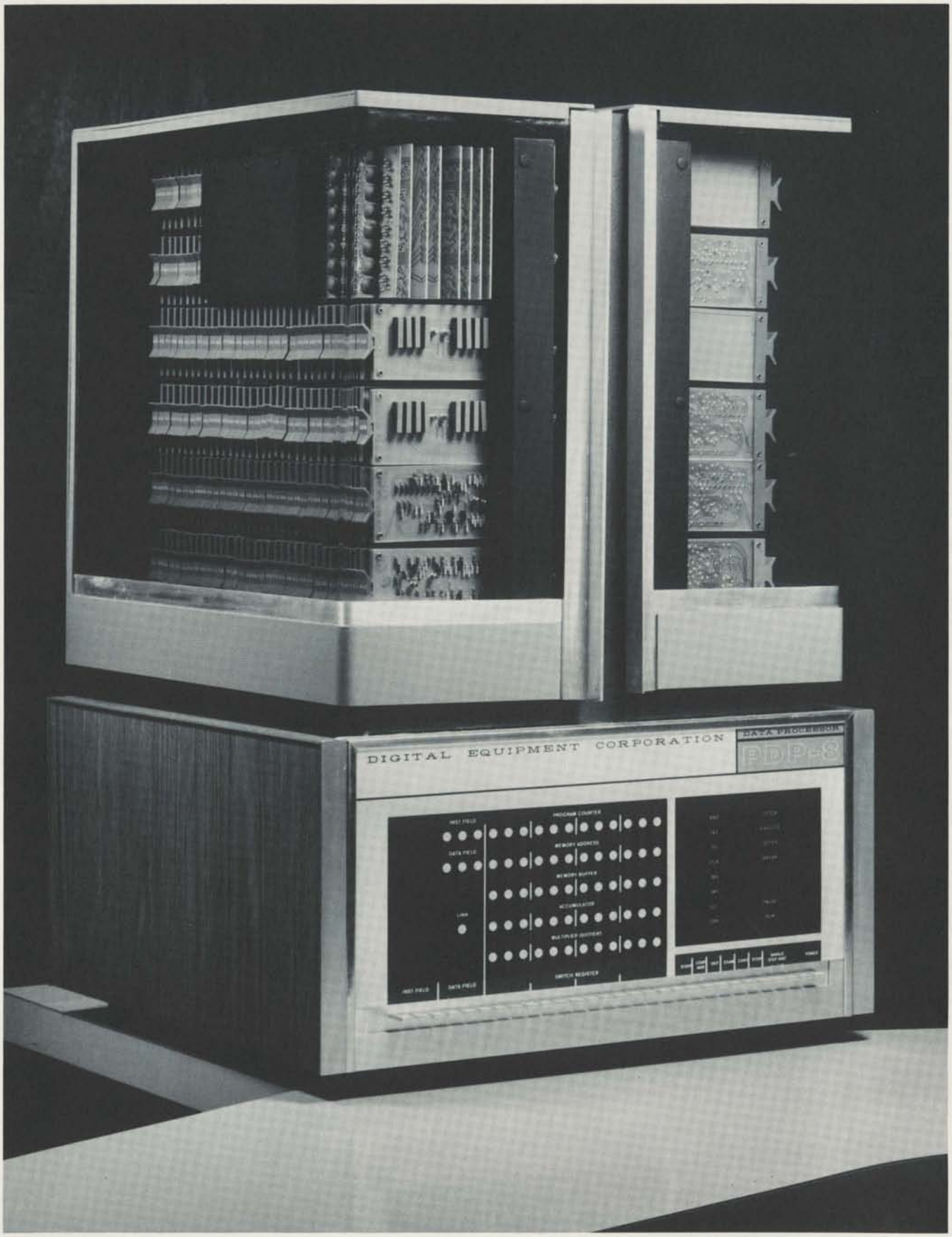


PDP-8

A HIGH SPEED DIGITAL COMPUTER

digital

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS



PDP-8

SCIENTIFIC COMPUTATION

SYSTEMS AND CONTROL APPLICATIONS

ON-LINE DATA COLLECTION AND REDUCTION

The programmed Data Processor-8 (PDP-8) makes available to engineering, scientific, and educational applications a compact but complete general-purpose digital computer with a high-speed, random-access, magnetic-core memory. It is intended for use in data processing or as a control element in on-line data handling, experiment monitoring, or a process control system. The standard PDP-8 is a complete hardware and software system, ready to perform general purpose computations and/or control operations on the day it is delivered. Optional data processing peripheral equipment or special control devices are easily connected to the PDP-8 to form a special-purpose system. Instruction format is simple and logical. One instruction format exists for each of four groups, so that format of individual instructions need not be memorized by the programmer. A complete software system accompanies each hardware system and contains FORTRAN, MACRO-8 assembler, a library of mathematical subroutines, and utility and maintenance programs.

The PDP-8 performs binary operations on 12- or 24-bit 2's complement numbers. PDP-8 circuits use DEC's integrated solid-state silicon FLIP CHIP™ modules and incorporate provisions for marginal checking to insure reliability even under difficult operating conditions. Its 1.6-microsecond cycle time give it a computation rate of 312,500 additions per second and permit it to handle programmed input/output data transfers of rates up to 2 million bits per second, or device-initiated input/output transfers at rates of over 7.5 million bits per second.

The PDP-8 programming system includes a FORTRAN compiler which operates in a basic PDP-8 with 4096 words of core memory. Other elements of the programming system are the MACRO-8 Symbolic Assembler, Symbolic On-Line Debugging Program, Symbolic Tape Editor, Floating Point Package, mathematical function routines, and utility and maintenance programs. On-line tape editing and debugging, a unique DEC combination, establish a close programmer-machine operating mode in which the computer assists in program debugging and edits program tapes to incorporate the programmer's changes. The result is far more speed in preparing operating programs and getting them on-line.

The PDP-8 is capable of servicing up to 64 external devices each requiring up to three commands, or 96 devices each requiring two commands, or 192 devices each requiring one command. The external devices can be special-purpose units or any of DEC's wide selection of unique display or tape equipment and more conventional card, tape, and mass storage equipment. The addition of devices in the field requires no modification to the computer processor.

FLIP CHIP is a trademark of Digital Equipment Corporation

FEATURES

INTEGRATED ALL-SILICON PROCESSOR CIRCUITS
All logic circuits of the basic PDP-8 are constructed from DEC's popular new FLIP CHIP modules.

FULLY PARALLEL ARITHMETIC OPERATION
Reliable high-speed transfers of data, and arithmetic and logical operations within the computer are effected in parallel.

CONTINUOUS DISPLAY OF ACTIVE REGISTERS
The content of the accumulator, link, memory address register, program counter, memory buffer register, instruction register, and major state generator of the basic PDP-8 are continuously indicated by lamps on the operator console. The major registers of optional processor equipment such as the extended arithmetic element and the memory extension control are also indicated by lamps on the operator console with the addition of this equipment.

SINGLE STEP AND SINGLE INSTRUCTION MODES
Switches on the operator console allow a program to be advanced one instruction or one cycle at a time for classroom demonstration, program debugging, or maintenance purposes.

LINK BIT
To facilitate arithmetic operations a link bit is provided so that a carry from the accumulator can be program sampled.

LARGE CORE MEMORY CAPACITY
The PDP-8 is a stored-program computer with a basic 4096-word core memory, capable of being expanded to 32,768 words in 4096-word increments.

INDIRECT ADDRESSING
Subroutine linkage and data accumulation is simplified by the ability to specify addresses indirectly.

AUTO-INDEXING
Eight core memory registers serve as auto-indexing registers to facilitate program searching, multiple input/output list processing, and sorting operations.

1.6 MICROSECOND CYCLE TIME
Instructions are executed in one or two cycles of 1.6 microsecond duration. Maximum execution time is 4.8 microseconds for instructions using indirect memory addressing.

MICRO-PROGRAMMABLE INSTRUCTIONS
All instructions which do not reference core memory (which do not contain a memory address) can be micro-programmed; which allows the programmer to specify several shift, skip, or input/output transfer commands to be performed within one instruction.

PROGRAM INTERRUPT
Standard facilities of the PDP-8 allow a peripheral device to interrupt the operating program and initiate a subroutine.

HIGH SPEED DATA BREAK
Facilities of the standard PDP-8 allow peripheral equipment to interrupt the operating program and effect data transfers to or from the computer core memory at a 1.6 microsecond per word transfer rate. Slower transfers are automatically interlaced with execution of instructions in the main program.

PRE-WIRED OPTIONS
Optional equipment which is closely related to the processor, such as the extended arithmetic element, memory extension control, and one of the analog-to-digital converter options, are pre-wired in the basic PDP-8 so that the time, effort, and cost involved in adding these options at the factory or in the field is a minimum.

FLEXIBLE MECHANICAL DESIGN
Several physical configurations of the computer are available so that it can be used alone in the table model configuration, can be installed as a portion of a user's system by installation in any standard 19-inch electronic equipment cabinet, or can be purchased in a standard DEC computer cabinet with other optional equipment (see Figures 1 and 2).

CUSTOMER TESTED SOFTWARE
Software supplied with the PDP-8 has been use-tested in over 75 installations of the program-compatible PDP-5.

ONE-PASS FORTRAN SYMBOLIC COMPILER
A FORTRAN symbolic compiler which includes dynamic error correcting mode for tape modification without recompiling is supplied with each PDP-8.

MACRO-8 SYMBOLIC ASSEMBLER
Programs can be written in a convenient, meaningful symbolic language consisting of user-defined macro-instructions for translation into machine language by the MACRO-8 program.

DDT-8 PROGRAM
This program allows a programmer to correct and improve a new object program by communicating with the PDP-8 in the source language, via the Teletype unit.

SYMBOLIC TAPE EDITOR PROGRAM
Fast accurate checking, editing, and/or updating of a program can be accomplished with the aid of this program.

BUS I/O SYSTEM
Data, select code, and control signals which pass between the PDP-8 processor and peripheral equipment use bussed connections which simplify system cabling and permit system expansion without making changes to the processor.

BUFFERED INPUT/OUTPUT
All peripheral equipment contains an input/output buffer register for data to be transferred with the computer so that various devices can be operated simultaneously at their maximum speed. The processor does not wait for a device to complete its cycle before continuing the program.

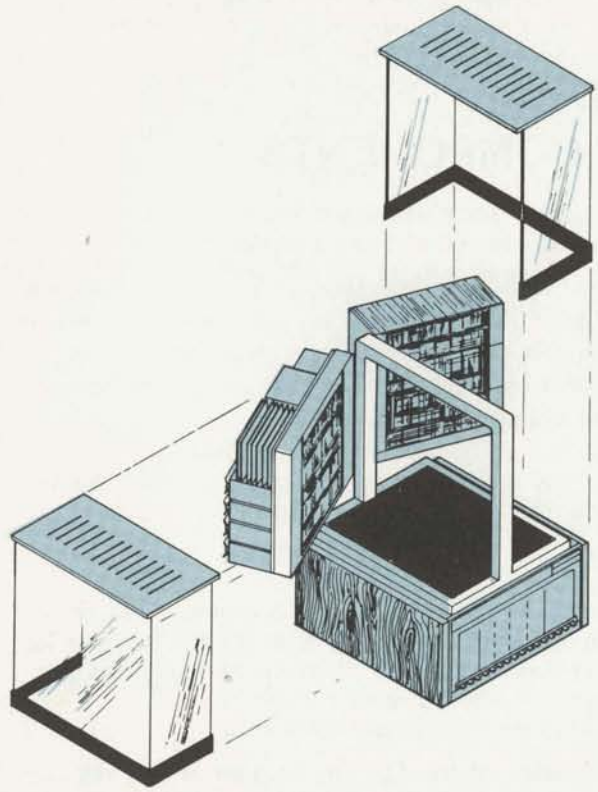


Figure 1 — Table Model PDP-8 showing removeable covers and swinging palets that allow access to all components.

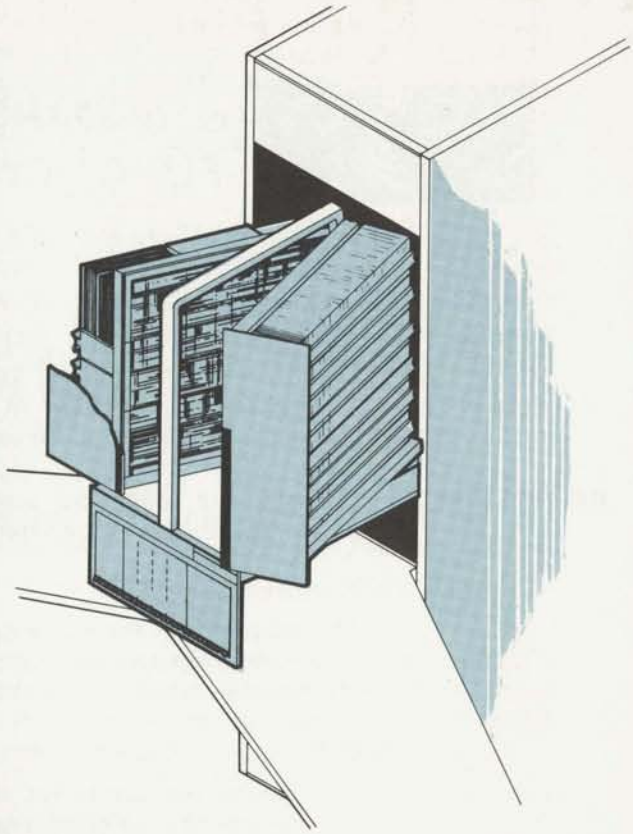


Figure 2 — Console Model PDP-8 showing sliding drawer that facilitates maintenance.

APPLICATIONS

PDP-8's functionally equivalent predecessor, the PDP-5, is being used for the following applications:

RESEARCH EXPERIMENTS AND MEASUREMENT

Pulse-height analysis
Time-of-flight and bubble-chamber measurements
General physics investigation and multichannel-multi-parameter analyzer

QUALITY CONTROL TESTING AND STATISTICAL ANALYSIS

Tensile-strength testing
Electronic component testing
Analog and digital circuit module testing
Computer peripheral equipment testing

DATA ACQUISITION, LOGGING, REDUCTION, AND ANALYSIS

Oceanographic research
Biomedical research
Telemetry
Real-time analog signal monitoring

PROCESS CONTROL

Steel mill control
Typesetting
Chemical and Petroleum industry process control
Nuclear reactor monitor and control

DATA PROCESSING

Open shop computing
Hybrid processing
Media conversion

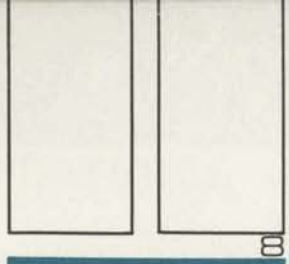
COMMUNICATIONS

Multi-user time-shared computing
Message switching systems
Data collection and processing from remote stations

EDUCATION AND TRAINING

The PDP-8 is an instruction-address, two's complement binary computer which is ideally suited for teaching engineering and programming fundamentals in colleges, high schools, military and industrial schools.

Specific information about each of these applications can be obtained by contacting our Maynard office.



STANDARD PDP-8 FUNCTIONAL COMPONENTS

The standard PDP-8, in any physical configuration, consists of a processor, core memory, operator console, input/output facilities, and a Teletype input/output device. This equipment, shown in Figure 3, constitutes a complete computer system capable of performing general purpose computations and/or control functions. Expansion of the system by addition of optional equipment can be accomplished to perform a specific function or to serve in a particular application.

PROCESSOR

All logic and arithmetic operations, and control functions are performed by the processor. The major registers and control elements are as follows:

Accumulator (AC)

The AC performs the major programmed arithmetic and logic operations and serves as the data input/output register. The AC also serves as a digital buffer register for the optional Analog-to-Digital Converter Type 189.

Link (L)

This one-bit register serves as an extension of the AC. The content of this register can be program sampled and program modified. Overflow into the L from the AC can be checked by the program to greatly simplify and speed up single and multiple precision arithmetic routines.

Program Counter (PC)

The PC determines the core memory address from which the next instruction of a stored program is to be taken. The sequence in which instructions are performed is called program control, and is determined by the PC.

Memory Address Register (MA)

The location in core memory which is selected for data storage or retrieval is determined by the MA. This register can directly address all 4096 words of the standard core memory or in any pre-selected field of extended core memory.

Memory Buffer Register (MB)

The MB serves as a buffer register for all information passing between the processor and the core memory, and serves as a buffer directly between core memory and peripheral equipment during data break information transfers. The MB is also used as a distributor shift register for the Analog-to-Digital Converter Type 189.

Instruction Register (IR)

When an instruction word is read from core memory the three most significant bits (the operation code of all types of instructions) are loaded into the IR. The IR, then decodes the three-bit operation code and determines the basic functions to be performed by the computer, and determines the use to be made of the least significant nine bits of the instruction. When the operation code is decoded as octal number 0 through 5, a memory reference instruction is specified so the least significant bits of the instruction are interpreted to select a core memory address for the operation. When the operation code is decoded as 6_8 or 7_8, an augmented instruction is designated so the least significant bits of the instruction serve as an extension of the operation code and are decoded into numerous microinstructions.

Major State Generator

One or more major control states are entered to determine and execute an instruction. During any one instruction a state lasts for one computer cycle, or 1.6 microseconds. The major state generator determines the machine state during each cycle as a function of the current instruction, the current state, and the condition of the Break Request signal supplied to an input bus by peripheral equipment.

Switch Register (SR)

Twelve toggle switches on the operator console provide a means of manually establishing a word to be set into the computer. The content of the SR can be transferred into the PC as an address by pressing the LOAD ADDRESS key, or can be stored in core memory at the address contained in the PC by pressing the DEPOSIT key. The content of the SR can also be loaded into the AC under program control to allow program modification by programmed evaluation of the word manually set into the SR.

Output Bus Drivers

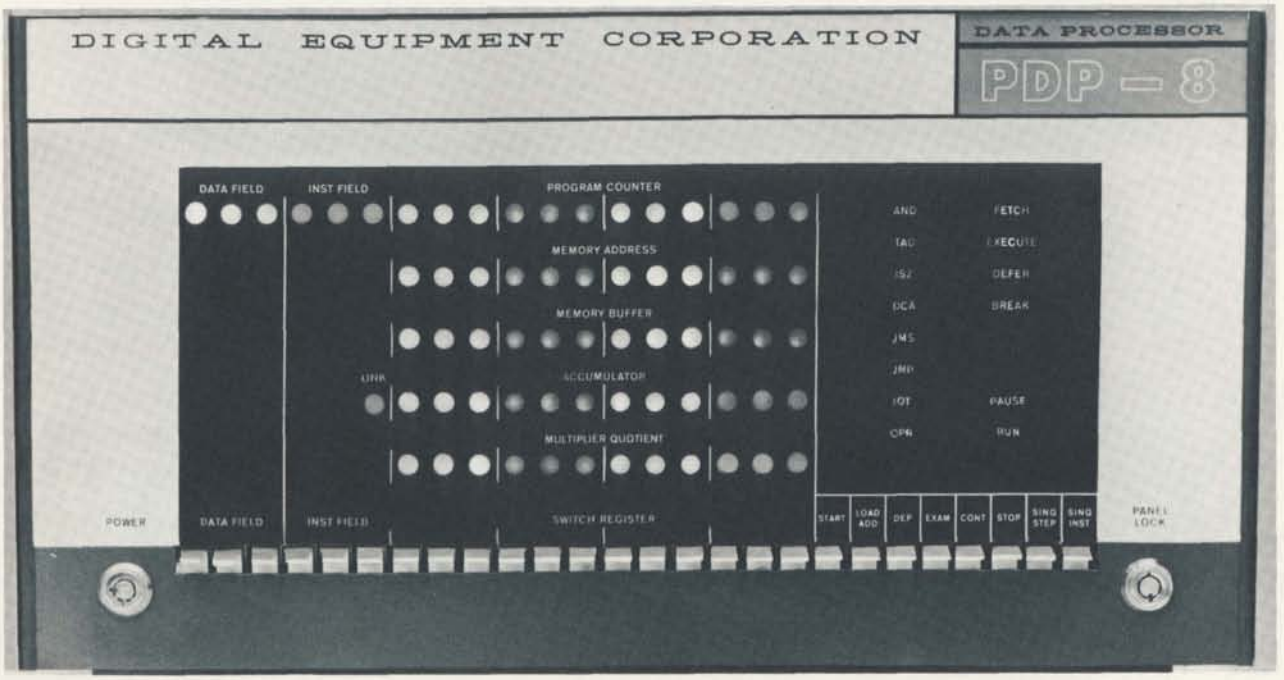
All major output signals from the standard PDP-8, used in programmed and data break information transfers, are power amplified by bus driver modules to allow them to drive a very heavy circuit load.

CORE MEMORY

Storage for instructions to be performed, or for data to be processed or distributed is provided by the core memory. Core memory for the standard PDP-8 has a capacity of 4096 words, 12 bits in length. The PDP-8 is the only computer in its price range with a full-size coincident-current random-address, ferrite-core memory.

OPERATOR CONSOLE

Keys, switches, indicators, and the switch register on the operator console allow manual address and data storage, core memory data examination, the normal start/stop/continue control, and single-step or single-instruction operation that allows each step or each instruction of the program to be monitored visually for demonstration or maintenance.



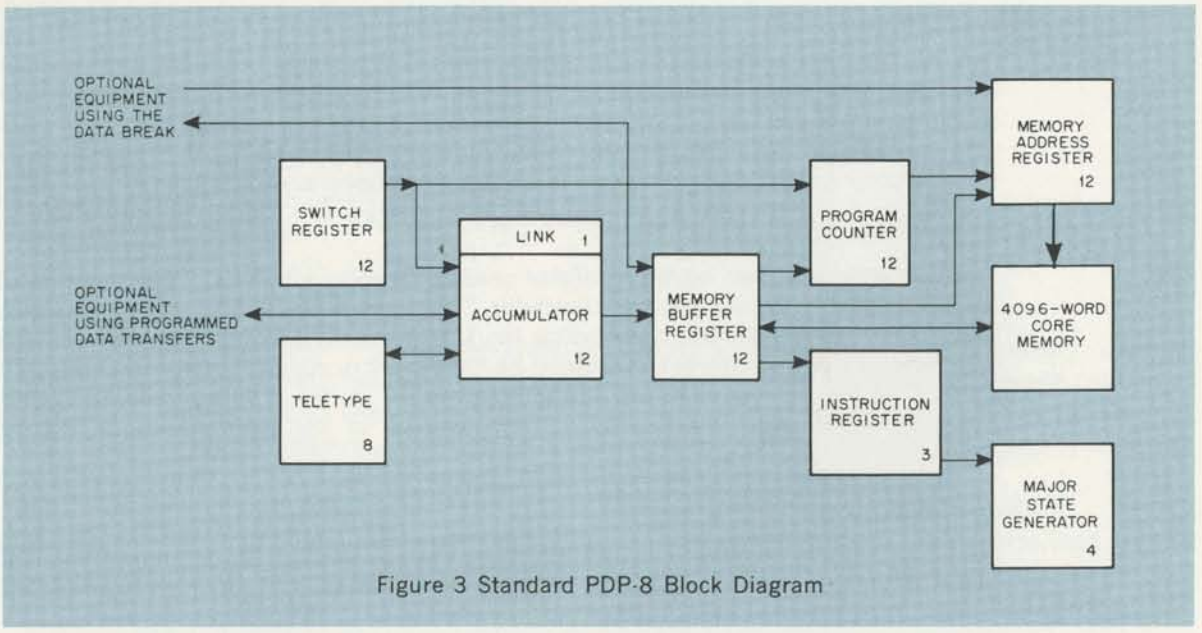


Figure 3 Standard PDP-8 Block Diagram

INPUT/OUTPUT FACILITIES

Standard equipment on the PDP-8 includes facilities for instruction skipping, program interrupt, programmed data transfers, and data break transfers.

Instruction Skip Facility

This facility allows the program to modify itself, or branch, as a function of the content of the AC, the content of the L, or the status of external equipment. Instructions are included in the repertoire of each optional device that allow the program to sense the condition of the device and then skip or proceed to the next instruction as a function of the device status. This feature can be considered programmed decision making.

Program Interrupt Facility

This facility allows signals from external equipment to interrupt the program and initiate a subroutine that services the equipment issuing the signal. Operation using this facility speeds the transfer of the data and control information between the computer and peripheral equipment by allowing conditions in the equipment to initiate a transfer of program control to a subroutine that enacts a transfer, rather than waiting for the main routine to sample the condition and initiate the subroutine.

Programmed Data Transfer Facility

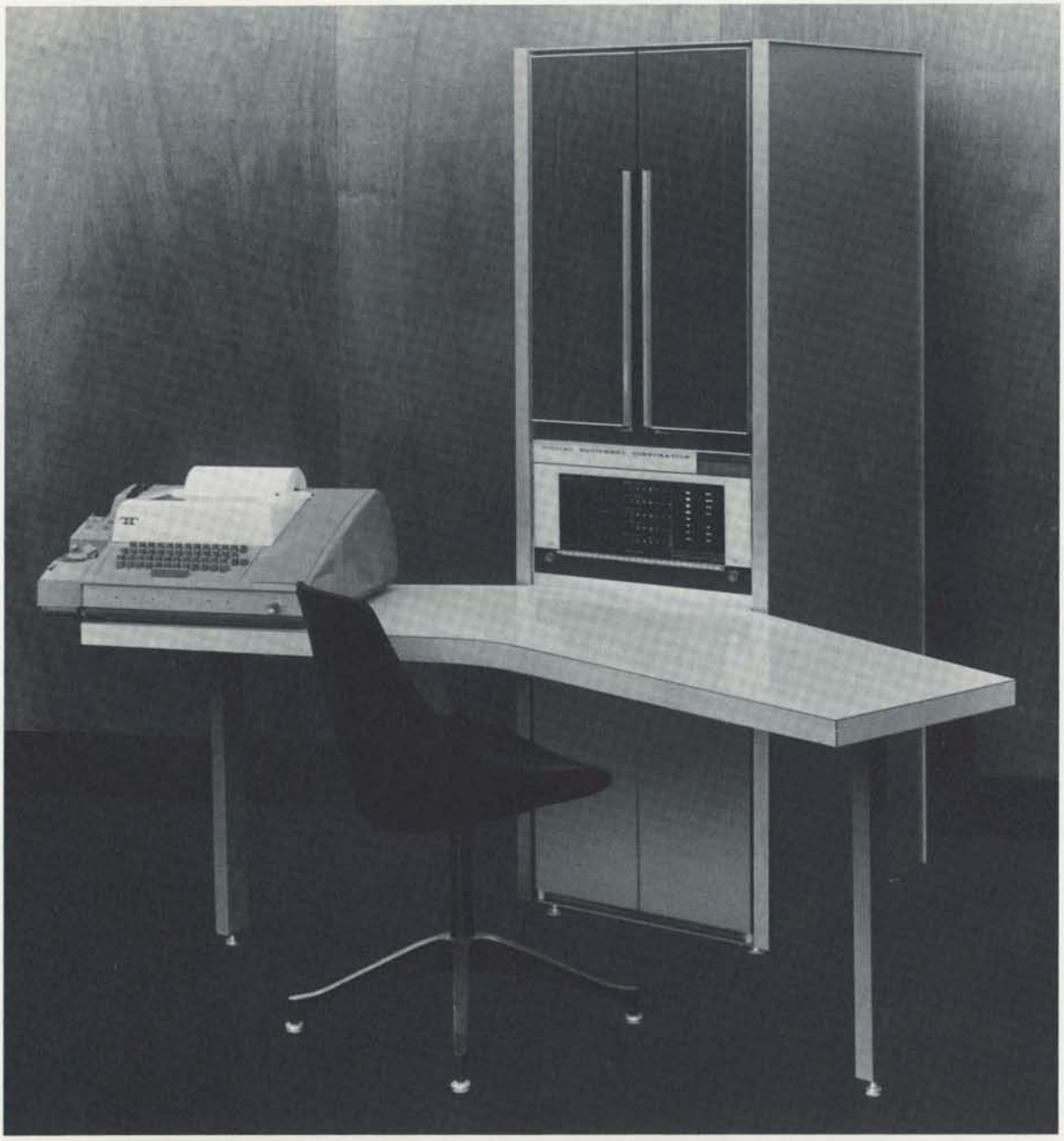
Normally data is transferred between the computer accumulator and an external device under program control. An input bus allows each device to clear the computer accumulator before transferring data into it.

Data Break Transfer Facility

Individual words or blocks of data can be transferred between a peripheral device and the computer core memory, via the MB, at a very rapid rate. A data break is entered upon receiving a Break Request signal and a Transfer Direction signal from the device. When the request is made the computer completes the current instruction, then enters the Break state to enact the transfers. Transfers are performed during every computer cycle until the Break Request signal is removed by the device. The core memory address of each transfer is specified by the peripheral device.

TELETYPE INPUT/OUTPUT DEVICE

A Teletype Model 33 Automatic Send Receive (ASR) set is included in each standard PDP-8. The ASR set transfers information into the PDP-8 from perforated tape or a keyboard, and supplies output information from the computer in the form of perforated tape and/or a typed message. The Teletype rate is 10 characters per second in either direction.



STANDARD PDP-8 INSTRUCTIONS

Instruction words are of two types: memory reference and augmented. Memory reference instructions store or retrieve data from core memory, while augmented instructions do not. All instructions utilize bits 0, 1, and 2 to specify the operation code. Operation codes of 0_8 through 5_8 specify memory reference instructions and codes of 6_8 and 7_8 specify augmented instructions.

MEMORY REFERENCE INSTRUCTIONS

Since the standard PDP-8 system contains a 4096-word core memory, 12 bits are required to address all locations. To simplify addressing, the core memory is divided into blocks, or pages, of 128 words (200_8 address). A memory reference instruction can directly address any one of 256 words; 128 words on page 0 or 128 words on the current page. All other core memory locations are addressed indirectly. Word format of memory reference instructions is shown in Figure 4 and the instructions are listed in Table 1.

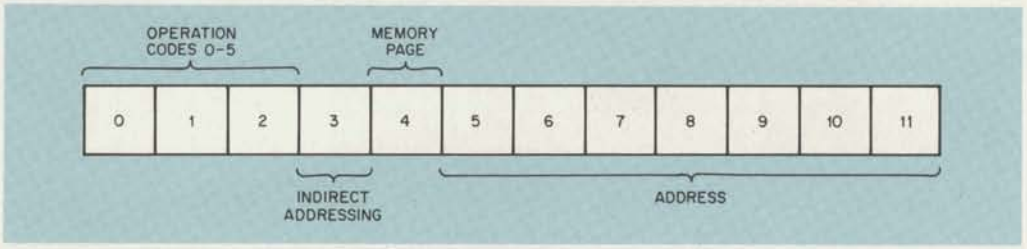


Figure 4 Memory Reference Instruction Format

TABLE 1 MEMORY REFERENCE INSTRUCTIONS

Mnemonic Symbol	Operation Code	Execution Time* (μsec)	Operation
AND Y	0	3.2	Logical AND. The AND operation is performed between the content of memory location Y and the content of the AC. The result is left in the AC, the original content of the AC is lost, and the content of Y is unchanged. Corresponding bits of the AC and Y are operated upon independently. This instruction often called extract or mask can be considered as a bit-by-bit multiplication.
TAD Y	1	3.2	Two's complement add. The content of memory location Y is added to the content of the AC in two's complement arithmetic. The result of this addition is held in the AC, the original content of the AC is lost and the content of Y is unchanged. If there is a carry from AC0, the link is complemented. This link feature is very useful in multiple precision arithmetic.
ISZ Y	2	3.2	Increment and skip if zero. The content of memory location Y is incremented by one. If the resultant content of Y equals zero, the content of the PC is incremented by one and the next instruction is skipped. If the resultant content of Y does not equal zero, the program proceeds to the next instruction. The incremented content of Y is restored to memory. This instruction is useful for incrementing operand addresses and in counting iterations.
DCA Y	3	3.2	Deposit and clear AC. The content of the AC is deposited in core memory at address Y and the AC is cleared. The previous content of memory location Y is lost. This is the basic store instruction.
JMS Y	4	3.2	Jump to subroutine. The content of the PC is deposited in core memory location Y and the next instruction is taken from core memory location Y + 1. This instruction is used for subroutine linkage.
JMP Y	5	1.6	Jump to Y. Address Y is set into the PC so that the next instruction is taken from core memory address Y. The original content of the PC is lost. This instruction is used to transfer program control to randomly selected core memory locations.

*The time listed is for direct addressing; add 1.6 microseconds to this time to determine indirect address execution time.

AUGMENTED INSTRUCTIONS

Instructions which do not reference core memory augment, or extend, the operation code by causing various operations to occur as a function of the content of bits 3 through 11. Augmented instructions with a basic operation code of 6_8 are input/

output transfer (IOT) instructions which serve peripheral equipment. Augmented instructions with a basic operation code of 7_8 are operate (OPR) instructions which deal with processing and sampling the information content of the AC and the L. Both of these instructions are microprogrammed, i.e., multiple operations can be specified and performed simultaneously according to the presence or absence of binary ones in bits 3 through 11.

INPUT/OUTPUT TRANSFER INSTRUCTIONS

Microinstructions of the IOT instruction addresses peripheral equipment to transfer information with it or to initiate operations within it. This instruction contains a 6-bit device selection code and three bits which can be programmed to produce pulses in the selected device that effect a transfer or initiate an operation. Figure 5 shows this instruction format. When an operation code of 6_8 is detected the pause/restart facility is used automatically to halt the program until the computer generates three command pulses at 1 microsecond intervals. These pulses are produced as a function of the content of bits 9, 10, and 11 of the instruction and are used to generate sequential command pulses in the selected device. Up to 64 individual devices can be selected to receive up to three command pulses, or up to 192 devices can each receive one command pulse. Use of the pause/restart facility allows IOT instructions to be performed in one computer cycle. The basic IOT microinstructions are listed in Table 2.

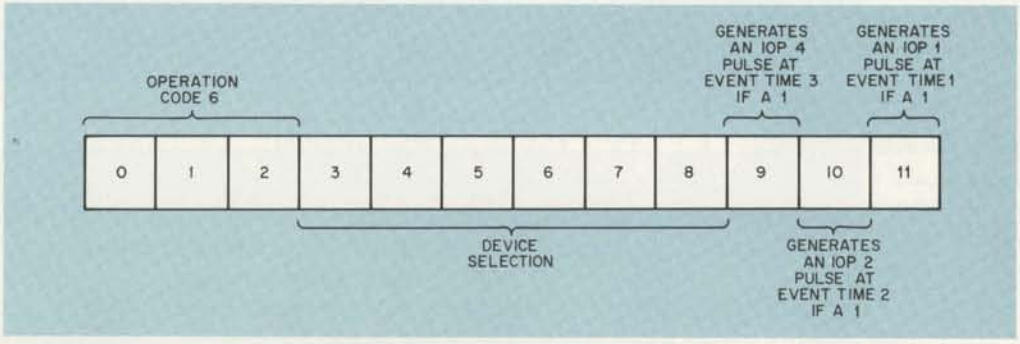


Figure 5 IOT Instruction Format

TABLE 2 BASIC IOT MICROINSTRUCTIONS

Mnemonic Symbol	Octal Code	Event Time	Operation
			PROGRAM INTERRUPT
ION	6001	1	Turn interrupt on and enable the computer to respond to an interrupt request. When this instruction is given, the computer executes the next instruction, then enables the interrupt. The additional instruction allows exit from the interrupt subroutine before allowing another interrupt to occur.
IOF	6002	2	Turn interrupt off i.e. disable the interrupt.
			ANALOG-TO-DIGITAL CONVERTER TYPE 189
ADC	6004	3	Convert the analog input signal to a digital value.
			TELETYPE KEYBOARD/READER
KSF	6031	1	Skip if keyboard flag is a 1.
KCC	6032	2	Clear AC and clear keyboard flag.
KRS	6034	3	Read keyboard buffer static. (This is a static command in that neither the AC nor the keyboard flag is cleared.) The content of the TTI buffer is transferred into AC4-11.
KRB	6036	2, 3	Clear AC, clear keyboard flag, and read the content of the keyboard buffer into the content of AC4-11.
			TELETYPE TELEPRINTER/PUNCH
TSF	6041	1	Skip if teleprinter flag is a 1.
TCF	6042	2	Clear teleprinter flag.
TPC	6044	3	Load the TTO from the content of AC4-11 and print and/or punch the character.
TLS	6046	2, 3	Load the TTO from the content of AC4-11, clear the teleprinter flag, and print and/or punch the character.
			MEMORY PARITY TYPE 188
SMP	6101	1	Skip if memory parity error flag = 0.
CMP	6102	2	Clear memory parity error flag.
			MEMORY EXTENSION CONTROL TYPE 183
CDF	62N1	1	Change data field N. The data field register is loaded with the selected field number (0 to 7). All subsequent memory requests for operands are automatically switched to that data field until the data field number is changed by a new CDF command.
CIF	62N2	2	Prepare to change to instruction field N. The instruction field register is loaded with the selected field number (0 to 7). The next JMP or JMS instruction causes the new field to be entered.
RDF	6214	3	Read data field into AC 6-8. Bits 0-5 and 9-11 of the AC are not affected.
RIF	6224	3	Same as RDF except reads the instruction field.
RIB	6234	3	Read interrupt buffer. The instruction field and data field stored during an interrupt are read into AC 6-8 and 9-11 respectively.
RMF	6244	3	Restore memory field. Used to exit from a program interrupt.

OPERATE INSTRUCTIONS

The OPR instruction consists of two basic groups of microinstructions. When bit 3 contains a binary zero, group OPR 1 is designated and the content of bits 4 through 11 is decoded to cause clear, complement, rotate, and increment operations. When bit 3 contains a binary one, group OPR 2 is designated and the content of bits 4 through 11 is decoded to cause operations that check the content of the AC and the L and continue to, or skip, the next instruction based on the results of the check. Any logical combination of bits within one group can be microprogrammed into one instruction. Figures 6 and 7 show the format of group 1 and group 2 operate microinstructions, and the basic OPR microinstructions are listed in Table 3.

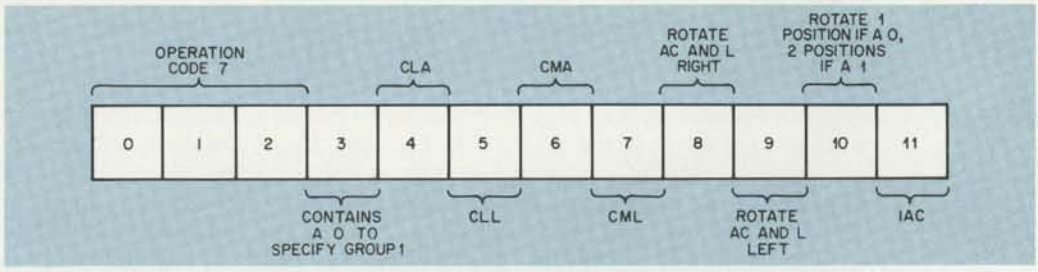


Figure 6 Group 1 Operate Microinstruction Format

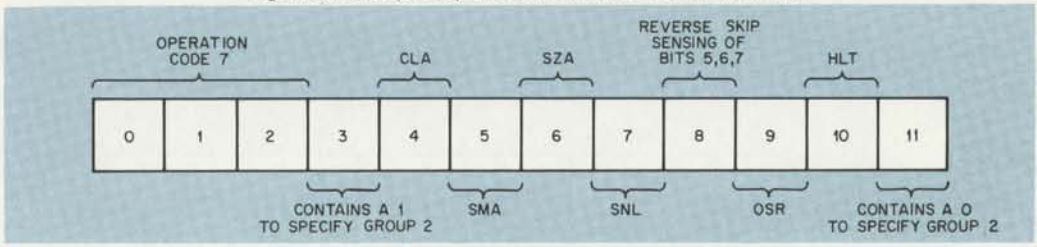


Figure 7 Group 2 Operate Microinstruction Format

TABLE 3 OPERATE MICROINSTRUCTIONS

Mnemonic Symbol	Octal Code	Event Time	Operation
		GROUP 1	
NOP	7000	—	No operation. Causes a 1.6 μsec program delay.
IAC	7001	2	Increment AC. The content of the AC is incremented by one in two's complement arithmetic.
RAL	7004	2	Rotate AC and L left. The content of the AC and the L are rotated left one place.
RTL	7006	2	Rotate two places to the left. Equivalent to two successive RAL operations.
RAR	7010	2	Rotate AC and L right. The content of the AC and L are rotated right one place.
RTR	7012	2	Rotate two places to the right. Equivalent to two successive RAR operations.
CML	7020	1	Complement L.
CMA	7040	1	Complement AC. The content of the AC is set to the one's complement of its current content.
CIA	7041	1, 2	Complement and increment accumulator. Used to form two's complement.
CLL	7100	1	Clear L.
CLL RAL	7104	1, 2	Shift positive number one left.
CLL RTL	7106	1, 2	Clear link, rotate two left.
CLL RAR	7110	1, 2	Shift positive number one right.
CLL RTR	7112	1, 2	Clear link, rotate two right.
STL	7120	1	Set link. The L is set to contain a binary 1.
CLA	7200	1	Clear AC. To be used alone or in OPR 1 combinations.
CLA IAC	7201	1, 2	Set AC = 1
GLK	7204	1, 2	Get link. Transfer L into AC11.
CLA CLL	7300	1	Clear AC and L.
STA	7240	1	Set AC = −1. Each bit of the AC is set to contain a 1.

Mnemonic Symbol	Octal Code	Event Time	Operation
		GROUP 2	
HLT	7402	1	Halt. Stops the program. If this instruction is combined with others in the OPR 2 group the computer stops immediately after completion of the cycle in process.
OSR	7404	2	OR with switch register. The OR function is performed between the content of the SR and the content of the AC, with the result left in the AC.
SKP	7410	1	Skip, unconditional. The next instruction is skipped.
SNL	7420	1	Skip if L ≠ 0.
SZL	7430	1	Skip if L = 0.
SZA	7440	1	Skip if AC = 0.
SNA	7450	1	Skip if AC ≠ 0.
SZA SNL	7460	1	Skip if AC = 0, or L = 1, or both.
SNA SZL	7470	1	Skip if AC ≠ 0 and L = 0.
SMA	7500	1	Skip on minus AC. If the content of the AC is a negative number, the next instruction is skipped.
SPA	7510	1	Skip on positive AC. If the content of the AC is a positive number, the next instruction is skipped.
SMA SNL	7520	1	Skip if AC < 0, or L = 1, or both.
SPA SZL	7530	1	Skip if AC > 0 and if L = 0.
SMA SZA	7540	1	Skip if AC ≤ 0.
SPA SNA	7550	1	Skip if AC > 0.
CLA	7600	2	Clear AC. To be used alone or in OPR 2 combinations.
LAS	7604	1	Load AC with SR.
SZA CLA	7640	1	Skip if AC = 0, then clear AC.
SNA CLA	7650	1	Skip if AC ≠ 0, then clear AC.
SMA CLA	7700	1	Skip if AC < 0, then clear AC.
SPA CLA	7710	1	Skip if AC ≥ 0, then clear AC.

When the Extended Arithmetic Element Type 182 option is added to the PDP-8, a whole class of instructions is added to the OPR 2 instruction list. The extended arithmetic (EAE) microinstructions are specified by an operate instruction (operation code 7) in which bits 3 and 11 contain binary ones. Being augmented instructions, the EAE commands are microprogrammed and can be combined with each other to perform non-conflicting logical operations. Format and bit assignments of the EAE commands are indicated in Figure 8 and the commands are listed in Table 4.

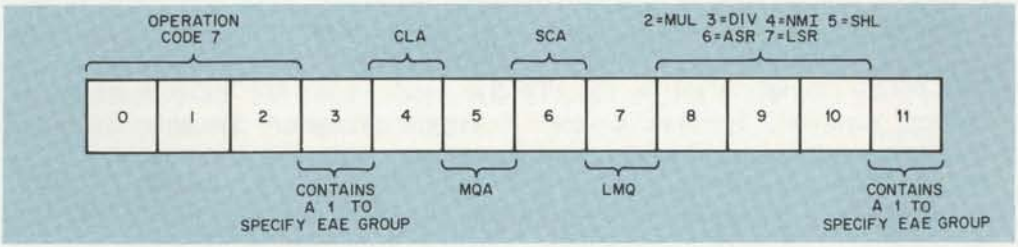
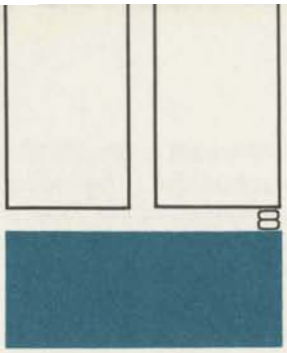


Figure 8 EAE Microinstruction Format

TABLE 4 EAE MICROINSTRUCTIONS

Mnemonic Symbol	Octal Code	Event Time	Operation
MUL	7405	2	Multiply. The number held in the MQ is multiplied by the number held in the next successive core memory location after the MUL command. At the conclusion of this command the most significant 12 bits of the product are contained in the AC and the least significant 12 bits of the product are contained in the MQ.
DIV	7407	2	Divide. The 24-bit dividend held in the AC (most significant 12 bits) and the MQ (least significant 12 bits) is divided by the number held in the next successive core memory location following the DIV command. At the conclusion of this command the quotient is held in the MQ, the remainder is in the AC, and the L contains a 0. If the L contains a 1, divide overflow occurred so the operation was concluded after the first cycle of the division.
NMI	7411	2	Normalize. This instruction is used as part of the conversion of a binary number to a fraction and an exponent for use in floating point arithmetic. The combined content of the AC and the MQ is shifted left by this one command until the content of AC0 is not equal to the content of AC1, to form the fraction. Zeros are shifted into vacated MQ11 positions for each shift. At the conclusion of this operation, the step counter contains a number equal to the number of shifts performed. The content of L is lost.
SHL	7413	2	Shift arithmetic left. This instruction shifts the combined content of the AC and MQ to the left one position more than the number of positions indicated by the content of the next successive core memory location following the SHL command. During the shifting, zeros are shifted into vacated MQ11 positions.
ASR	7415	2	Arithmetic shift right. The combined content of the AC and the MQ is shifted right one position more than the number contained in the next successive core memory location following the ASR command. The sign bit, contained in AC0, enters vacated positions, the sign bit is preserved, information shifted out of MQ11 is lost, and the L is undisturbed during this operation.
LSR	7417	2	Logical shift right. The combined content of the AC and MQ is shifted left one position more than the number contained in the next successive core memory location following the LSR command. This command is similar to the ASR command except that zeros enter vacated positions instead of the sign bit entering these locations. Information shifted out of MQ11 is lost and the L is undisturbed during this operation.
LMQ	7421	2	Load multiplier quotient. This command clears the MQ, loads the content of the AC into the MQ, then clears the AC.
SCA	7441	2	Step counter load into accumulator. The content of the step counter is transferred into the AC. The AC should be cleared prior to issuing this command or the CLA command can be combined with the SCA.
MQA	7501	2	Multiplier quotient load into accumulator. The content of the MQ is transferred into the AC. This command is given to load the 12 least significant bits of the product into the AC following a multiplication or to load the quotient into the AC following a division. The AC should be cleared prior to issuing this command or the CLA command can be combined with the MQA.
CLA	7601	1	Clear accumulator. The AC is cleared during event time 1, allowing this command to be combined with the other EAE commands that load the AC during event time 2 (such as SCA and MQA).



PROGRAMMING SYSTEM

The programming system for the PDP-8 consists of the MACRO-8 Symbolic Assembler, FORTRAN System compiler, Symbolic On-Line Debugging Program, Symbolic Tape Editor, Floating Point Package, mathematical function subroutines, and utility and maintenance programs. All operate with the basic computer. Because the PDP-8 makes high-speed computing available to many new users, the programming system was designed to simplify and accelerate the process of learning to program. At the same time, experienced programmers will find that it incorporates many advanced features. The system is intended to make immediately available to each user the full, general-purpose data processing capability of the PDP-8 and to serve as the operating nucleus for a growing library of programs and routines to be made available to all installations. New techniques, routines, and programs are constantly being developed, field-tested, and documented in the Digital Program Library for incorporation in users' systems.

MACRO-8 SYMBOLIC ASSEMBLER

The use of an assembly program has become standard practice in programming digital computers. This process allows the programmer to code his instructions in a symbolic language, one he can work with more conveniently than the 12-bit binary numbers which actually operate the computer. The assembly program then translates the symbolic language program into its machine code equivalent. The advantages are significant: the symbolic language is more meaningful and convenient to a programmer than a numeric code; instructions or data can be referred to by symbolic names without concern for, or even knowledge of, their actual addresses in core memory; decimal and alphabetical data can be expressed in a form more convenient than binary numbers; programs can be altered without extensive changes; and debugging is considerably simplified.

The MACRO-8 Symbolic Assembler accepts source programs written in the symbolic language and converts core memory locations, computer instructions, and operand addresses from the symbolic to the binary form. It produces an object program tape, a symbol table defining memory allocations, and useful diagnostic messages. Some of the outstanding features of this assembler are:

User-Defined MACROs: Groups of computer instructions required for the solution of specific operations or algorithms can be defined as a MACRO instruction by the user.

Double Precision Integer Pseudo Groups: Positive or negative double precision integers are allotted two consecutive core registers.

Double Precision Floating Point Constant: The format and rules for defining these constants is compatible with the format used by the PDP-8 Floating Point Package.

Operators: Symbols and integers may be combined with a number of operators

+	arithmetic plus	&	Boolean AND
−	arithmetic minus	—	following a symbol indicating the following value should be assembled as an address
:	Boolean inclusive OR		

Literals: Symbolic or mnemonic literals (constants) are arranged automatically.

Variables: Variables can be assigned to page zero at any time and are assigned for the current page automatically.

Parameter Assignments: A symbol may be assigned the value of an expression.

Decimal and Octal Pseudo Operation Codes: The current radix may be specified by decimal or octal.

Text Facility: There are text facilities for single characters and blocks of text.

FORTRAN SYSTEM COMPILER

The FORTRAN (for FORmula TRANslation) System compiler for the PDP-8 lets the user express the problem he is trying to solve in a mixture of English words and mathematical statements that is close to the language of mathematics and is also intelligible to the computer. In addition to reducing the time needed for program preparation, the compiler enables users with little or no knowledge of the computer's organization and operating language to write effective programs for it. The FORTRAN Compiler contains the instructions the computer requires to perform the clerical work of translating the FORTRAN version of the problem statement into an object program in machine language. It also produces diagnostic messages. After compilation, the object program, the operating system and the data it will work with, are loaded into the computer for solution of the problem.

The FORTRAN language consists of four general types of statements: arithmetic, logic, control, and input/output. Fixed and floating point arithmetic can be expressed in both simple and complex numbers. FORTRAN functions include addition, subtraction, multiplication, division, sine, cosine, arctangent, square root, natural log, and exponential.

SYMBOLIC ON-LINE DEBUGGING PROGRAM

On-line debugging with DDT-8 gives the user dynamic printed program status information. It gives him close control over program execution, preventing errors ("bugs") from destroying other portions of his program. He can monitor the execution of single instructions or subsections, change instructions or data in any format, and output a corrected program at the end of the debugging session.

Using the standard Teletype keyboard/reader and teleprinter/punch, the user can communicate conveniently with the PDP-8 in the symbols of his source language. He can control the execution of any portion of his object program by inserting breaks, or traps, in it. When the computer reaches a break, it transfers control of the object program to DDT. The user can then examine and modify the content of individual core memory registers to correct and improve his object program.

SYMBOLIC TAPE EDITOR

The Symbolic Tape Editor program is used to edit, correct, and update symbolic program tapes using the PDP-8 and the Teletype unit. With the editor in core memory, the user reads in portions of his symbolic tape, removes, changes, or adds instructions or operands, and gets back a complete new symbolic tape with errors removed. He can work through the program instruction by instruction, spot-check it, or concentrate on new sections.

FLOATING POINT PACKAGE

The Floating Point Package permits the PDP-8 to perform arithmetic operations that many other computers can perform only after the addition of costly optional hardware. Floating point operations automatically align the binary points of operands, retaining the maximum precision available by discarding leading zeros. In addition to increasing accuracy, floating point operations relieve the programmer of scaling problems common in fixed point operations. This is of particular advantage to the inexperienced programmer.

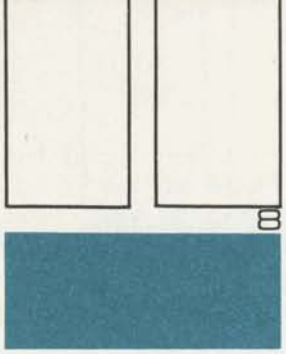
MATHEMATICAL FUNCTION ROUTINES

The programming system also includes a set of mathematical function routines to perform the following operations in both single and double precision: addition, subtraction, multiplication, division, square root, sine, cosine, arctangent, natural logarithm, and exponential.

UTILITY AND MAINTENANCE PROGRAMS

PDP-8 utility programs provide printouts or punchouts of core memory content in octal, decimal, or binary form, as specified by the user. Subroutines are provided for octal or decimal data transfer and binary-to-decimal, decimal-to-binary, and Teletype tape conversion.

A complete set of standard diagnostic programs is provided to simplify and expedite system maintenance. Program descriptions and manuals permit the user to effectively test the operation of the computer for proper core memory functioning and proper execution of instructions. In addition, diagnostic programs to check the performance of standard and optional peripheral devices are provided with the devices.



OPTIONAL EQUIPMENT

Equipment available for inclusion in a PDP-8 system includes options for the processor, reading and punching devices, plotting and printing output machinery, CRT displays, analog-to-digital conversion equipment, magnetic drum and tape storage devices, communication equipment, and equipment housing hardware.

PROCESSOR OPTIONS

EXTENDED ARITHMETIC ELEMENT TYPE 182

This option consists of circuits that allow the PDP-8 to perform parallel arithmetic operations on positive binary numbers much faster than by programmed subroutine. The option multiplies two 12-bit unsigned numbers to obtain a 24-bit product in an average of 15.2 μsec (including access), divides a 24-bit dividend by a 12-bit divisor to obtain a 12-bit quotient in an average of 30.2 μsec (including access), and normalizes a 12-bit number in 1.6 μsec + 0.5 μsec for each shift. When this element is added to the PDP-8 a whole group of microinstructions is added to the OPR instruction to permit automatic multiplication and division, and 24-bit shifting to normalize and scale arguments.

MEMORY EXTENSION CONTROL TYPE 183

The core memory address selection circuits are extended by this option to allow addition of up to seven fields of 4096 words, or up to a total of 32,768 words.

MEMORY MODULE TYPE 184

The basic PDP-8 core memory is extended by one field of 4096 words with the addition of each Type 184. From one to seven Memory Modules can be added to a PDP-8 containing a Memory Extension Control Type 183. The Type 184A is a 12-bit, 4096-word core array similar to standard core memory. The Type 184B is a 13-bit, 4096-word core array used to extend the memory of a system containing the Memory Parity Type 188.

MEMORY PARITY TYPE 188

Automatic checking of the transfer of each word between the processor and core memory is provided by this option. The Type 188 generates a 13th parity bit for each word written in core memory and checks parity during memory reading. A program interrupt is initiated upon detection of a parity error. With the addition of the Type 188 the standard 12-bit core memory and each field of extended memory (at additional cost), is replaced by a 13-bit core array to accommodate the parity bit.

DATA CHANNEL MULTIPLEXER TYPE 129

The Type 129 option expands the data break facilities of the computer to allow up to four input/output devices to transfer data directly with the core memory, via the memory buffer register. Simultaneous data break requests are serviced by the Type 129 according to a prewired priority.

READERS AND PUNCHES

HIGH SPEED PERFORATED TAPE READER AND CONTROL TYPE 750

This equipment senses eight-channel, fan-fold, perforated Mylar or paper tape photoelectrically at 300 characters per second. A Perforated Tape Spooler Type 435 is available to facilitate use of rolled paper tape with the Type 750 in place of fan-fold tape.

HIGH SPEED PERFORATED TAPE PUNCH AND CONTROL TYPE 75A

This equipment punches eight-channel, fanfold paper tape at 63.3 lines per second. A Perforated Tape Spooler Type 436 option can be obtained to facilitate use of rolled paper tape with the Type 75A in place of fan-fold tape.

CARD READER AND CONTROL TYPE 451

Standard punched cards are read optically at up to 200 cards per minute on the Type 451A or up to 800 cards per minute on the Type 451B. Information punched on the cards is read column by column in binary or alphanumeric modes.

CARD PUNCH CONTROL TYPE 450

This device controls on-line buffered operation of a standard card punch machine. Cards are punched one row at a time at 40 millisecond intervals, providing a punching rate of 100 cards per minute. Any or all positions can be punched in any format.

PLOTTER AND PRINTER

INCREMENTAL PLOTTER CONTROL TYPE 350

One plotter selected from the following list of four models of California Computer Products Digital Incremental Recorder can be operated from a DEC

Increment Plotter Control Type 350. Characteristics of the four recorders are:

CCP Model	Step Size (inches)	Speed (steps/minute)	Paper Width (inches)
563	0.01	12,000	31
564	0.005	18,000	31
565	0.01	18,000	12
566	0.005	18,000	12

The Type 350 provides high-speed plotting of points, continuous curves, points connected by curves, curve identification symbols, letters, and numerals under program control.

AUTOMATIC LINE PRINTER TYPE 64

This machine prints a selection of 63 characters on a line of 120 characters at a rate of 300 lines per minute. Printing of one line of 120 characters can be carried out while the next 120 characters are being loaded into the printer. Loading, printing, and format are under program control. Format is program selected from a punched format tape in the printer.

CATHODE RAY TUBE DISPLAYS

OSCILLOSCOPE DISPLAY TYPE 34B

Computer data can be plotted point-by-point on a 5-inch oscilloscope, such as the Tektronix Model RM503, by this option. The horizontal axis of each point is determined by 10 binary bits, and the vertical axis is determined by another 10 binary bits. This option can be obtained with or without the oscilloscope.

PRECISION CRT DISPLAY TYPE 30N

The Type 30N is a random-position point-plotting display with a self-contained, 16-inch CRT using magnetic deflection and focusing.

PHOTOMULTIPLIER LIGHT PEN TYPE 370

A fiber optic light pipe and photomultiplier in the light pen allow high-speed detection of information displayed on the Type 34B or 30N displays. Detection of information by the Type 370 can be sampled by the computer to alter the program.

ANALOG-TO-DIGITAL CONVERTERS

ANALOG-TO-DIGITAL CONVERTER TYPE 189

This successive approximation converter uses the AC and MB of the computer for its digital registers and so provides an inexpensive device capable of selected accuracy from 6 to 12 bits. This option is wired into the basic PDP-8 and requires modules to activate it. Analog input signal range is 0 to −10 volts.

GENERAL PURPOSE ANALOG-TO-DIGITAL CONVERTER TYPE 138D

The Type 138D is a high-speed, successive approximation converter with switch-selected word length from 6 to 11 bits and switch-selected error from ±0.8% to ±0.05%. Conversion time varies from 6 to 45 microseconds according to these switch settings. Analog input signal range is 0 to 10 volts.

GENERAL PURPOSE MULTIPLEXER AND CONTROL TYPE 139D

Up to 64 analog input channels can be selected for application to the input of the Type 189 or Type 138D by the Type 139D. Channels can be program selected in sequence or by individual address. The number of channels that can be selected is determined by the number of optional Multiplexer Switches Type 15780 used in the Type 139D. Each Type 15780 can select four channels.

MAGNETIC DRUMS AND TAPES

SERIAL MAGNETIC DRUM SYSTEM TYPE 250

Blocks of 128 computer words are transferred between the computer core memory and the Type 250. Seven capacities are available from 8,192 to 262,144 words.

DECTAPE DUAL TRANSPORT TYPE 555 AND CONTROL TYPE 552

The DECtape system provides a unique fixed-address magnetic-tape facility for high-speed loading, readout, and program updating. Each DECtape transport contains two independent tape drives. Up to four transports (eight drives) can be used with one control.

MAGNETIC TAPE SYSTEM TYPE 580

The Type 580 is a semi-automatic system consisting of a magnetic tape control and one magnetic tape transport. Data transfer with this system is completely under program control and timing is controlled almost exclusively within this IBM-compatible system. Magnetic tape is read and written at 9,000 characters per second at a density of 200 bits per inch, or 25,000 cps at a density of 556 bpi.

AUTOMATIC MAGNETIC TAPE CONTROL TYPE 57A

Up to eight IBM or IBM-compatible tape transports can be used with the Type 57A to transfer information through the PDP-8 data break facility. Magnetic tape transports are controlled to read or write at densities of 200, 556, or 800 characters per inch at speeds of 75 or 112.5 inches per second.

MAGNETIC TAPE TRANSPORT TYPE 50

The Type 50 can be used with the Type 57A to read or write IBM-compatible magnetic tapes at transfer rates of 15,000 or 41,700 characters per second. Tape speed is 75 inches per second at densities of 200 or 556 characters per inch.

MAGNETIC TAPE TRANSPORT TYPE 570

The Type 570 is a highly sophisticated tape transport that reads and writes at 75 or 112.5 inches per second at program-selected densities of 200, 556, or 800 characters per inch. Transfer rates of up to 90,000 characters per second can be obtained in IBM-compatible format. The Type 570 contains a multiplex interface which permits time-shared use of the transport by two Type 57A tape controls on the same or different computers.

COMMUNICATION EQUIPMENT

DATA COMMUNICATION SYSTEMS TYPE 630

This system is a real-time interface between Teletype stations and the PDP-8 and is ideal for multi-user computer time-sharing, message switching systems, and data collection-processing systems. A variety of Type 630 systems are available for half-duplex and full-duplex operation with up to 64 stations.

EQUIPMENT HOUSING HARDWARE

EQUIPMENT CABINETS

The basic PDP-8 can be housed in a standard computer cabinet 22 1/4 inches wide, 27 1/16 inches deep, and 69 1/8 inches high. When several optional equipments are included in the PDP-8 system additional cabinets can be bolted together to provide an integrated installation.

TABLES AND CHAIRS

Functional tables with adequate work space are available to support the table-model PDP-8 and the Teletype console, or for installation on the front of standard equipment cabinets. Modern computer chairs are also available.

SPECIFICATIONS

PHYSICAL

TABLE MODEL SIZE: 32 inches high, 21 1/2 inches wide, and 21 1/4 inches deep.

TABLE MODEL WEIGHT: 250 pounds.

CONSOLE MODEL SIZE: 31 1/4 inches high, 19 1/2 inches wide, 21 7/8 inches deep (logic), and 24 3/8 inches deep from front of console to back of slides.

CONSOLE MODEL WEIGHT: 250 pounds.

TELETYPE SIZE (ON STAND): 33 inches high to top of console, 44 1/4 inches high to top of copy holder, 22 1/4 inches wide, 18 1/2 inches deep.

TELETYPE WEIGHT (WITH STAND): 40 pounds.

STANDARD CABINET SIZE: 69 1/8 inches high, 22 1/4 inches wide (with end panels), and 27 1/16 inches deep.

STANDARD CABINET DOOR CLEARANCES: 14 7/8 inches at back.

STANDARD CABINET WEIGHT: 225 pounds (with two doors and two end panels).

TABLE (FOR TABLE MODEL) SIZE: 70 1/2 inches wide, 44 inches deep, and 27 inches high.

TABLE (FOR TABLE MODEL) WEIGHT: 100 pounds.

TABLE (FOR CABINET) SIZE: 70 1/2 inches wide, 29 inches deep, braces extend 22 inches into cabinet, 27 inches high.

TABLE (FOR CABINET) WEIGHT: 75 pounds.

ELECTRICAL

POWER REQUIREMENTS: 115 volts, 60 cycles, 1 phase, 7.5 amperes for standard PDP-8 (can be constructed for 220 volts or 50 cycles upon special request).

POWER DISSIPATION: 780 watts.

DIGITAL SIGNAL LEVELS: ground and −3 volts.

INTERNAL CIRCUIT POTENTIALS: +10, −3, −13, −15 volts.

FUNCTIONAL

CYCLE TIME: 1.6 μsec

WORD LENGTH: 12 bits

CORE MEMORY SIZE: 4096 words, expandable to 32,768 in fields of 4096 words.

INSTRUCTIONS: 8 basic instructions: 6 memory reference and 2 augmented. The augmented instructions are microprogrammed to produce more than 200 commands.

INPUT/OUTPUT CAPABILITY: 64 different devices can be individually selected and addressed by 3 command pulses.

TRAINING AND ASSISTANCE

Digital Equipment Corporation offers monthly courses in programming and maintaining each of its computer lines as part of the service provided to purchasers. These courses include instruction by experienced DEC personnel, training manuals, and supplies. Classes are kept small to insure adequate attention to individual students. DEC will assist you with specific programming problems before, during, and after installation of your computer and can provide a computer at our home office to permit you to check your programs under the guidance of DEC programmers.

DECUS LIBRARY AND NEWSLETTER

In addition to the Digital Program Library, users of DEC equipment have access to the growing DECUS Library of utility programs, subroutines, and other programming materials. DECUS (for Digital Equipment Computer Users' Society) was formed to promote a free and effective interchange of information. A principal channel for the dissemination of information is DECUSCOPE, a monthly technical newsletter to which users contribute their ideas, techniques, routines, and program summaries. The DECUS Library distributes program descriptions and the corresponding program tapes and listings to members. Certification of these materials is under the direction of the users' programming committee, which also guides the operation of the Library. DECUS also publishes the proceedings of its annual symposiums and frequent seminars.

ADDITIONAL INFORMATION

OTHER PDP-8 LITERATURE

The following PDP-8 literature is available upon request from DEC's main office, or from any district sales office or representative. Upon request we will add your name to our PDP-8 literature distribution list so that you receive application notes and other current information.

USERS HANDBOOK, F-85: contains computer organization information, detailed description of all instructions, basic PDP-8 programming data, and operating procedures.

INTERFACE BROCHURE: contains detailed information on the interface characteristics of the PDP-8 in an easy-to-read format using many diagrams.

SOFTWARE BROCHURE: contains descriptive material and specifications for the programs supplied with each PDP-8 system.

INSTRUCTION LIST, F-86: is a shirt-pocket list of all memory reference instructions, all augmented instructions, the most common IOT instructions, and the ASCII code (used with most peripheral equipment).

FLIP CHIP MODULES CATALOG, C-105: presents information pertaining to the function and specifications for the line of modules used in the PDP-8. This information is helpful in designing equipment to be connected to the PDP-8 or in learning the technical details of the circuits in the computer.

PRICE LIST, F-82: contains current price information on standard PDP-8 optional equipment.

PRICE ESTIMATE

Your computer system requirements can be analyzed for implementation by a PDP-8 system by personnel from any of DEC's district sales offices or sales representatives.

DIGITAL SALES AND SERVICE

MAIN OFFICE AND PLANT

146 Main Street, Maynard, Massachusetts 01754
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Elsewhere: AC617-897-8821
TWX: 710-347-0212 Cable: Digital Mayn. Telex: 092-027

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Telephone: AC412-351-0700 TWX: 710-797-3657

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Telephone: AC312-825-6626 TWX: 312-823-3572

ANN ARBOR OFFICE:
3853 Research Park Drive, Ann Arbor, Mich. 48104
Telephone: AC313-761-1150 TWX: 810-223-6053

LOS ANGELES OFFICE:
8939 Sepulveda Boulevard, Los Angeles, Calif. 90045
Telephone: AC213-670-0690 TWX: 910-328-6121

SAN FRANCISCO OFFICE:
2450 Hanover, Palo Alto, California 94304
Telephone: AC415-326-5640 TWX: 910-373-1266

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Digital Equipment of Canada, Ltd.,
150 Rosamond Street, Carleton Place, Ontario, Canada
Telephone: AC613-237-0772 TWX: 610-561-1650

IN EUROPE:
Digital Equipment GmbH, Theresienstrasse 29
Munich 2/West Germany
Telephone: 29 94 07, 29 25 66 Telex: 841-5-24226

Digital Equipment Corporation (UK) Ltd.
11 Castle Street
Reading, Berkshire, England
Telephone: Reading 57231 Telex: 851-84327

IN AUSTRALIA:
Digital Equipment Australia Pty. Ltd.,
89 Berry Street
North Sydney, New South Wales, Australia
Telephone: 92-0919 Telex: 790AA-20740
Cable: Digital, Sydney

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