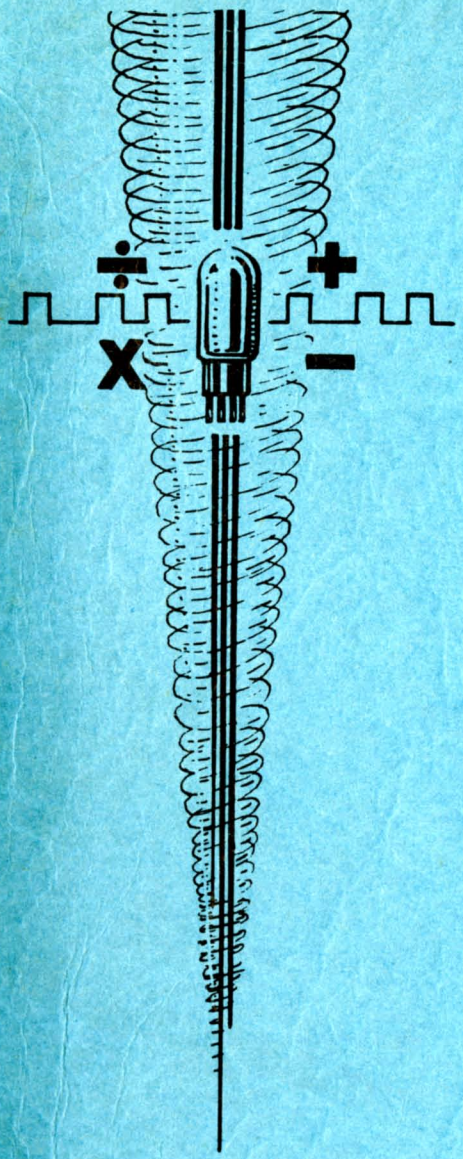

PROJECT WHIRLWIND

Contract N5ori60
Project NR-720-003

REPORT R-161

WHIRLWIND I TEST CONTROL

APRIL 14, 1949

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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PROJECT WHIRLWIND

Report R-161

WHIRLWIND I TEST CONTROL

Submitted to the
OFFICE OF NAVAL RESEARCH
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Report by
George G. Hoberg

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Cambridge 39, Massachusetts

Project DIC 6345

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CONTENTS

WHIRLWIND I TEST CONTROL

ABSTRACT

The test-equipment system known as Whirlwind I test control is described. This system comprises the temporary control and storage facilities necessary for detailed testing of the WWI arithmetic element. The purpose of each unit of the system is discussed with reference to a complete block diagram. Timing is considered in detail, and traffic schedules for individual operations are presented. Operating procedures are outlined briefly. Comments are made on the difficulties encountered with closed loops in computing circuits. Successful achievement of objectives and future plans are discussed.

OBJECT

The overall plan for the construction of the large-scale high-speed electronic digital computer known as Whirlwind I called for completion of the arithmetic-element registers and a number of arithmetic control panels before the main control and storage systems. This scheme was adopted for a number of reasons: (1) the work of constructing the arithmetic element was largely repetitive in nature and therefore more suitable for giving over to an available subcontractor than was the layout and construction of one-of-a-kind units of central control; (2) attainment of the necessary storage facilities involved a long-term development project; (3) it was felt that integration and testing of the complex high-speed pulse networks of the arithmetic element might require more time than installation of other parts of the computer, and that this work could well be in progress during the design and construction of other portions.

A consequence of this approach has been the need for apparatus to supply the completed arithmetic element with pulses properly routed and timed so as to simulate actual computation as closely as possible and thus maximize the significance of test results. The problem is one involving large-scale electronic systems, which unfortunately do not necessarily function properly even when synthesized from components which all appear to function properly before insertion into the system. Individual tests on panels and signal channels, though invaluable as a starting point, were not at all adequate for the purpose. Means had to be devised for simulating all pertinent functions of other elements (central control, storage, etc.) which control or are dependent upon the arithmetic element so as to ensure that it would work properly when finally integrated with the remainder of WWI.

Having been conceived for just such systems simulation, the line of standard test equipment designed by H. Kenosian and other members of the Project was readily adaptable to this task. (See Ref. 1.) Knowledge of this equipment is assumed here. About 50 units of various types were utilized in the manner indicated on drawing E-33028-2, based on a preliminary layout done in conjunction with G. C. Sumner and on the results of discussions with R. P. Mayer. Almost all interconnections shown on the drawing are accomplished by means of plug-in coaxial cables. However,

the arrangement is sufficiently flexible to permit almost any desired pulse routing by the setting of toggle switches, and recabling is not necessary except for occasional tests of an unforeseen nature. This equipment, which has been mounted on racks in the WWI control room (Photograph F644), is known as WWI test control.

Specifically, the test control system provides:

1. All timing and control pulses necessary for operating the arithmetic element so as to perform selected single arithmetic operations.
2. Temporary storage facilities in the form of 3 toggle-switch registers.
3. Indicator lights and synchroscopes for observing the performance of all test equipment and arithmetic-element equipment.
4. A basis for the design of a permanent operator's console.

LOGICAL DESIGN OF SYSTEM

The logical design of test control closely parallels that of portions of WWI. In fact, groups of its test-equipment units correspond almost identically to permanent WWI storage and control elements now in various stages of design, construction, and test.

Storage

The test control is equipped with toggle-switch storage in the form of banks of standard coders. Coders 2-1*, 3-1, and 4-1 represent a 15-digit storage register whose sign digit is provided by pulse standardizer channel 1-1. When inputs are pulsed, the outputs set to (+) send pulses to corresponding WWI busses and thus provide a complete number to be read into an arithmetic register. Coders 2-2, 3-2, 4-2, and standardizer 1-2 provide a second register. Coder 4-3 provides an additional 5-digit register for holding a number to be sent to the step counter.

Master Clock

The clock-pulse generator (8-1) corresponds exactly to the prime pulse source in WWI. Like the WWI clock pulse generator, it is set to provide 2-mc pulses. This prf is reduced to 1 mc and 62.5 kc by a test-equipment binary frequency divider quite

* Numbers refer to coordinates of location of unit in equipment racks; see Note on drawing E-33028-2 and Photograph F644. Racks 9 and 10 are located behind racks 1 to 8 shown in F644.

similar to that planned for WWI. Binary counters 8-2 and 8-3 and register panel 8-4 make up this divider. Coders 8-5 and 8-6 distribute 1-mc and 62.5-kc pulses to the system. Pulse standardizer 10-10 and gate panel 10-4a provide compensating delays for the 2-mc pulses. An experimental WWI panel provides all the functions of the permanent clock-pulse control. The WWI matrix-type time-pulse distributor is simulated in the test control by a conventional whiffletree arrangement of the gate tubes and flip-flops contained in 3 register panels (10-1, 10-3, 10-5) and 4 gate panels (10-2, 10-4, 10-6, 10-7).

Central Control

Coders 6-1 through 6-8 and 7-1, 7-3, 7-6, 7-7 represent the control-pulse output units of the WWI operation matrix. This setup is really the only radical departure from permanent WWI techniques. Control lines must be selected manually and separately, instead of automatically and simultaneously by means of a matrix switch as in WWI.

TIMING

The test control permits performance of arithmetic operations either at high speed or step-by-step at a pushbutton rate. The latter means that if Operating Instruction II of drawing E-33028-2 is followed, each depression of pushbutton No. 5 of the pushbutton pulse generator (3-6) causes execution of one step in the operation.

During high-speed functioning of the equipment, a given Whirlwind arithmetic operation is repeated cyclically at an audio repetition rate. Although standard WWI prf's are used during the operation, the long delay between operations is used to attach significance to the conditions of flip-flop indicator lights. Neither the human eye nor the standard indicator circuit can detect the switching of flip-flops which occurs during the high-speed part of the cycle, so the indicator lights always show only the contents of all flip-flops during the delay between operations. Since provision is made for interposing this long delay (usually of the order of several hundred microseconds) between any two consecutive high-speed steps, the contents of all flip-flops may be conveniently checked at any stage of a gneuine WWI arithmetic operation.

Sequencing of control pulses is quite similar to that of the permanent WWI system, with the exception that in many cases two numbers are extracted from storage during one operation cycle. The operation timing, worked out with G. C. Summer and checked by R. P. Mayer, is illustrated by Mayer's traffic schedules in drawing B-33500. These schedules show information routing and the timing of individual commands for each operation.

The basic timing of a single cycle during cyclical high-speed multiplication is shown in drawing B-33521-1, which indicates the waveforms to be expected at various points in the system under typical conditions. These waveforms, derived theoretically, were accurately reproduced on a synchroscope during the initial integration of the console with arithmetic control.

As can be seen from drawing B-33521-1 and a study of the system, the selected arithmetic operation can be performed either once or successively an arbitrary number of times, m, during each major cycle. The setting of delay unit 3-5b determines the number of times per cycle the operation is performed by inserting a 1 in the flip-flop of register panel 3-8 at a time such that the mth pulse from the time-pulse selector (5-5) passes through the register-panel gate tube and on to the change-to-pushbutton terminal of clock-pulse control. This arrangement permits study of the performance of WWI circuits at prf's at least as high as any to be expected during operation of the finished computer. It also permits observation of complete uninterrupted cycles of 8 time pulses, and in the case of special add, where m must be chosen an even number, permits the required alternation between the special-add and clear-and-add operations. (Special add has little significance unless done in conjunction with clear and add). Register panel 7-2 and gate panel 7-4 provide the binary counter necessary for routing control pulses so as to perform these operations alternately.

A major cycle starts with the emergence of a pulse from the scope synchronizer (3-4). This pulse triggers a synchroscope (5-4) which starts the electron beam across the face of the cathode-ray tube about 90 microseconds later. In addition, after a variable delay, an output trigger is generated which is attenuated and reduced in duration by a simple clipped differentiating circuit. This pulse is used to insert a 1 in the flip-flop of a d-c-coupled register panel (7-11). Less than 16 microseconds after this occurs, a 62.5-kc pulse, delayed about 6 microseconds by a gate-and-delay unit (6-9a), passes through the register-panel gate tube and buffer to a pulse standardizer (8-9b), which inserts a 0 in the flip-flop and simultaneously pulses the restart terminal of clock-pulse control. Here the asynchronous delayed trigger pulse from the scope has effectively been replaced by a synchronous 62.5-kc pulse, and when settings are approximately correct no pulse interference is likely to occur. The pulse standardizer (8-9b) is used to provide discrimination against pulses of marginal amplitude which might be produced if the trigger arrives at the flip-flop less than a rise-time before the delayed 62.5-kc pulse. The time position of the waveforms with respect to the start of the sweep can be adjusted in 16-microsecond increments by the trigger delay, smoothly by the delay unit, or in 1-microsecond increments by the scope-synchronizer delay adjustment.

Upon arrival of the restart pulse at clock-pulse control, high- and low-frequency clock pulses are sent to the arithmetic element, and low-frequency clock pulses (1 mc) begin operating the time-pulse distributor (10-1 through 10-7). If 62.5-kc restorer-generating pulses had been coming from clock-pulse control they are shut off.

The control coders (6-1 through 6-8, etc.) are now pulsed in sequence, starting at the point where the previous cycle had stopped. If the output selector switches of these coders had been set for a given operation, say multiply and round off (mr), as indicated in Table 1 and drawing E-33028-2, one or more steps of the selected operation would be performed on each time pulse.

Drawing B-33521-1 shows the train of events in detail, with the assumption that the time-pulse distributor began counting on time-pulse 5 after the restart pulse. This means that TP4 had been selected on the time-pulse selector (5-5), and the long delay which occurs each cycle had taken place with the indicator lights showing the results of TP4. TP6 and TP7 follow at 1-microsecond intervals. TP7 is sent both to clock-pulse control and to the restorer-pulse generator to cause restoration of the system (which is to be carried out on TP5 in the permanent WWI system). After restoration, TP8 and TP1 follow, but again time pulses are interrupted, since during multiplication TP1 generates a so-called "stop-clock" command to permit the 2-mc multiplication. After the actual multiplication of the two operands is completed, an end carry from the step counter causes resumption of normal counting, and TP2 through TP4 appear in order. The whole operation is then repeated again without pause if delay unit 3-5b was adjusted for $m>1$. The timing drawing represents conditions for performance of 2 time-pulse cycles per major cycle, i.e., $m = 2$.

Note that the previous selection by the operator of TP4 on the time-pulse selector caused TP4 to be sent via a pulse standardizer (3-9a) to a register panel (3-8) connected so as to pass a pulse through its gate tube if delay unit 3-5b has set its flip-flop to 1. Thus only the mth TP4 arrives at the change-to-pushbutton terminal of clock-pulse control. After m complete time-pulse cycles, then, high-speed operation is interrupted, clock pulses no longer come out of clock-pulse control, and in lieu of TP7 the 62.5-kc pulses now coming out of clock-pulse control generate restorer pulses. The contents of all flip-flops are preserved in this manner until the next pulse emerges from the scope synchronizer, whereupon the entire major cycle is repeated.

Flip-flop contents can even be observed during the stop-clock portion of an operation such as multiplication, despite the fact that the time-pulse selector selects only time pulses and not one of the high- or low-frequency clock pulses to the arithmetic element. Such observation of a step within execution of an actual

multiplication command can be accomplished by first selecting the time pulse on which stop-clock occurs, and then by following Operating Instruction III of drawing E-33028-2 and routing the counted selected time pulses through gate-and-delay unit 6-9b to register panel 7-5. Here the smoothly delayed TP1 is exchanged for the next following high-frequency clock pulse, which starts the long delay immediately. Thus the results of, say, the 2nd add pulse or the 13th shift-and-carry pulse of a multiplication can be observed on the indicator lights merely by adjusting the delay at 6-9b to the proper value. The desired pulse can be selected, however, only if the operator orients himself by properly interpreting the number in the step counter or the number of pulses in a synchroscope waveform.

This arrangement has proved to be quite stable. As in the restart system previously described, the pulse standardizer (8-8b) provides excellent amplitude discrimination, and there are no observable regions of marginal operation as the delay is increased to select successive time pulses.

An alternate method of selecting an arithmetic-element clock pulse for observation utilizes the test-reset function of the step counter, whereby the step counter counts only a fraction of the usual number of arithmetic pulses before providing an end carry during multiplication and division. To utilize this feature the normal multiply-reset or divide-reset line must be disconnected by a toggle switch* at the step counter, and the arbitrary number to which the step counter is to be reset is introduced by pulsing the test-reset line simultaneously with execution of the stop-clock command.

The arbitrary number is selected on the step-counter test-reset switch (3-3), which controls crystal gates at each SC flip-flop. If now the time pulse is selected which <u>follows</u> that on which stop-clock occurs, the indicator lights show the results after the (33-n)th pulse sent to the step counter, where n is the number set into the test-reset switch.

This alternate method has the advantage that the particular pulse observed is identified by the switch setting, and that no smoothly adjustable multivibrator delay of uncertain length is involved. It has the disadvantage that the results of add pulses during multiplication and carry pulses during division cannot be observed because the SC end carry can never occur immediately after one of these pulses, since only shift-and-carry and divide-shift-left pulses are counted.

* When one of these lines is disconnected an indicator light glows on the test-reset switch (3-3) at the console to remind the operator that abnormal operating conditions prevail.

SUMMARY OF OPERATING PROCEDURE

Drawing E-33028-2 contains a list of operating instructions which point out the switch settings required for various operating conditions. These instructions necessarily assume reasonable familiarity with both WWI and the objects and capabilities of the test control system already discussed. They are amplified to some extent below.

I. Start - Depression of the start pushbutton grounds the suppressor grid of a clock-pulse control gate-tube so as to permit 62.5-kc pulses to generate restorer pulses which establish normal operating conditions within the many a-c coupling circuits handling flip-flop waveforms. Whenever the system stops restoring for any reason, this start button (6-6) must be depressed.

II. Step-by-step pushbutton operation - The equipment is placed in condition for this type of operation merely by blocking the restart pulse which normally comes to clock-pulse control indirectly from the scope synchronizer during cyclical high-speed operation. Each depression of pushbutton 5 of the pushbutton pulse generator (3-6) then produces one step of the operation.

III. Cyclical high-speed operation - This is more or less the normal mode of operation for the test control. A requirement is that one of the time-pulse selector buttons be depressed at all times to provide the change to pushbutton pulse which initiates the long delay. Note that although "pushbutton" operation prevails except during the relatively short time devoted to the actual time-pulse cycles, it is of no use to attempt to use any of the pushbutton controls when operating in this manner because a single pushbutton pulse merely disturbs a single major cycle, and has essentially no effect upon observable operating conditions.

IV. Select arithmetic operation - Table I provides better concepts than drawing E-33028-2 as to the manner in which the control-pulse output coder switches are to be set up for a specific arithmetic operation. Switches are to be set at (+), (0), or (-) as indicated in the table. Incorrect setting of these switches may cause omission of or interference between commands.

V. Store numbers - One coder is by its nature a 5-digit toggle-switch storage register, the use of which in this system should be obvious. (See Ref. 1 and 2.)

VI. Clear - During testing and step-by-step pushbutton operation it is sometimes desirable to clear one or all WWI registers and control flip-flops. Such clearing is accomplished here with a single pushbutton after proper selection of the flip-flops to be cleared by the setting of the output switches of 2 coders (5-2 and 5-3).

Another factor to be considered by the operator of the system is the pulse amplitude at all points. The equipment is such that 20-volt peak amplitudes are satisfactory throughout the system except at the scope synchronizer. Sufficient amplitude can be obtained at the input only by not terminating the cables which pulse the synchronizer, and the synchronizer output amplitude should be as great as possible to assure synchronization of the synchroscopes. At a point like the gate input of register panel 8-4, which is driven by the high-power output of binary counter 8-3, an adjustable T-pad consisting of two 100-ohm potentiometers makes a convenient attenuator and amplitude controller. Trouble can be expected wherever gate-tube pulse inputs are much in excess of 20 volts.

TROUBLE LOCATION IN CLOSED-LOOP SYSTEMS

One basic, but by no means prohibitive, difficulty which has been encountered is the location of trouble in a closed loop which has stopped functioning for an unknown reason. Operation of test control with the arithmetic element involves a number of pulse feedback loops which, although they make a fault immediately obvious, have the undesirable property of also making the fault difficult to find. For instance, suppose upon depression of the start button the system will not commence cyclical high-speed operation, and scope checks show all necessary pulses to be arriving at clock-pulse control. Either clock-pulse control, or the time-pulse distributor, or any one of many test equipment units in the basic control loop may not be working, and logical isolation of the source of error is often not readily accomplished. Although various open-loop tests are possible, trouble-shooting in such information feedback systems is in most cases fairly difficult.

One closed-loop trouble is brought about by occasional interruption of the step-counter end carry when a test probe is applied to a circuit terminal so as to block even a single end-carry pulse. The system is left in the stop-clock condition, no restoration occurs, and the contents of all registers are lost. Plans are being considered to remedy this difficulty by making a provision for an artificial end-carry pulse if the actual one does not occur, but such artificial systems are often a source of trouble in themselves.

Another information feedback difficulty characteristic of this system has been encountered in tests in which pulse amplitudes are varied to ascertain allowable operating limits. Under marginal conditions the information residing in the various storage elements of the arithmetic element and test control systems often is not the same at corresponding points of successive major cycles because circuits appear to operate intermittently. Means for reducing difficulties from this effect by automatic resetting of critical elements to predetermined states by non-marginal pulses once each major cycle are being studied by H. Ziegler. Improvements here should permit a clearer evaluation of marginal performance in some cases.

It should be emphasized that the difficulties mentioned, although bothersome, were not of such a nature as to require an inordinate amount of time or to impair the effectiveness of the apparatus as a test system.

RESULTS

During tests extending over a period of about three months, test control has performed satisfactorily with the WWI arithmetic element, and many informative experiments have been conducted. All operations indicated by symbols in Table I have been successfully performed. Correct answers to addition, subtraction, multiplication, and division problems have been consistently obtained. With an error-alarm system improvised from the WWI program register, a trial run resulted in correct multiplication of two 15-digit binary numbers about 150,000,000 times in succession, after which the experiment was purposely stopped.

It is expected that a large amount of valuable quantitative information on the performance of the circuits in the arithmetic element can be accumulated during its operation with test control. As permanent units are installed for performing the functions now supplied by test control the test equipment system will be correspondingly reduced in size and function. Relatively little trouble is foreseen during these changeovers because of the great similarity between test and permanent systems, and because of the operating experience and data which can be obtained after each new installation in this step-by-step synthesis of Whirlwind I.

Signed _____
George G. Hoberg

Approved _____
N. H. Taylor

Approved _____
Jay W. Forrester

GGH:ejc

TABLE I

Coder Channel	Function	Oper:	Switch Setting mr	mh	dv	sl	sr	ca	ad	cs	su	am	sa-ca	sf	cp
(1) a 1	stop clock		-	-	0	-	-	0	0	0	0	0	0	-	0
2	subtract AR to AC		0	0	+	0	0	0	0	+	+	0	0	0	0
3	multiply		+	+	0	0	0	0	0	0	0	0	0	0	0
4	shift right		0	0	0	0	+	0	0	0	0	0	0	0	0
5	add AR to AC		0	0	0	0	0	+	+	0	0	+	+	0	0
b 1	shift left		0	0	0	+	0	0	0	0	0	0	0	0	0
2	point off		0	0	0	0	0	0	0	0	0	0	0	-	0
3	add to SC		0	0	0	+	+	0	0	0	0	0	0	0	0
4	clear sa FF		+	+	+	+	+	+	+	+	+	+	+	+	+
5	SC test reset		0	0	0	0	0	0	0	0	0	0	0	0	0
(2) a 1	stop clock		0	0	-	0	0	0	0	0	0	0	0	0	0
2	divide		0	0	+	0	0	0	0	0	0	0	0	0	0
3	carry		+	+	0	0	0	+	+	+	+	+	+	0	0
4	roundoff		+	0	0	+	+	0	0	0	0	0	0	0	0
5	SC test reset		0	0	0	0	0	0	0	0	0	0	0	0	0
(3) a 1	FF storage read in		-	-	-	-	-	-	-	-	-	-	-	-	-
2	BR read out		0	0	+	0	0	0	0	0	0	0	0	0	0
3	clear BR		+	0	0	0	0	0	0	0	0	0	0	0	0
4	prod. sign		+	+	+	+	+	0	0	0	0	0	0	+	0
5	spare		0	0	0	0	0	0	0	0	0	0	0	0	0
b 1	SC read out		0	0	0	0	0	0	0	0	0	0	0	+	0
2	arith. check		0	0	0	+	+	+	+	+	+	+	+	0	0
3	spare		0	0	0	0	0	0	0	0	0	0	0	0	0
4	special add		0	0	0	0	0	0	0	0	0	0	+	0	0
5	spare		0	0	0	0	0	0	0	0	0	0	0	0	0
(4) a 1	preset SC		-	-	-	-	-	-	-	-	-	-	-	-	-
2	AC read out		+	+	0	+	+	+	+	+	+	+	+	0	0
3	clear AR		+	+	+	+	+	+	+	+	+	+	+	+	+
4	FF sto. read in		-	-	0	-	-	-	-	-	-	-	-	0	0
5	spare		0	0	0	0	0	0	0	0	0	0	0	0	0
(5) a 1	(delayed) add AR to AC		+	+	+	+	+	0	+	0	+	+	+	+	+
2	No. 1 sto. reg. read out		+	+	+	+	+	0	+	0	+	+	+	+	+
3	AR read in		-	-	-	-	-	-	-	-	-	-	-	-	-
4	clear AC		+	+	+	+	+	+	+	+	+	+	+	+	+
5	spare		0	0	0	0	0	0	0	0	0	0	0	0	0

TABLE I (continued)

Coder Channel	Function	Switch Setting												
	Oper:	mr	mh	dv	sl	sr	ca	ad	cs	su	am	sa-ca	sf	cp
(6) a 1	clear AR	+	+	+	+	+	+	+	+	+	+	+	+	0
2	AC sign	+	+	+	+	+	0	0	0	0	0	0	+	0
3	clear BR	+	+	+	+	+	+	+	+	+	+	+	+	+
4	No. 3 sto. reg. read out	0	0	0	+	+	0	0	0	0	0	0	0	0
5	special carry	0	0	0	0	0	+	0	+	0	0	+	0	0
b 1	SC read in	0	0	0	-	-	0	0	0	0	0	0	0	0
2	clear FF storage	+	+	+	+	+	+	+	+	+	+	+	+	+
3	compare	0	0	0	0	0	0	0	0	0	0	0	0	+
4	spare	0	0	0	0	0	0	0	0	0	0	0	0	0
5	spare	0	0	0	0	0	0	0	0	0	0	0	0	0
(7) a 1	No. 2 sto. reg. read out	+	+	+	+	+	+	+	+	+	+	+	+	+
2	AR read in	-	-	-	0	0	-	-	-	-	-	-	0	-
3	AC to BR	+	+	0	0	0	0	0	0	0	0	0	0	0
4	add to SC	0	0	0	+	+	0	0	0	0	0	0	0	0
5	BR read in	0	0	0	-	-	0	0	0	0	0	0	-	0
b 1	spare	0	0	0	0	0	0	0	0	0	0	0	0	0
2	spare	0	0	0	0	0	0	0	0	0	0	0	0	0
3	TP7 to CPC	-	-	-	-	-	-	-	-	-	-,	-	-	0
4	Complement R7-2	0	0	0	0	0	0	0	0	0	0	0	0	0
5	Restore	+	+	+	+	+	+	+	+	+	+	+	+	+
(8) a 1	AR sign	+	+	+	0	0	0	0	0	0	0	0	0	0
2	clear AC	+	+	0	0	0	0	0	0	0	0	0	0	0
3	magnitude	0	0	0	0	0	0	0	0	0	+	0	0	0
4	AR read out	0	0	0	0	0	0	0	0	0	0	0	0	0
5	BR read in	0	0	0	0	0	0	0	0	0	0	0	0	0

REFERENCES

1. R-143, Specifications for Standard Test Equipment

2. R-144 through R-151, Operating Instructions for Individual Units of Standard Test Equipment.

LIST OF ILLUSTRATIONS

Drawing No.

E-33028-2

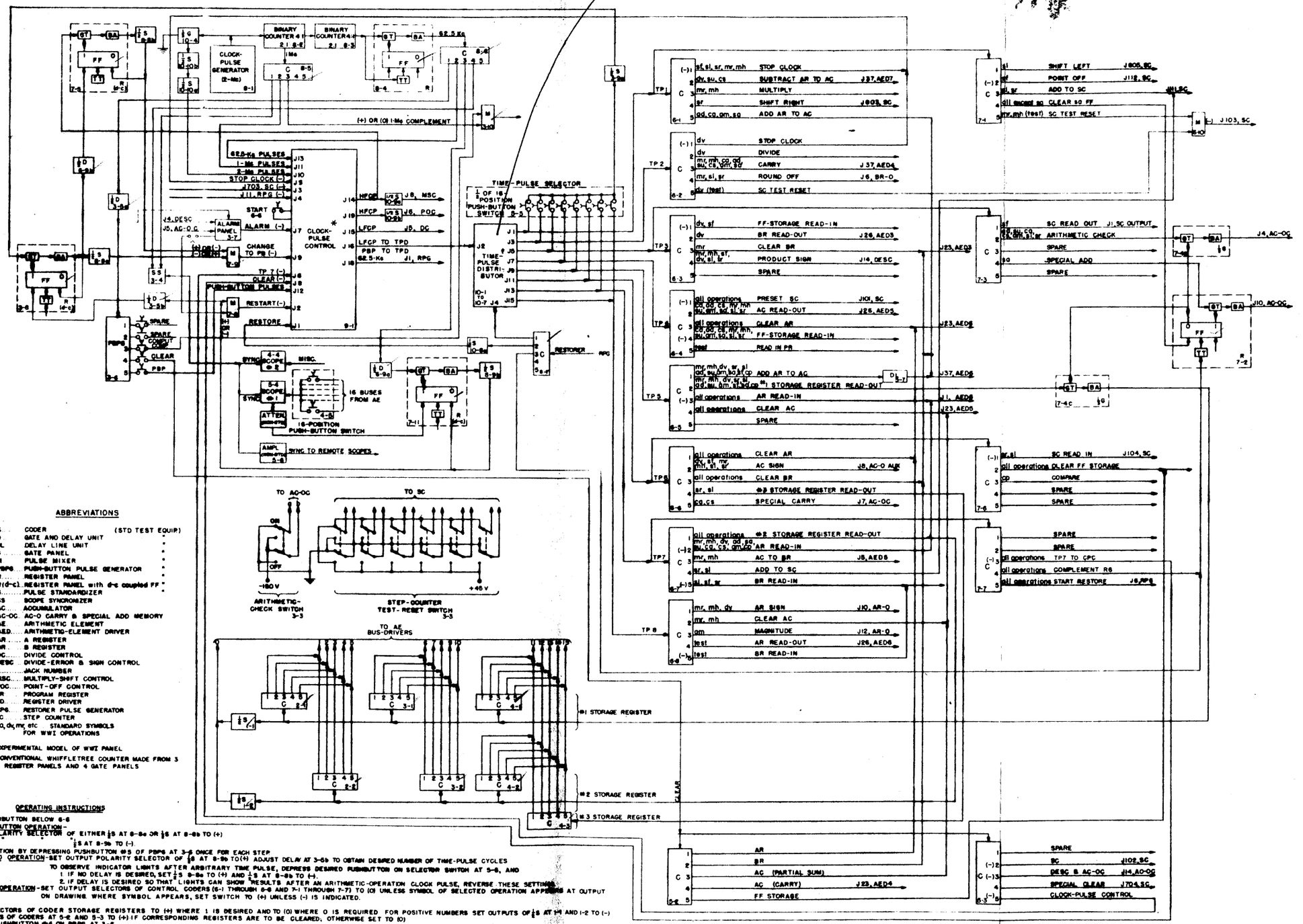
F644

B-33500

B-33521-1

E-33028-2

later made from 17 gates + 3 flip flops



ABBREVIATIONS

C	CODER	(STD TEST EQUIP)
D	GATE AND DELAY UNIT	*
DL	DELAY LINE UNIT	*
G	GATE PANEL	*
M	PULSE MIXER	*
PBPB	PUSH-BUTTON PULSE GENERATOR	*
R	REGISTER PANEL	*
R(d-c)	REGISTER PANEL with d-c coupled FF	*
S	PULSE STANDARDIZER	*
SS	SCOPE SYNCRONIZER	
AC	ACCUMULATOR	
AC-OC	AC-O CARRY & SPECIAL ADD MEMORY	
AE	ARITHMETIC ELEMENT	
AED	ARITHMETIC-ELEMENT DRIVER	
AR	A REGISTER	
BR	B REGISTER	
DC	DIVIDE CONTROL	
DESC	DIVIDE-ERROR & SIGN CONTROL	
J	JACK NUMBER	
MSC	MULTIPLY-SHIFT CONTROL	
POC	POINT-OFF CONTROL	
PR	PROGRAM REGISTER	
RD	REGISTER DRIVER	
RPG	RESTORER PULSE GENERATOR	
SC	STEP COUNTER	
CG, dv, mr, etc	STANDARD SYMBOLS FOR WWI OPERATIONS	

* EXPERMENTAL MODEL OF WWI PANEL

† CONVENTIONAL WHIFFLETREE COUNTER MADE FROM 3 REGISTER PANELS AND 4 GATE PANELS

OPERATING INSTRUCTIONS

I START - DEPRESS PUSHBUTTON BELOW 6-6

II STEP-BY-STEP PUSHBUTTON OPERATION -
1. SET OUTPUT POLARITY SELECTOR OF EITHER ½S AT 8-8a OR ½S AT 8-8b TO (+)
2. " " " " ½S AT 8-9b TO (-).
3. PERFORM OPERATION BY DEPRESSING PUSHBUTTON #5 OF PBPB AT 3-6 ONCE FOR EACH STEP

III CYCLICAL HIGH SPEED OPERATION - SET OUTPUT POLARITY SELECTOR OF ½S AT 8-9b TO (+) ADJUST DELAY AT 3-5b TO OBTAIN DESIRED NUMBER OF TIME-PULSE CYCLES

TO OBSERVE INDICATOR LIGHTS AFTER ARBITRARY TIME PULSE, DEPRESS DESIRED PUSHBUTTON ON SELECTOR SWITCH AT 5-5, AND
1. IF NO DELAY IS DESIRED, SET ½S 8-8a TO (+) AND ½S AT 8-8b TO (-).
2. IF DELAY IS DESIRED SO THAT LIGHTS CAN SHOW RESULTS AFTER AN ARITHMETIC-OPERATION CLOCK PULSE, REVERSE THESE SETTINGS.

IV SELECT ARITHMETIC OPERATION - SET OUTPUT SELECTORS OF CONTROL CODERS (6-1 THROUGH 6-8 AND 7-1 THROUGH 7-7) TO (0) UNLESS SYMBOL OF SELECTED OPERATION APPEARS AT OUTPUT ON DRAWING WHERE SYMBOL APPEARS, SET SWITCH TO (+) UNLESS (-) IS INDICATED.

V STORE NUMBER -
SET OUTPUT SELECTORS OF CODER STORAGE REGISTERS TO (+) WHERE 1 IS DESIRED AND TO (0) WHERE 0 IS REQUIRED. FOR POSITIVE NUMBERS SET OUTPUTS OF ½S AT 1-1 AND 1-2 TO (-)

VI CLEAR 1. SET OUTPUTS OF CODERS AT 5-2 AND 5-3 TO (+) IF CORRESPONDING REGISTERS ARE TO BE CLEARED; OTHERWISE SET TO (0)
2. DEPRESS PUSHBUTTON #4 ON PBPB AT 3-6.

NOTE: PHYSICAL LOCATION OF EACH UNIT IN TEST EQUIPMENT SETUP IS GIVEN BY SYMBOL IN BLOCK; e.g., 7-5a INDICATES THE UPPER (OR LEFTMOST) CHANNEL OF THE 5TH UNIT FROM THE TOP OF THE 7TH RACK FROM THE LEFT

DRAWING REFERENCE: E-32174

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
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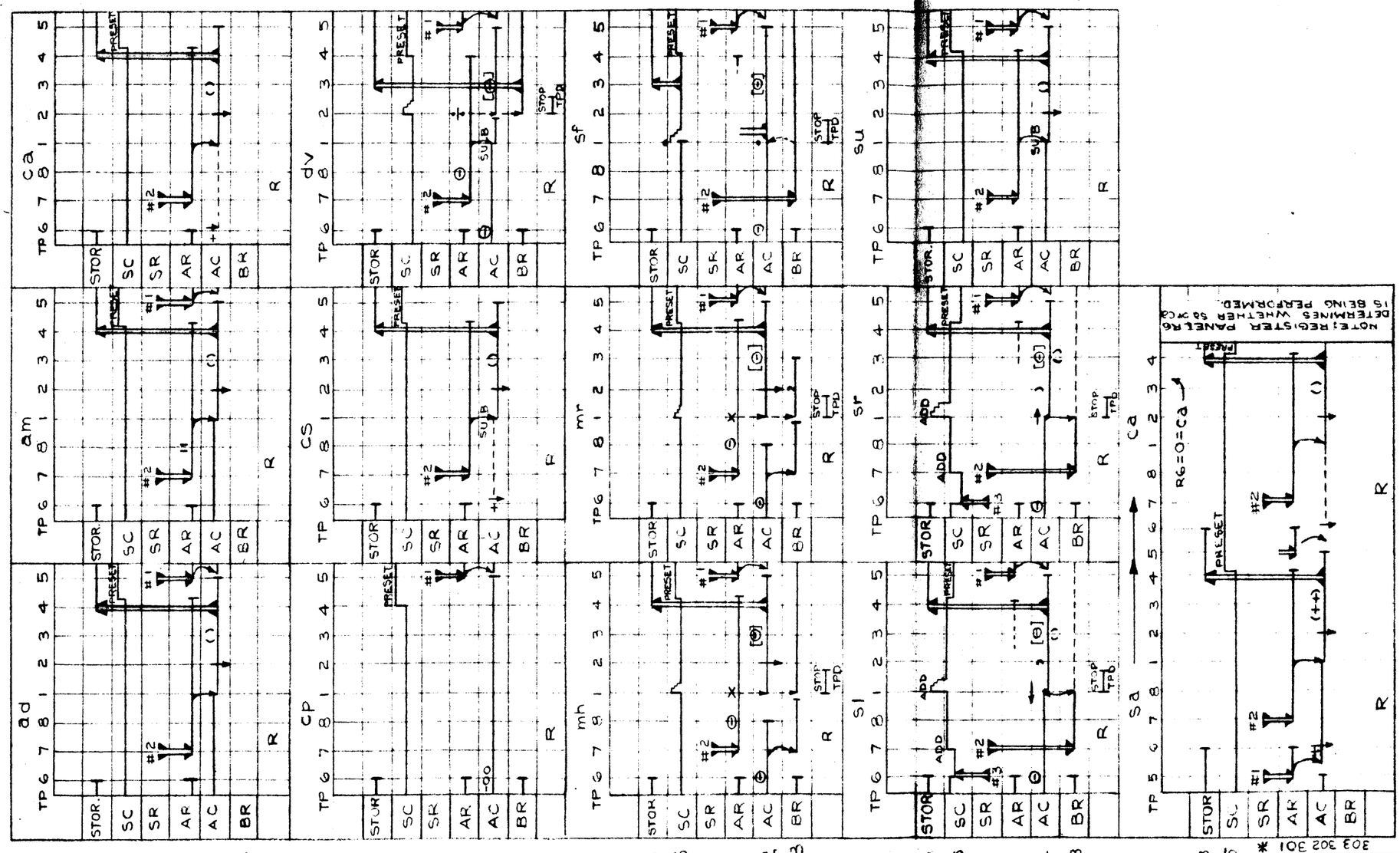
SYSTEM FOR TESTING
WWI ARITHMETIC ELEMENT

AGARTS 12-6-48

E-33028-2

B-33500



DATA PRESENT
AC (4AR) SIGN CHECK
PRODUCT SIGN CHECK
MAGNITUDE
COMPARE
BUS USED
MULTIPLY
SHIFT LEFT
SHIFT RIGHT
DIVIDE

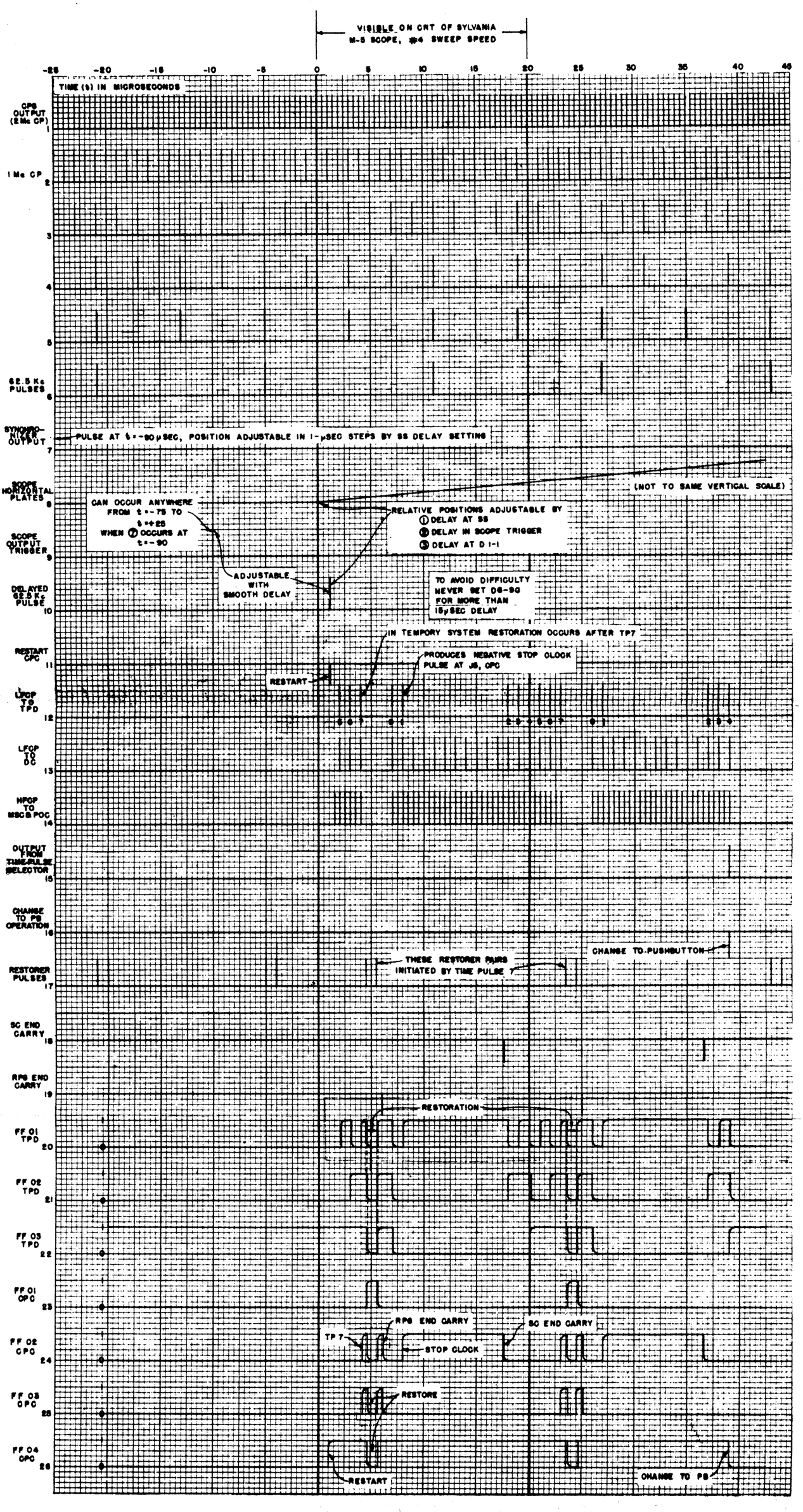
SYMBOLS USED:

* TOGGLE SWITCH
STORAGE REGISTER
\# FLIP-FLOP
STORAGE REGISTER
RESTORE
CLEAR
CARRY
SPECIAL CARRY
ARITHMETIC CHECK
SPECIAL ADD
ROUNDOFF
TRANSFER

SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

TRAFFIC SCHEDULES FOR OPERATION OF ARITHMETIC ELEMENT WITH TEST CONTROL

SCALE:	DR. M. Matas - 2-4-49	B-33500
ENG. 3/11/49	CK.	APP.



MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6346

TIMING FOR TEMPORARY CONSOLE

SCALE

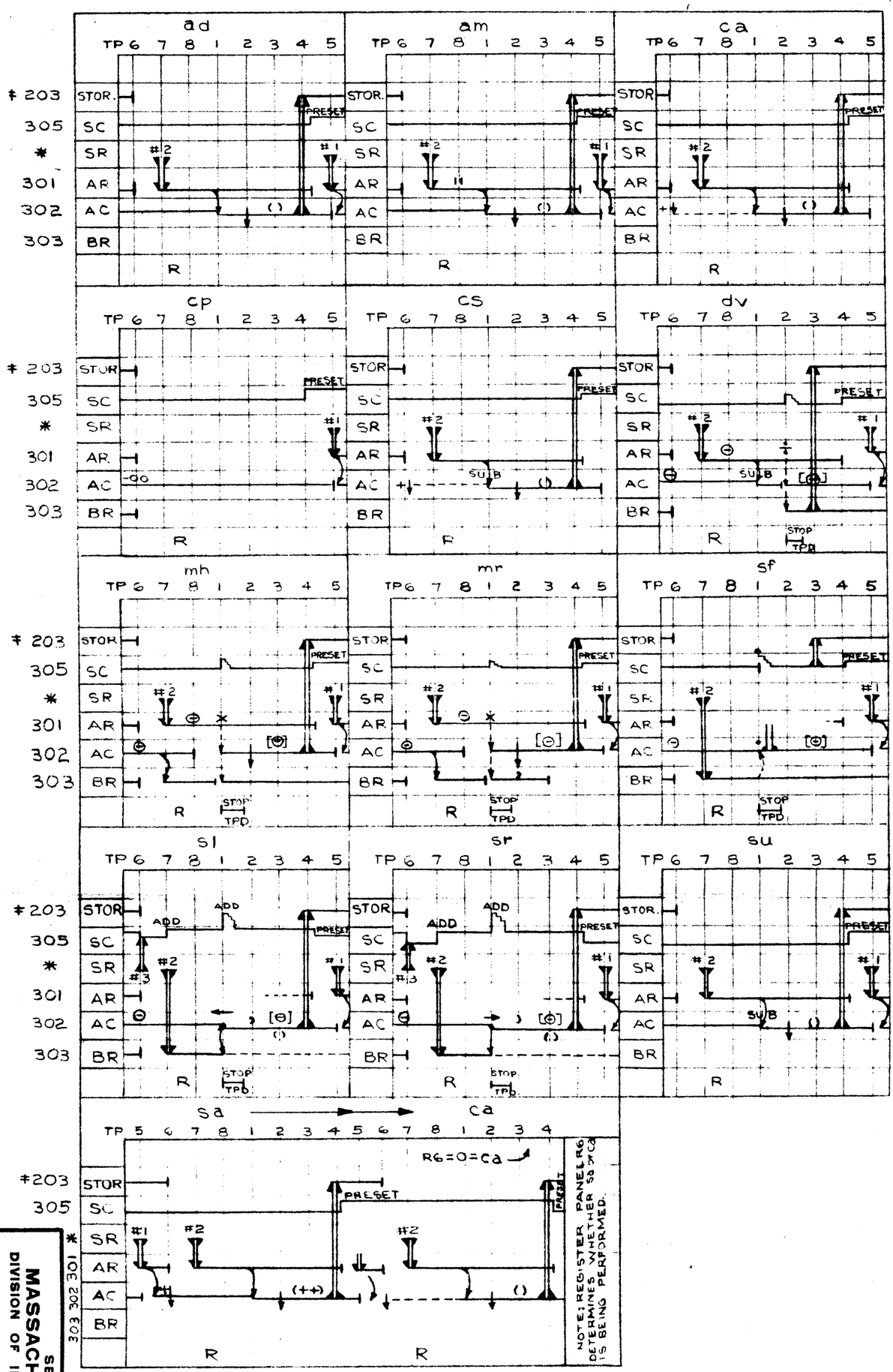
DRN. [illegible] DATE 6-11-56

CHK. [illegible] DATE

B-33521-1

B-33521-1

B-33500



SYMBOLS USED:

* TOGGLE SWITCH STORAGE REGISTER---: SR

\# FLIP-FLOP STORAGE REGISTER --: STOR

RESTORE ----------: R

CLEAR ----------: ——|

CARRY ----------: ↓

SPECIAL CARRY ----------: +↓

ARITHMETIC CHECK -----: ( )

SPECIAL ADD ----------: (++)

ROUNDOFF ----------:)

TRANSFER ----------: ⤵

DATA PRESENT ----------: ——

AC (&AR) SIGN CHECK -----: ⊖

PRODUCT SIGN CHECK ----: [⊖]

MAGNITUDE ----------: ||

COMPARE ----------: -oo

BUS USED ----------: ⊥

MULTIPLY ----------: ×

SHIFT LEFT ----------: ←

SHIFT RIGHT ----------: →

DIVIDE ----------: ÷

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

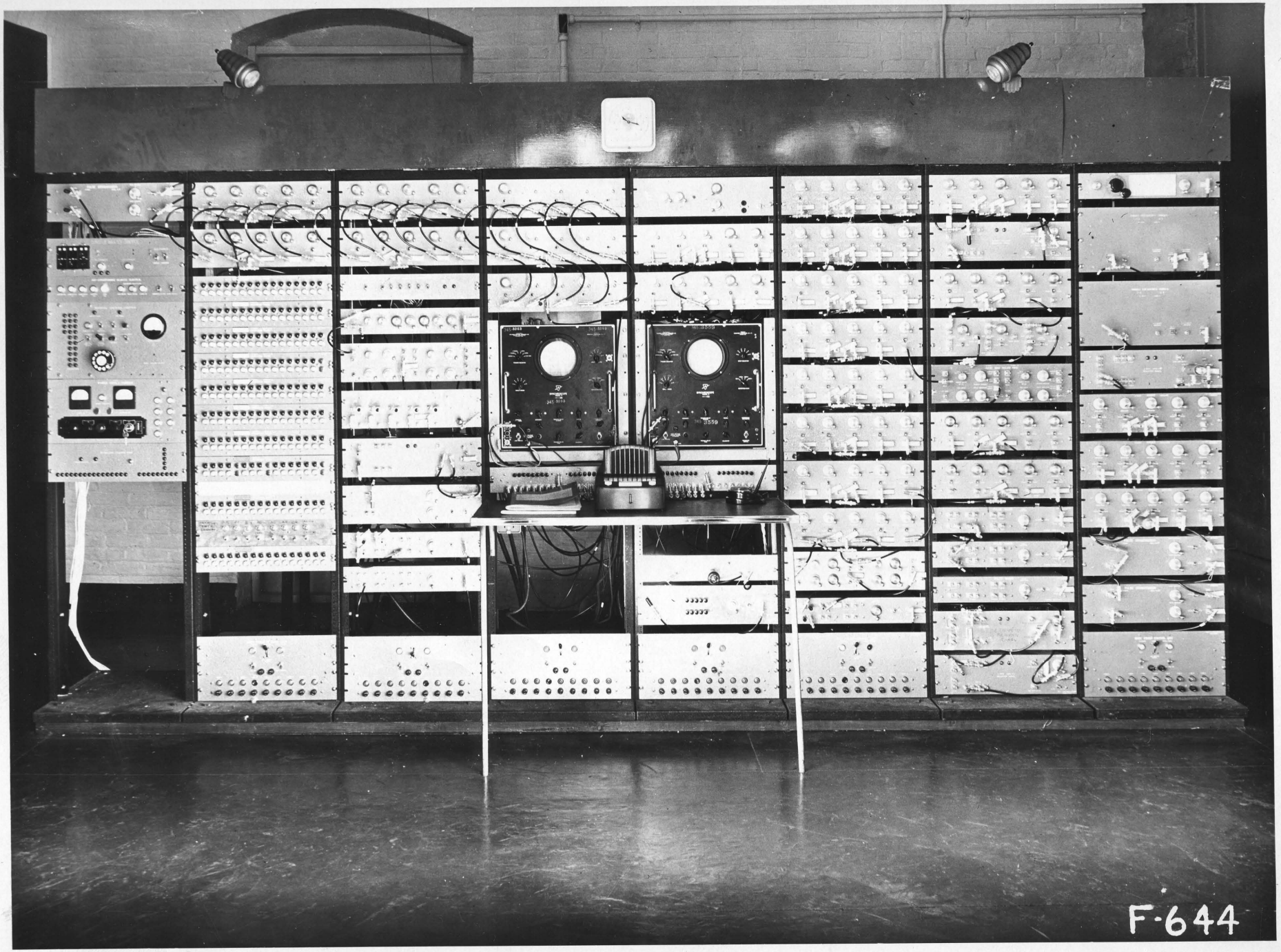
TRAFFIC SCHEDULES FOR OPERATION OF ARITHMETIC ELEMENT WITH TEST CONTROL

ENG.	CK.	DR. M. Matas 2-4-49	APP.
RMH 2/11/49			

SCALE:

B-33500

A-33653



WWI TEST CONTROL