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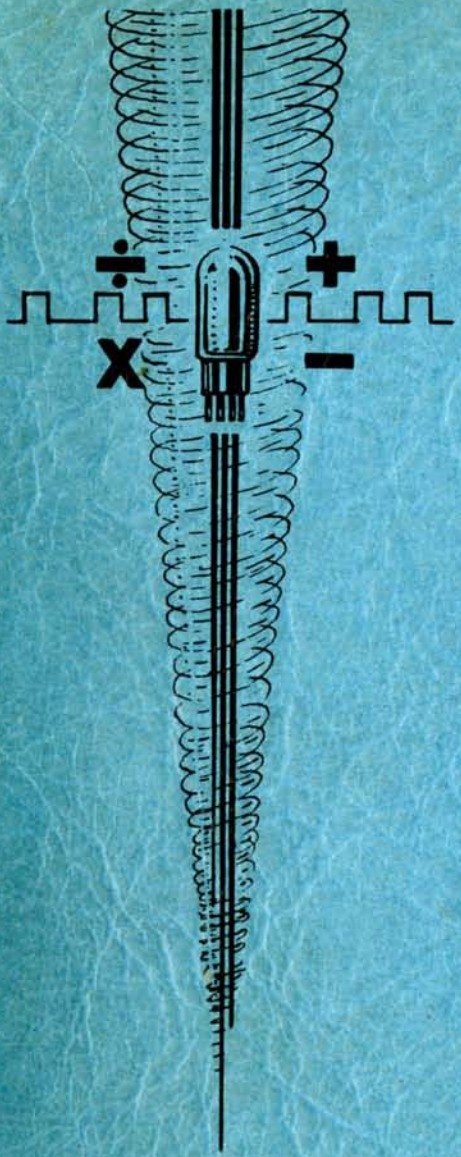

PROJECT WHIRLWIND

Contract N5ori60
Project NR-720-003

R-134

THE FIVE-DIGIT MULTIPLIER

DECEMBER 3, 1948

VOLUME 1

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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PROJECT WHIRLWIND

Report R-134

FIVE-DIGIT MULTIPLIER

Volume 1 of 2 Volumes

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FOREWORD

This report is a description of the first high-speed multiplier developed at the Servomechanisms Laboratory of MIT for the Project Whirlwind program. It records the high points in the development of the machine, and is intended to acquaint the reader with many of the electronic problems which confront the designer of a high-speed digital computer. In order to facilitate reference, the text is contained in Volume 1 and the illustrations in Volume 2.

The writer wishes to acknowledge the cooperative efforts of all members of Project Whirlwind who devoted their time and energy to make the multiplier program a success. The valuable assistance of George Sumner and Norman Daggett is especially appreciated.

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THE FIVE-DIGIT MULTIPLIER

1. INTRODUCTION

1.1 Problems in Realizing an Electronic Computer

In the development program of such a large and complex system as an automatic digital computer, there is a tremendous gap between a block-diagram outline of the over-all system, such as presented in R-127,[5*] and the realization of a physical system which will actually perform computations. The five-digit multiplier was built to help bridge that gap.

A study of the various functions necessary in an electronic digital computer indicates that four types of problems are of particular interest: the storage problem, the input-and-output problem, the multiple-channel-switching problem, and the arithmetic problem. Before construction of Whirlwind I could be definitely planned, these problems had to be investigated thoroughly and prototype equipment built.

Design and construction of the five-digit multiplier was the result of experimentation with the last, the arithmetic problem. In its entirety, the arithmetic problem covers the operations of adding, subtracting, multiplying, and dividing. It also includes such functions as checking the transfer of numbers and orders.

WWI will have circuits for all these arithmetic duties. However, since the electronic circuits and techniques are similar in each, the solving of the multiplication process by the five-digit multiplier will essentially indicate the solution of the others.

* Superscripts refer to numbered bibliography, Appendix VI.

1.2 Aims of the Multiplier Project

The multiplier project was undertaken with several distinct aims in mind. The first and most significant aim is to determine the optimum multiplication speed obtainable using present electronic techniques. Since optimum multiplication speed is closely associated with storage access time, these two factors will determine the limiting speed in the final computer design.

The answers to other questions concerning future computer work are likewise pertinent aims of the multiplier project:

Is the parallel method of design as outlined in Report R-127 a reasonable and practical approach to this problem of high-speed computation?

Will the basic circuits perform successfully when tied together in a system?

What unforeseen problems of stability, noise, crosstalk, and tube reliability may become stumbling blocks in the realization of a final machine?

1.3 General Description of the Five-Digit Multiplier

The major unit component of the five-digit multiplier is an arithmetic element, prototype of 5 digits of the arithmetic element of WWI. Three other units are used with the arithmetic element: the arithmetic-element control, toggle-switch storage, and an indicator panel.

The arithmetic element is composed of three registers: the A-register, the accumulator, and the B-register.

The arithmetic-element control provides a switch for manual or automatic operation, and push buttons for pulsing the machine. It also

contains a step counter which is used to count the number of shifts during a multiplication and shut off the machine when the correct number of shifts has been made.

Toggle-switch storage has 2 five-digit toggle-switch storage registers from which numbers may be read into the A-register and B-register.

The indicator panel holds an array of indicator lights connected to each flip-flop of the A-register, accumulator, and B-register. When a light is glowing, it indicates that the associated flip-flop contains a 1.

Figure 1 illustrates the functional relationship of these units.

1.4 Machine Performance

After the multiplicand has been read into the A-register and the multiplier into the B-register, the machine is able to perform a multiplication automatically in 5 microseconds. This is accomplished mathematically by a series of shifts and additions, and electronically by using a series of 0.1-microsecond pulses at a 2-megacycle pulse repetition frequency. The answer is then displayed by the indicator lights of the accumulator and B-register. All these operations are explained in detail in Section 3, Section 4, and Appendix IV.

2. BINARY MULTIPLICATION

The binary number system was selected for Whirlwind computers in preference to the decimal system because of its adaptability to electronic circuits. Therefore, in order to understand fully the problems of designing the electronic medium of the five-digit multiplier, it should prove helpful to the reader if a discussion of the nature of binary multiplication is presented at this point.

In the binary system, our familiar longhand method of multiplication is simply a series of additions. These additions occur as one of the following three numerical combinations:

0	0	1
0	1	1
0	1	10

Adding Binary Numbers

To multiply two binary numbers, the multiplicand is added in for every digit of the multiplier which is a 1, while 0's are added when the multiplier digit is a 0. It may be noted in the example below that each partial product is shifted one digit to the left under the preceding partial product as in decimal multiplication before being added to produce the complete product.

110	multiplicand
101	multiplier
110	first partial product
000	second partial product
110	third partial product
11110	complete product

Binary Multiplication

If a machine were to perform multiplication in this manner, it would have to be able to distinguish a 0 from a 1 in every digit of the multiplier and be instructed to add in either the multiplicand or a set of 0's. It would also have to shift left at the proper time and add the partial products. The process is not impossible electronically, but it constitutes a rather long computing time and involves many electronic components. Accordingly, a modified method of multiplication is used. Instead of expecting the machine to inspect the entire multiplier, we ask it to examine only the right-most digit. We then let the machine "throw away" the examined digit, shift the multiplier one digit to the right, and examine the new right-most digit. Rather than add in 0's as we did in the longhand method whenever the multiplier digit was a 0, we allow the machine to shift the partial product one digit to the right. Offhand this method might appear more complicated than the conventional one. Actually the machine has to use only a single circuit to examine the right-most digit of the multiplier, another simple circuit to shift each digit to the right, and a device known as the step counter to tell when to stop. Throwing away of the used digits, reserves space in the B-register of the machine for part of the answer.

The modified method is accomplished mathematically as follows:

(1) Examine the right-most digit of the multiplier. If it is a 1, add the multiplicand in as a partial product and then shift the multiplier and partial product 1 digit to the right, throwing away the used multiplier digit. If it is a 0, shift the multiplier and throw away the used digit.

(2) Examine the new right-most digit of the multiplier. If it is a 1, add the multiplicand to the shifted partial product (considered all

0's if the first right-most digit of the multiplier was a 0), obtaining a second partial product. Shift the new partial product and multiplier one digit to the right. If it is a 0, shift the partial product and multiplier one digit to the right.

(3) Perform successive shifts and additions until all the digits of the multiplier have been used.

The next example illustrates multiplying two longer numbers by the modified method:

0111	multiplicand
1101	multiplier
0111	partial product
0111	multiplicand
110	shifted multiplier
0111	shifted partial product
0111	multiplicand
11	shifted multiplier (2nd shift)
0111	shifted partial product (2nd shift)
0111	multiplicand added in
100011	second partial product
0111	multiplicand
1	shifted multiplier (3rd shift)
0100011	shifted 2nd partial product
0111	multiplicand added in
1011011	answer

Modified Multiplication

In the example above, whenever two 1's were added, a 0 was produced and a 1 was shifted mentally to the left as a carry. If the next column to the left contained 0, the carry was added in directly. If it contained a 1, the carry was added to the 1, giving a 0 and producing a second carry to be shifted. This process was continued until all carries were added. Since the machine is not capable of shifting carries mentally, we must consider a step-by-step process which the machine can perform. The

following illustration shows how multiple carries are handled for the last steps in the previous example.

0111	shifted partial product (2nd shift)
0111	multiplicand added in
1	carry
011011	
1	carry
010011	
1	carry
000011	
100011	second partial product
0100011	shifted second partial product
0111	multiplicand added in
1	carry
0011011	
1011011	answer

Multiple Carry

It may be seen in the example of modified multiplication that shifting and adding are the primary requirements, and also that 4 carry additions are necessary in order to get the complete answer in the example of multiple carry. However, in machine solving, after the first carry operation, the circuits containing the partial product and carry are in a position to accept a second number for addition; that is, a given partial-product digit and its associated carry digit to the left together never hold more than a single 1 after shift and carry, and another addition may be performed before both could hold 1's. Thus a partial carry will suffice for the successive additions during a multiplication, and the complete carry may be deferred until the end of the process. For example, starting at the same point as we did in the illustration of multiple carry we follow these steps:

(1) Add and obtain the first carry.

(2) Shift the carry and partial product one digit to the right.

(3) Add in the multiplicand, obtaining a new partial product and new carry.

(4) Perform a high-speed complete carry and obtain the answer.

	0111	
	0111	
Step 1	(001000	carry
	(011011	partial product
Step 2	(0001000	shifted carry
	(0011011	shifted partial product
Step 3	(0111	multiplicand added in
	(0111000	new carry
Step 4	(0100011	new partial product
	(1011011	high-speed carry and answer

Shift and Carry

In the above example, a partial carry was performed and then the partial carry and partial product were shifted before the next addition. Although this eliminates the necessity of the second and third carry operations and could be accomplished electronically without any difficulty, the two steps still consume much computing time. To increase computing speed, Whirlwind I circuits combine the two operations into one called, "shift and carry". This operation is explained fully in the discussion of the whiffletree circuit in Appendix V.

The final step is a high-speed carry which adds each number of the carry directly into the partial product to obtain the answer. Whenever a 1 in the partial product is encountered during addition, the carry is propagated to the left until it finds a 0, changing the 1's in the partial-product to 0's as it goes.

Further investigation of the mathematical process of shift and carry will show that four possible combinations may result in a carry and partial-product column after two numbers are added. In the example

below, two seven-digit binary numbers, 0111000 and 0011010, have been added to produce the carry and partial product shown. Each carry digit is the result of addition occurring to its right. The columns in which the four combinations mentioned appear have been circled for reference.

Columns:	1	(2)	(3)	4	(5)	(6)	7
carry	0	1	1	0	0	0	
partial product	0	1	0	0	0	1	0

Carry and Partial-Product Combinations

If we shift the carry digits and partial product one column to the right (A) and then add in the carries (B), the above numbers take the following form:

		1	(2)	(3)	4	(5)	(6)	7	8
(A)	carry	0	0	1	1	0	0	0	
	partial product	0	0	1	0	0	0	1	0
(B)	carry	0	1	0	0	0	0	0	
	partial product	0	0	0	1	0	0	1	0

Shift Right and Carry

Let us now examine the circled digit columns in both examples. In column 2, the carry and partial-product combination, 1/1, becomes 1/0 after shift and carry (B). The carry is left at 1 while the 1 in the partial-product is cleared and a 0 shifted to the right. In column 3, the 1/0 combination becomes 0/0; the 1 in the carry is shifted right into

column 4 of the partial product. In column 5, 0/0 remains 0/0, shifting a 0 to the right in column 6. The 0/1 in column 6 becomes 0/0 and a 1 is shifted right.

The four conditions of shift and carry in Whirlwind computer circuits are the same as those shown above and may be learned easily by following this rule of thumb: If the combination of the carry flip-flop (carry digit) and accumulator flip-flop (partial-product digit) in the same column is 0/0, shift a 0 to the right in the partial product. If the combination is 0/1 or 1/0, shift a 1 to the right and clear. If a 1/1 exists, shift a 0 to the right, leave the 1 in the carry, and clear the partial product.

3. HISTORY OF THE MULTIPLIER PROJECT

3.1 Shift-and-Carry Function

From the above discussion of multiplication the reader may gather that the shift-and-carry function is somewhat more involved than the other arithmetic functions. This complication is justified only as a means of increasing multiplication speed; therefore, a detailed study of the shift-and-carry problem was selected as the starting point for electronic work on the project.

3.11 Component Circuits

Shift and carry was accomplished initially by using the 4-position matrix switch (Fig. 5). This method, previously outlined in R-127,[5] is described in Appendix I of this report. The basic circuits which were used to design the matrix are the flip-flop (Fig. 3) and the gate circuit (Fig. 4). Appendix I likewise contains a discussion of basic circuits, and Appendix II, methods of coupling.

3.12 The Shift-and-Carry Breadboard

Fig. 2 is a photograph of the breadboard used to test the shift-and-carry matrix. The breadboard provided a means of studying the four conditions of shift and carry mentioned in Section 2, Binary Multiplication. The gate tubes in the matrix were switched rapidly by changing the contents of the associated flip-flops. This sequence permitted detailed study of the timing and impedance problems.

The experimental work at this stage of the program made possible several important decisions. The most significant was the establishment

of the maximum frequency for shift and carry. Two megacycles was selected as optimum, resulting in a 0.5-microsecond delay period. This period was employed as follows: the switching time of the system was measured at 0.2 microsecond, the pulse width used was 0.1 microsecond, while the remaining 0.2 microsecond provided a safety margin. Fig. 6 shows the relative placement of pulses in time as a gate circuit of the matrix is switched.

Faster operation was attempted, and successful switching was achieved at a 2.8-megacycle rate. To increase the speed further, heavier tubes and more power dissipation by the crystals were necessary. As crystal reliability is directly related to power dissipation, this plan was abandoned. The decision to operate at 2 megacycles was a compromise to obtain maximum reliability with minimum equipment.

A-C coupling with the use of restorer pulses (discussed in Appendix II) was verified as a practical and useful method to avoid the cascading of power supplies. Its success in the shift-and-carry breadboard was largely responsible for the decision to use a-c coupling in the five-digit multiplier and later in WWI.

3.2 The Control Panel

The function of the control panel is to supply pulses to the arithmetic panels in such sequence as is required to carry out a multiplication. The operations of adding, shifting, clearing, and reading in new numbers are all necessary. Provision must be made for the operator to initiate these pulses by push-button for step-by-step solution or to

call for automatic operation.

Two registers of toggle-switch storage allow the operator to set up manually the two numbers he desires to multiply, and provision to read these into the A and B-registers is made.

Indicator lights which show the position of each flip-flop in the digit panels are provided so that each step in the solution of a problem may be studied.

A central restorer line capable of restoring the whole multiplier is on this panel, and the necessary line drivers to take the control pulses to the five digits are also included.

The block schematic, Fig. 16, shows the separate channels which perform each of these functions. The circuit schematic, Fig. 9, includes the wiring of the indicator lights.

Fig. 7 is a photograph of the panel. In this illustration, the indicator lights of the accumulator and B-register show the solution to the problem 31 x 31 --- 961. The A-register still holds the multiplicand 31.

Most of the circuits are conventional; however, the method of obtaining a single pulse for push-button operation using a switch tube, 2D21 thyratron, is of interest and is presented in Appendix III.

3.3 Mechanical Aspects of Design

In considering the many possible physical arrangements of parts for the multiplier panels, it was decided that ease in trouble analysis, accessibility, and good video-layout techniques should take precedence over compactness or appearance. This decision was made to affect WWI

as well as the multiplier panels. Accordingly the design of a single-digit multiplier panel comprising the A-register, B-register, and accumulator was made with the tubes mounted horizontally in the rear and circuits laid out on the front of the panel. Fig. 10 shows the prototype panel used to test the mechanical and electrical design. Video cables were installed close to the particular tube with which they function to minimize possible crosstalk problems.

Exhaustive testing of the prototype assured that this type of layout was adequate for high-speed circuits. No relaxation of performance requirements was necessary between the breadboard and this prototype panel.

The final panels of the five-digit multiplier, Fig. 11 and Fig. 12, differ only slightly from the prototype. They were constructed and tested by Sylvania Electric Products, Inc., Boston, Massachusetts. A sixth rack contains the necessary control apparatus, indicator lights, two registers of toggle-switch storage, and step counter (Section 3.2). Each of these six racks has its own power distribution panel with associated fuses and relay interlocking circuits.

3.4 Systems Operation (Refer Fig. 14A, Fig. 14B, Fig. 15 for typical circuits)

3.41 Five-Digit Multiplier as a System

When functioning as a multiplier, the five digit panels of this system are activated by pulses from the control panel. Control is a means of distributing pulses to the proper location at the proper time. To accomplish this, test equipment must provide pulses for control. The test equipment needed to run a system such as the five-digit multiplier

was not available at the start of the project, and considerable effort has been expended to develop adequate circuits. A history of the systems operation, in fact, closely parallels a history of test equipment required to actuate it.

The preliminary studies of restoring the system made use of the restorer pulse generator, which gives two pulses each 10-microsecond period when supplied with 1-megacycle clock pulses. These restorer pulses were amplified and distributed by the buffer in the control panel.

Systems operation was successful first at the push-button rate and soon afterwards at a clock frequency of 100 kc. In the latter case, a second restorer generator providing a single pulse in each restorer interval was used as a clock-pulse source. Very little trouble was experienced in operating at this rate, beyond the routine problems due to wiring errors and a few design omissions.

Increasing the frequency to 1 megacycle, however, created a test-equipment problem. At this rate it was necessary to gate out clock pulses during the period of restoration to avoid the possibility of a control pulse being sent out at that time. The arrangement shown in the block diagram, Fig. 13, made this possible and allowed a margin of safety in each side of the restorer period. The crystal-controlled clock fed both 1-and 2-megacycle pulses to the pulse distributor and 1-megacycle pulses to the restorer pulse generator. A single 100-kc pulse from the output of this unit produced a 1.25-microsecond gate by a flip-flop and delay line in the distributor and allowed 2 pulses from the 1-megacycle line to pass along the restorer output line. During this 1.25-microsecond period, the

2-megacycle clock pulses were suppressed by another gate on the same flip-flop.

Using the above test equipment, the multiplier operated at a 1-megacycle rate but required very high amplitude pulses. Increasing the clock rate to 2 megacycles resulted in operation on a rather intermittent basis; nevertheless, a few successful multiplications of five-digit numbers were obtained.

From this experience, it was apparent that existing techniques and tools were inadequate for the task, and again more test equipment was indicated. As a result, the periodic-program control panel was designed to repeat each solution at an audio rate; that is, every millisecond a 5-microsecond solution would occur and then hold for 985 microseconds. During the period 985 to 995, the machine was cleared and the multiplicand and multiplier read into the A-and B-registers as described in Section 4. From 995 to 1000 microseconds the solution would recur to complete the cycle. The 985-microsecond delay between problem solutions gave ample time to turn on the indicator lights. The remaining 15-microsecond period was short enough to prevent the lights from being extinguished and permitted the operator to see a continuous display of the problem solution. If any change due to machine error or intermittent solution occurred, these lights would flicker and give warning that all was not well. The photographs of Fig. 17 and Fig. 20 were made using the periodic program panel. The reader will see readily the advantage of this equipment in studying detailed action of flip-flops and gates.

3.42 Design Considerations

The most important single factor in improving multiplier reliability from the original stage to the present was the removal of the circuits' sensitivity to prf variations. Soon after the periodic-program control was available it was found that the circuits using pulse transformers would pass the first pulse of a chain at full amplitude but subsequent pulses would appear at a reduced amplitude. Once this tendency was established, each subsequent tube and transformer would accentuate it; and after 3 or 4 stages, the 3rd and 4th pulse in the chain and all following pulses would be attenuated to a low value.

The cause of the trouble was found to be the failure of a transformer and its load circuit to recover completely from one pulse of energy before receiving another. This load circuit was essentially an LC tuned circuit which oscillated at a frequency of 5 mc, giving a 0.1-positive half-sine wave in the first half-cycle. In the second half-cycle, as the voltage reversed, a crystal came into action and damped out the negative wave, leaving only a positive pulse. This damping was the important problem. In order to keep the time of damping below the 0.5-microsecond limit, an optimum resistor was needed in series with the crystal. For 1:1 transformers, 470 ohms is optimum; for 3:1 units, 390. The photographs of the clock pulses in Fig. 20 show that the results arrived at are satisfactory. Between the first and last clock pulses of each group there is no perceptible decrease in amplitude. The slight overshoot after each pulse returns to the base line does not affect the succeeding pulse.

A second important consideration arose in regard to the four-position crystal switch (Appendix I). In restoration, this switch changes to its complementary state; that is, a 1/1 condition becomes 0/0 and a 1/0 becomes 0/1. In either case, two of the four channels are unaffected and remain closed. The gates of these channels remain closed because they receive no signal from the matrix. This condition is only fulfilled, however, when all four tubes driving the matrix have equal plate currents. Should one tube age sooner than another the change in signal on switching appears as a reduction in bias on the channel held off by a biasing voltage.

It soon became apparent that keeping plate currents equal in tubes of varying duty factors was an impossible task; accordingly this method was abandoned in favor of the whiffletree switch discussed in Appendix V. This method does not require balanced tubes. It has been installed in the five-digit system and proved to be very reliable.

3.43 Tubes

The 6AG7 tube was used in the flip-flop and buffer at the start of the project. This tube deteriorated rapidly, especially in circuits of low duty factor. Investigation indicated that this plate current deterioration resulted from a cathode resistance developing internally. There is some indication that this resistance is due to the formation of an interface on the nickel sleeve of the cathode. Silicon and iron have been detected in the sleeves of those tubes which have shown deterioration, and it is believed that these impurities may be the source of trouble. The Sylvania 7AD7 has been substituted for this 6A67 and to date has exhibited a better life expectancy in low-duty-factor circuits. A

comprehensive treatment of this study is given in Report R-139.[2]

The 6AS6 gate tube was selected as most suitable at the beginning of the project. This tube is proving to be a reliable one. Many of the original tubes are still usable after 5000 hours of operation. The tube, however, has low current capacity and requires the use of a buffer amplifier in many circuits. The Sylvania 7AK7 developed for the project has been substituted in some circuits to avoid these buffers. Present indications of its life expectancy are also favorable. A discussion of the use of this tube including characteristics and data, is available in Engineering Notes E-139.[6]

3.44 Trouble Location

Successful systems operation depends largely on trouble analysis where symptoms are often obscure and diagnosis involved. Considerable effort has been expended to minimize the difficulties in tracing troubles which occur in day-to-day operation. A method of attacking the problem has been developed and its usefulness verified. This method makes use of the step counter. In normal operation the step counter keeps track of the number of shift-and-carry operations which have occurred in a problem. In a five-digit machine, five shifts are always required for multiplication in order to examine each digit of the multiplier. After the fifth shift pulse, the counter gives an end-carry pulse which shuts off the multiply gate and initiates a final end carry. The step counter can be used also as a piece of trouble-location test equipment. If we preset it to different numbers it will stop the problem after any desired number of pulses, and a partial solution of the problem may be examined for error.

It may be connected to count either the shift or add pulses. A partial solution to any multiplication may be obtained and displayed by manually changing the preset number in the step counter. If, in addition, the periodic-program-control is used to repeat these partial solutions, the operator may scrutinize each section of a solution with an oscilloscope. The photographs in Fig. 20 were taken using this equipment.

The method of trouble analysis usually followed is to observe each partial solution and determine which step in the solution is deviating from the correct pattern. By applying the periodic-program control, the operator may tell from a few oscilloscope observations which flip-flop or gate circuit is acting abnormally.

The total sequence has been reduced to the solution of three problems. If any one of these problems is incorrect the first deviation from the correct solution may be found in a matter of minutes using the above method of analysis. This known deviation isolates the trouble to a single gate and flip-flop combination, and in most instances points directly to the trouble.

The three problems which achieve this checking are:

	Problem	AR	BR
(1)	31 x 31	11111	11111
(2)	27 x 19	11011	10011
(3)	2 x 1	00010	00001

Fig. 27 shows which tubes pass or reject a pulse with each step of these problems. As mentioned above, each partial solution serves to isolate the origin of an error and directs the operator to the gate tube or flip-flop causing the trouble.

4. FUNCTIONAL ASPECTS

4.1 Over-All View of the Multiplier

The functional aspects of the multiplier may best be presented by first taking an over-all view of what operator and machine are expected to do, and then following up with the steps involved in solving a typical problem.

Looking at the whole picture, we realize that the multiplier was constructed as a five-digit prototype of the arithmetic element of WWI and that no stress was put upon control. As a result, a simple panel of push-buttons and toggle switches is used to effect operations. Thus the operator must perform duties which will be accomplished electronically in WWI.

Concerning the performance of the machine, we expect it to be able to add, obtain partial products, shift to the right, store and add carries, and supply the correct answer. Finally, we expect it to perform these functions at high speed.

4.2 Illustrations Used

The problem chosen for solution is 25 x 31. To aid in the discussion, three sets of illustrations have been selected. The first represent unit relationship by means of block diagrams. The second and third (Fig. 20) show respectively the different arrays of indicator lights on the control panel for each step in the solution, and the pulse and waveform behavior at as many of these steps as space permits. Scope pictures for clock pulses 5-9 have not been included because it is

believed that typical situations are shown under clock pulses 1-4. The horizontal arrangement of pulses and waveforms is cumulative, however, and the reader may see the entire problem under clock pulse 10 and end-carry pulse. Restorer action is shown throughout the photographs. The reader should not confuse the voltage pedestals between restorer pulses with waveforms caused by clock pulses. In Figure 20, the waveforms and indicator lights are located in clock-pulse columns so that the reader may see what each clock pulse does and, by looking at the column to the left, what condition it found upon arrival. The multiplier uses parallel-digit transmission over a system which provides one channel for each binary digit. However, as it is impractical to show scope pictures of the entire simultaneous process, waveforms have been selected which may be considered typical in all five major units.

Buffer amplifier units and many delay elements have been omitted in the block diagrams to reduce the drawings to the simplest terms. A block schematic of the entire multiplier may be found in Volume II, Fig. 16, for those interested in more than a single-digit view.

4.3 Preliminary Steps

As has been mentioned previously, the operator has to perform several functions which will be programmed and machine-performed in WWI. To simplify the description, let us consider these functions as preliminary steps to the actual problem-solving. They consist of (1) deciding which two numbers to multiply together, (2) converting these from decimal to binary form, (3) throwing toggle switches to place these numbers in the AR and BR storage, (4) clearing the machine of all previous numbers which

may remain, (5) reading the numbers into the AR and BR, (6) checking the indicator lights on the control panel to see if these numbers have arrived in the respective register, (7) ordering the operation to be performed.

Preliminary Steps

(Refer to Fig. 17, Volume II, during steps 4-7.)

Step 1. The two numbers to be multiplied are 25 x 31.

Step 2. Converting these from decimal to binary form we get 11001 and 11111.

Step 3. Place the multiplicand 11001 in the A-register storage and the multiplier 11111 in the B-register storage. To do this, throw the toggle switches of the AR and BR on the control panel (see Figure 7) to the on position for each digit which is a 1. In this example, switches 1, 2, and 5 should be on in the A-register and all switches on in the B-register. Each switch is connected to a read-in gate and when a switch is thrown the gate is opened.

Step 4. Push the clear button. This produces a negative pulse which removes any numbers still in the multiplier from a previous problem by clearing all register flip-flops. The first scope picture in Fig. 17 shows at the left a positive gate formed by pairs of restorer pulses. At the right, the negative pulse clears the flip-flop.

The clear pulse also triggers the clear line to the step counter and presets the counter flip-flops to the binary number 011. Because of the physical arrangement of components in the step counter, numbers are read from right to left and the indicator lights display 110. Each

multiplier is considered as a five-digit number, and five shifts are necessary in order to examine each digit in the right-most position. If the counter is triggered each time a shift occurs, it will contain 111 after the fourth shift. The fifth shift-and-carry pulse can pass through the step counter, become an end-carry pulse and terminate the operation. A description of the step counter is given in Section 4.4 under Clock Pulse 2.

Step 5. Push the read-in button. This control causes a read-in pulse to arrive at each read-in gate whether opened or closed. In Step 3 whenever a 1 was switched into a read-in gate circuit, the gate was opened. The read-in pulse then is able to pass through to the flip-flop in that particular register and set it to a 1 (Fig. 18). Should the read-in pulse arrive at a gate and find it closed, it stops and the flip-flop controlled by that gate remains at 0. In WWI, read-in will be performed more rapidly. All read-in gates of the AR are opened simultaneously by the read-in pulse and numbers are read into the AR from the digit transfer bus.

When read-in is complete, flip-flops 1, 2, and 5 of the AR and all flip-flops of the BR should be set to 1. The waveform picture in Fig. 17 under Step 5 shows a 1 being read into the flip-flop by a positive read-in pulse.

Step 6. To check if the numbers have arrived in the respective registers, make sure that the indicator lights are glowing for each toggle switch in the on position. For this problem, the indicator lights of digits 1, 2, and 5 in the AR and all digits in the BR should check "on" (See Fig. 17,

Step 6). The indicator lights of the step counter should display 11[illegible].

Step 7. Push the multiply button. The action causes a multiply pulse to arrive on the line designated "X" in Fig. 19. This pulse switches the multiply-switch flip-flop which opens the multiply gate. Clock pulses now pass through to gates 1 and 0 of digit 5 of the B-register (BR5). The waveforms in Fig. 17 show the simultaneous actions started by the multiply pulse.

4.4 Problem Solution

The preliminary operations of setting up the problem are now complete. With the multiplier on step control, we are ready to trace what happens to each clock pulse as it passes through the multiply gate and arrives at the 1 and 0 gates of BR.

Fig. 20 has been prepared to help the reader follow the action in detail. Referring to the figure for a moment, we find that clock pulse 1 in the first column of the series of photographs clears BR5, adds 1 to AC1 and AC2, and leaves Carry 1 at 0. Since the first operation is add, no shift-right pulses appear in the 0-to-right and 1-to-right row.

Clock Pulse 1

The first clock pulse approaches both the 1 and 0 gates of BR5 (see Fig. 21) and passes through the 1 gate which was opened when a one was read into the BR flip-flop from toggle-switch storage. This action of the 1 gate in examining the right-most digit of the BR or multiplier is called "sensing".

Once through the 1 gate, the clock pulse becomes an add pulse and arrives simultaneously at all five AC-input gates between the AR and

AC (Fig. 21). As the flip-flops of digits 1, 2, and 5 in the AR contain 1's, their gates are open, and a 1 is added to the associated AC flip-flops. The action of adding a 1 into AC1 and AC2 is shown in the waveforms under clock pulse 1 in Fig. 20.

In addition to becoming an add pulse, the first clock pulse passes back to the flip-flop of BR5 and clears it (BR5 under clock pulse 1, Fig. 20). In the discussion of binary multiplication, this procedure was called throwing away the used multiplier digit.

The panel indicator lights in Fig. 20 show the array of numbers at this point to be:

AR	11001
Carry	0000
AC	11001
BR	11110
Counter	110

Clock Pulse 2

The second clock pulse approaches both the 1 gate and the 0 gate of BR5, and finds the 0 gate open as the first add pulse cleared the flip-flop.

As may be seen in Fig. 21, this pulse becomes a shift-and-carry pulse and performs three important functions:

1. It pulses the shift-and-carry line in the accumulator.
2. It pulses the shift-right line in the B-register.
3. It adds 1 to the step counter.

The indicator lights in Fig. 20 show that the 11001 in the AC

under clock pulse 1 becomes 01100 after the shift-and-carry line is pulsed. No carries were present after the first addition; therefore, the carry register still reads 0000. The 1 in AC5 under clock pulse 1 is shifted to BR1 and the B-register is shifted right to indicate 11111. The step-counter add line is pulsed and the lights change from 110 to 001.

The waveform photographs under clock pulse 2 show BR5 set to a 1, carry 1 still cleared, and a 1 shifted from AC1 to AC2 by the negative 1-to-right pulse.

The three functions initiated by the shift-and-carry pulse are treated fully in Appendix IV.

Clock Pulse 3

Clock pulse 3 is an add pulse. The same action takes place as with clock pulse 1 except that the flip-flops of AC2 and AC3 already contain 1's. When the multiplicand 11001 is added to the partial product, 01100, a 1 is added to a 1 in column 2 producing a carry in column 1. This sequence may be followed in the block diagram, Fig. 16. The indicator array in Fig. 20 now is:

Carry	1 0 0 0
AC	1 0 1 0 1
BR	1 1 1 1 0

The waveforms in Fig. 20 show that clock pulse 3 has set carry 1 and AC1 to 1, and cleared AC2 and BR5.

Clock Pulse 4

The right-most digit of the B-register being sensed as a 0, the 0 gate opens and passes clock pulse 4 as a shift-and-carry pulse. The

shift-and-carry line, shift-right line, and step-counter add line are then pulsed. The resulting action occurs in each digit:

(1) Contents before shift and carry

Carry	1	0	0	0	Counter	0 0 1
AC	1	0	1	0	1	
BR	1	1	1	1	0	
Digit	1	2	3	4	5	

(2) Contents after shift and carry

Carry	1	0	0	0	Counter	1 0 1
AC	0	0	0	1	0	
BR	1	1	1	1	1	
Digit	1	2	3	4	5	

The photographs under clock pulse 4 show that BR5 is set to a 1 by the shift-right pulse, AC2 is left at 0 by the 0-to-right pulse, and AC1 is cleared by the shift-and-carry pulse.

Clock Pulses 5-9

Clock pulses 5 through 9 are alternately add and shift-and-carry pulses and perform functions similar to those described in detail above. The control panel arrays in Fig. 20 indicate the binary numbers in all registers for each step. Particular attention should be given to clock pulse 5 (add) which produces a 1/1 in carry 1 and AC1, a 0/1 in digits 2 and 4; and clock pulse 9 (add) which produces a 1/1 in digits 1 and 4, and a 0/1 in digits 2 and 3.

Clock Pulse 10

This clock pulse becomes a shift-and-carry pulse, pulsing the shift-and-carry line, the shift-right line, and the add line to the step

counter. The latter, set at 111 by the previous shift-and-carry pulse, (clock pulse 8), allows clock pulse 10 to pass through all three gates, clearing the flip-flops of the counter as it goes (Fig. 20).

If the indicator circuits were arranged to obtain a display on the control panel at this point, the register digits would read:

AR	1 1 0 0 1
Carry	1 0 0 1
AC	0 0 1 1 0
BR	0 0 1 1 1

Such indications are not given, however, as another step is combined with shift and carry to give the final answer. Note in the illustration above that the carry flip-flops of digits 1 and 4 contain 1's. The correct answer cannot be obtained until a full carry has been made.

The multiplier performs a full carry in one operation through a high-speed-carry circuit shown in Fig. 26. After the shift-and-carry pulse (clock pulse 10) passes through counter GT3, it becomes an end carry pulse, clears the multiply-switch FF, and also pulses a high-speed-carry line. This line is connected to four high-speed-carry gates, each gate controlled by a carry flip-flop. Fig. 26 shows a typical circuit.

With the carry flip-flop at 0, gate 1 is closed. With the carry flip-flop at 1, the high-speed-carry pulse goes through, clears the carry flip-flop and triggers the input of the AC flip-flop in the same digit. One of two conditions may now exist: the AC flip-flop holds either a 0 or a 1. If it contains a 0, the pulse sets it to a 1. If it contains a 1, the pulse clears it and also travels through gate 2 to the AC flip-flop

next to the left, arriving shortly after a similar operation has been performed in the high-speed-carry circuit there.

Thus, whenever the condition 1/0 exists in the carry and accumulator flip-flops of the same digit, the 1 from the carry is transferred to the accumulator. Whenever 1/1 exists, the 1 from the carry flip-flop goes to the accumulator flip-flop of the next digit left and the AC flip-flop in the same digit changes to 0.

Should a 1 be encountered in the second accumulator flip-flop, the incoming 1 passes again to the left, and the second accumulator flip-flop changes to 0. This occurs until an accumulator flip-flop not holding a 1 is reached. For example, in our problem after the last shift and carry (clock pulse 10) we have:

Carry	1 0 0 1
AC	0 0 1 1 0

High-speed carry gives us:

Carry	0 0 0 0
AC	1 1 0 0 0

In Fig. 20 the photographs under clock pulse 10 and end carry show the complete action of the FF's in BR5, AC2, carry 1, AC1, and indicate the four 0-to-right and one 1-to-right pulses.

4.5 Reading the Answer

The final array of numbers in the indicator lights of the control panel in Fig. 20 is:

AR	1 1 0 0 1
Carry	0 0 0 0
AC	1 1 0 0 0
BR	0 0 1 1 1

The answer appears partly in the AC and partly in B-register as 1 + 2 + 4 (BR) + 256 + 512 (AC) = 775, the B-register holding quantities smaller than 32, and the AC quantities from 32 to 512.

AC	512	256	128	64	32
BR	16	8	4	2	1

5. CONCLUSIONS AND RECOMMENDATIONS

The first phase of the multiplier project has been quite successful. The aims set out in Section 1.2 have been realized, and valuable information has been gained which might have been overlooked had the multiplier project not been undertaken.

An optimum multiplication speed of 2 megacycles has been decided on and verified. The parallel method of computation has been established as practical. Basic circuits have been subjected to systems' requirements, and modifications made where necessary. Tube types which have proved to be inadequate for computer applications have been avoided and circuit changes made which have aided in minimizing the effect of tube deterioration.

One of the most important contributions to the Whirlwind program has been the experience gained through the use of high-speed video circuitry in the multiplier. This background has formed the basis for many decisions in the Whirlwind design.

While the value of high-speed circuitry cannot be overemphasized, realization of the system would not have been possible without perfecting other factors to the same degree of performance. Two major factors were:

1. The test equipment necessary to run a complex system demanded a good proportion of the effort expended on the system itself.
2. The power supplies used with these high-speed computing systems had to be well regulated and isolated from outside disturbances.

These two considerations, significant as they have been in the development

of the multiplier, assume even more importance when one starts to study computer reliability and methods of minimizing computational errors which occur over extended periods of time.

At the time of writing, the multiplier project is entering a second phase aimed entirely at a study of the reliability of computers. There is no doubt that this factor is the most important one in the minds of those who plan to use digital computers, and yet the history of the field contains little evidence that present reliability is adequate for the job.

The five-digit multiplier can contribute valuable information to the fund of knowledge available on the question of computer reliability. To this end, it is recommended that every effort be made to study the existing state of reliability in the multiplier circuits, and that adequate measures be taken to improve the situation by means of marginal checking, improved tubes, and more reliable test equipment as the need arises. The work on this portion of the program has just been started. At present, indications are that considerable effort will have to be expended to isolate those portions of the system causing trouble. These troubles are of the non-recurring isolated variety, and do not point to any particular piece of equipment or location in the computer. The function of marginal checking will be to change these intermittent failures to permanent recurring ones which will make it possible to isolate the sources of the error and correct the cause of it.

The reliability problem, therefore, must receive the same earnest attention as the original multiplier design and testing received. Its

solution is vital if electronic computers are to fill the role which has been outlined for them.

Signed Norman H. Taylor
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Approved
Jay W. Forrester

NHT:RRR:mms

APPENDIX

APPENDIX I

COMPONENT CIRCUITS

The component circuits mentioned in Section 3.11 which were used to design the five-digit multiplier system are discussed in the following paragraphs.

The Flip-Flop[8]

The development of a flip-flop for storing a 1 or a 0 and switching from one state to the other in a minimum time is a fundamental problem in the WWI program. This flip-flop problem is a continuing one, as the reliability and long life of the circuit will determine to a major extent the success of the computer. At the start of the multiplier project, the flip-flop which was available used two 6AG7 tubes in a circuit shown in Fig. 3. This circuit will switch in 0.2 microsecond. It may be complemented in the cathode, or reset on either the 1 or 0 side by pulsing the grids. The output voltage is adequate to open or close gate circuits or to switch channels in a crystal matrix.

The Gate Circuits[1, 11, 17]

The gate circuit provides the channels through which control or signal pulses may pass. The basic requirements are:

1. When opened by its flip-flop on one grid, the gate tube will allow a pulse at another grid topass through.
2. When it is closed, the incoming pulse is rejected.
3. The action of opening or closing the gate must not produce a spurious pulse.

The most satisfactory circuit at the beginning of the project was built around a W.E. 6AS6 gate tube. The circuit in Fig. 4 will pass a pulse when the No. 3 grid is allowed to go to 0 volts with respect to its cathode, and reject a pulse when the No. 3 grid is held below -10 volts. In the multiplier circuit the No. 3 grid is controlled by the signal from the flip-flop. The No. 1 grid, normally biased off, is driven on by incoming pulses. This arrangement provides a favorable duty factor, allowing low screen dissipation.

The 4-Position Matrix Switch[3]

This matrix, shown in Fig. 5, selects one of four gate tubes for each of the four conditions of shift and carry. The buffer amplifiers are necessary to drive the capacitance of the matrix at a rapid switching rate. The resistors R_1, R_2, R_3, R_4 are plate-load resistors for these BA's. The action is as follows: For each of the four shift-and-carry conditions two BA's are conducting. In the 0/0 case, BA1 conducts and draws current through R_3 and R_4. There is no current in R_1 and the potential of line one is at the B + level, all other lines being at a lower level due to the voltage drop in R_2, R_3, and R_4. Line one becomes therefore the selected line and lines 2, 3, and 4 unselected. Gate tube 1 is opened and ready to pass a control pulse. The other three conditions 0/1, 1/0, and 1/1 open gates 2, 3, and 4 in order.

APPENDIX II

COUPLING METHODS

Designing the circuitry for the shift-and-carry function brought into focus the question of coupling between flip-flops, buffers, matrix, and gates. Direct coupling seemed to be indicated, as no limit could be set on the time, whether microseconds or minutes, that a given flip-flop would be asked to hold a given number. Early design efforts clearly indicated, however, that direct coupling would have serious limitations. The regulation requirements of plate power supplies became very stringent, as flip-flop or buffer plate voltage determined the bias of an associated gate tube. To allow for power supply variations and also tube deterioration, considerable overdesign became necessary. This caused power requirements again to increase, and regulation problems became more difficult.

The above problems indicated that a new approach was needed, so the a-c coupling method was conceived. This system makes use of the Germanium crystal in a clamp circuit and provides a method of coupling which is independent of the absolute voltage level of each stage. Cascading power supplies are thereby eliminated.

Most arithmetic operations occur in time spans of from 10 to 50 microseconds, and condensers used to couple adjacent circuits are capable of holding the proper voltage for this period of time. If we restore the small charge which is lost during this period before we start on the next operation, we have achieved an a-c coupling method with no limitation in frequency response.

A simple comparison of the d-c and a-c coupling methods will serve to illustrate.

The D-C Case

In the circuit of Fig. 8(A) a conventional flip-flop is d-c coupled to its gate tube. With V2 conducting, the drop across R2 is large and the voltage at point P is 90 volts. The gate-tube suppressor, d-c coupled to this plate, will likewise be at 90 volts. If now the cathode of the gate is held at 120 volts, the gate will be closed and pulses on No. 1 grid will fail to pass through. When the flip-flop is reversed, V2 does not conduct; the plate voltage rises to approximately 120 volts and the gate circuit is opened to allow pulses to pass.

The A-C Case

By inserting a condenser and crystal as a coupling network between the flip-flop and the gate as shown in diagram B, Fig. 8, it is possible to eliminate the d-c coupling, providing that we supply restorer pulses to the flip-flop at periodic intervals. These restorer pulses (Graph 2, Fig. 8) reverse the position of the flip-flop and then return it to its original position in an interval of 1 microsecond. This process provides a voltage pedestal (Graph 1) on the plate of the flip-flop which passes through the coupling condenser to the grid of the gate tube.

If we use a resistor at this gate-tube grid, the voltage pedestal e_g will appear as in Graph 3. The average voltage developed is 0 volts with no charge accumulating on the coupling condenser. This is not the case when a crystal is substituted for this grid resistor. The crystal will exhibit a resistance value which depends on the voltage across it,

and the coupling condenser will charge more rapidly in one direction than the other. The back-to-front resistance ratio of crystals is high, of the order of 10,000 to 1, and the charge on the condenser accumulates rapidly in one direction.

In the circuit shown, the condenser will develop a negative bias of 30 volts when subjected to the voltage pedestal of 30 volts developed at the flip-flop (Graph 4). This 30-volt bias will effectively cut off the gate tube when its cathode is at ground.

APPENDIX III

PUSH-BUTTON PULSE CIRCUIT

In order to achieve push-button operation, the following requirements must be met:

1. A single pulse must be generated, 0.1 microsecond long and completely independent of the rate of pushing the button.
2. The single pulse must occur at some time after the restorer interval not closer than 0.5 microsecond to a restorer pulse.

Two dual-grid thyratrons, 2D21's are employed. The first receives its plate voltage through a normally closed contact on the push-button switch. When the button is pushed, B+ is removed but a condenser at the plate holds a positive charge. Simultaneously the No. 2 grid is grounded, removing the bias on the tube and putting it in a condition for conduction. Conduction does not occur, however, as the No. 1 grid is biased below cut off. During the next 10-microsecond period, restoration of the system does occur and a sync pulse arrives at the No. 1 grid. The tube now conducts, as both grids are at 0 volts. The duration of conduction is short due to the disconnected B+ . All the energy in the condenser is used to generate a single pulse, satisfying the first requirement.

This pulse now passes thru an RC delay circuit and triggers a second thyratron at a time later than the restoration interval, satisfying the second requirement. The plate of this tube is loaded with a coil and

condenser to produce a pulse in its cathode circuit, which is coupled to an output amplifier for distribution. The output pulse is about 0.1 microsecond in width due to the action of the pulse-forming circuit.

APPENDIX IV

FUNCTIONS OF THE SHIFT-AND-CARRY PULSE

(Refer Page 27)

1. Pulsing the Shift-and-Carry Line

   (a) To shift the partial product one digit to the right.

   (b) To clear partially all carries so that no 1/1 combinations exist, and another addition may be performed without overflowing the capacity of the AC register.

2. Pulsing the Shift-Right Line (Shifting the Multiplier)

All five B-register flip-flops control 1 and 0 output gates. Except in digit 5, which has been examined earlier, these gates are connected to the set and clear inputs of the flip-flop next to the right.

In the problem 25 x 31, when the shift-right line is pulsed, BR1 contains a 1 and the shift-and-carry pulse becomes a 1-to-right pulse. BR2, BR3, and BR4 contain 1's and pass similar pulses. The delay incurred by the gate action in this register is not sufficient for complete clearance of the flip-flops; therefore, a short delay period is added. Simultaneous pulsing of the shift-and-carry line and the shift-right line causes a 1 to arrive in BR1 from AC5 immediately after the former shifts its contents to the right (See Fig. 23). The indicator array in Fig. 20 now shows:

BR 1 1 1 1 1

The waveform under clock pulse 2 also shows that BR5 has been switched from a 0 to a 1. This number is the new right-most digit of the multiplier and indicates that the next operation will be add.

3. Pulsing the Step Counter

The third function of the shift-and-carry pulse is to add 1 to the step counter. Since five shifts are necessary to perform the multiplication, the right-most digit of the multiplier (BR5) is sensed and, if found to be a 0, permits the pulse to pass through the 0 gate and add 1 to the step counter (Fig. 24). When five pulses have been passed by this gate, the counter returns to 0 0 0, an end-carry pulse switches the multiply-switch flip-flop to 0, and the multiply gate is closed to all clock pulses.

The step counter used in the multiplier is composed of three flip-flops and three gates. Their arrangement in block is shown in Fig. 24; the circuit schematic, in Fig. 25.

In order to count five shifts and produce an end carry, the counter is preset to 011 (the lights show 110). The first shift-and-carry pulse finds gate 1 open, passes through, and simultaneously triggers FF1 to a 0. It also finds gate 2 open, passes through, and triggers F2 to a 0. Gate 3 is closed and FF3 is triggered to a 1.

The counter indicator lights now read 0 0 1 (Fig. 20, clock pulse 2).

APPENDIX V

THE WHIFFLETREE

In the discussion of binary multiplication, it was stated that computing speed in Whirlwind circuits is greatly increased by combining the operations of shift and carry. The multiplier does this by means of a circuit known as the "whiffletree" (See Fig. 22). The whiffletree contains four channels to provide for any combination of 0 and 1 in the accumulator and carry flip-flops. The table below which refers to Fig. 22, shows the content of the carry and AC for each channel as the circuit is pulsed, the shift operation effected, and the FFs' content after shifting.

CHANNEL	CARRY CONTENT	AC CONTENT	SHIFT IN AC	FF'S AFTER SHIFT
1	0	0	0 to right	carry 0, AC 0
2	0	1	1 to right	carry 0, AC 0
3	1	0	1 to right	carry 0, AC 0
4	1	1	0 to right	carry 1, AC 0

Whiffletree Channels

Electronically, each channel uses two gates. The AC flip-flop controls the first gate; the carry flip-flop, the second. The following table gives the gates used for each channel in Fig. 22.

CHANNEL	GATES USED
1	B B_1
2	A A_1
3	B B_2
4	A A_2

Whiffletree Gates

Figure 22 illustrates shift and carry in AC1. The shift-and-carry pulse approaches gates A and B, passes through whichever is open.

and arrives at either B_1, B_2, or A_1, A_2. One gate in each combination is open depending upon the content of the carry flip-flop. The pulse passes through to AC2 as either 0-to-right or 1-to-right.

If any 1's exist in the four carry flip-flops when the partial product is shifted, they are added at the time of the shift. Should this result in further carries, these carries are left in the respective carry flip-flops to be added during the next shift.

Referring back to the example 25 x 31, at clock pulse 1, the registers contain:

Carry 0 0 0 0

AC 1 1 0 0 1

Gate A in Fig. 22 is open because the AC1 flip-flop contains a 1. Gate A_1 is open because the carry flip-flop contains a 0. The shift-and-carry pulse follows channel 2, shifting a 1 to AC2 and leaving the carry flip-flop at 0. Under clock pulse 2, Fig. 20, AC1 is now 0, and AC2 contains a 1. The negative pulse at the bottom of the column is the 1-to-right pulse.

The operation of shift and carry is executed similarly in AC2. AC3 and AC4 use channel 1, 0-to-right. AC5 has no whiffletree switch and its shift-right gates are controlled by the AC flip-flop (Fig. 23). Since the number in this flip-flop is a 1, the 1 gate is open. When the shift-and-carry line is pulsed, a 1 is shifted to BR1, where it is stored as the least significant portion of the answer.

The shift-and-carry pulse also goes to a delay element at the same time it pulses the shift-and-carry line. This unit is connected to

to the AC flip-flop of digit 1 only, and clears it after each shift.

With shift and carry completed, the indicator lights in Fig. 20 are as follows:

Carry 0 0 0 0

AC 0 1 1 0 0

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