

THIS MAY HELP WITH THE DECRYPTING!

COMPUTER DEVELOPMENT AT MANCHESTER UNIVERSITY

— DRAFT OF  
MY LOS  
ALAMOS  
PAPER.

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INTRODUCTION

The design of digital computers at Manchester started in late 1946 with the arrival of F C Williams and Tom Kilburn, who were both previously engaged in wartime electronics development at the Telecommunications Research Establishment. The first patent application for Williams Tube electrostatic storage was filed on 11th December, 1946. Williams and Kilburn decided to build a small digital computer - the 'baby Mark I' - to provide a realistic test for their storage invention. The baby machine ran a 52-minute program on 21st June, 1948 and is believed to be the first stored-program computer to come into operation. From August 1948 this prototype was under intense engineering development and the Manchester Mark I working by April 1949 had an enhanced specification including a larger random-access store, a drum backing store and two B-line (index) registers. A further enhancement concerning programmed input/output transfers was introduced in October 1949. The Manchester project began to attract government interest and the firm of Ferranti Ltd. was given support to build a production version of the university prototype. The Ferranti Mark I, delivered in February 1951, is believed to be the first commercially-available stored-program computer.

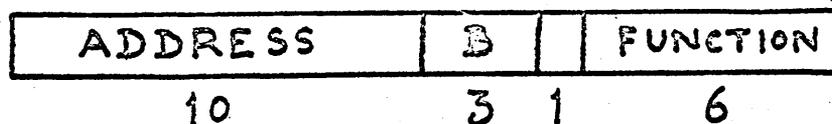
The early days at Manchester were characterised by a relatively small team of about four people working in an environment where electronic components and other resources were difficult to obtain. Significantly, the prototype Mark I was built in the Electrotechnical Laboratories, where an enthusiasm for hardware innovation tended to outweigh any call for a stable computing service. By the end of 1956 the U K National Research Development Corporation held 81 computer patents originating from Manchester. It is very difficult to assess the overall historical impact of the Mark I on computer science development. Certainly, Manchester inventions such as address modification would have been developed sooner or later elsewhere if Williams and Kilburn had never existed. Perhaps of more significance is the ongoing tradition of large machine design and fruitful cooperation with industry which was established at Manchester by the Mark I project. Over the years this has led to the production of five systems of which the latest - MU5 and its industrial counterpart the ICL 2900 range - has recently been commissioned. The fourth Manchester computer was called Atlas. This grew from Kilburn's Muse project, started in 1956. The Ferranti Atlas was developed by a joint University/Ferranti team and at its inauguration in December 1962 was regarded as the most powerful computer in the world. Many Atlas ideas such as virtual storage and paging have made their impact on present-day computer design.

An overall account of computer development at Manchester from 1946 - 76 has been given elsewhere (reference 1). The purpose of this paper is to provide more details of the structure and order code of the Mark I machine. This is described in modern terminology since the original papers and user-manuals are written in an obsolete notation, and in any case are often difficult to obtain. Emphasis has been placed on the production version of the Mark I, because it was the definitive expression of ideas contained in the series of University prototypes commissioned during the period June 1948 to October 1949.

#### Main characteristics of the production Mark I

The Ferranti Mark I was a serial, fixed-point binary computer with a CPU technology based on EF50 (CV1091) and EF55 pentodes, and EA50 vacuum tube diodes (reference 2 - 5). It had a normal word length of 40 bits treated either as a two's complement number or an unsigned quantity, depending on the instruction. The least significant digit was stored on the left - ('backwards binary').

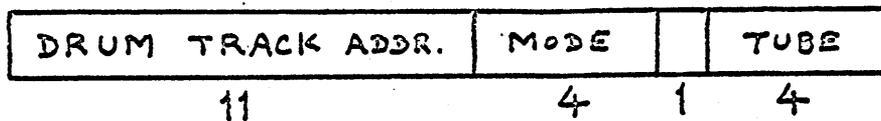
Two 20 - bit instructions were packed to a word, with an instruction format as follows:-



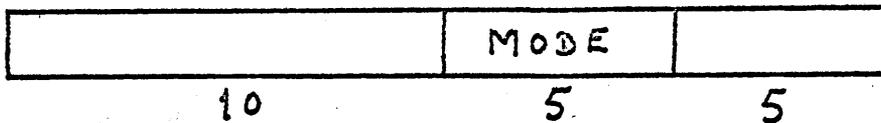
There were eight B - lines (index registers). The main store (random access) consisted of 256 x 40 - bit words arranged as eight 32 - word pages on eight Williams Tubes. Addressing was to 20 - bit boundaries. The main store was backed by 16K (max.) of drum storage. The track-address was stored along with each page of information on the drum, and when a page became resident in main store an extra 20 - bit line was assigned on each Williams Tube to hold the

track-address of that page. (This was the germ of an idea which later led to page-address registers and virtual-to-real address translation of the Atlas computer).

Transfers to and from the drum and other peripheral equipment was carried out via 20 - bit Control Words. These had two formats, distinguished by one of the mode bits. For drum transfers the format was:-



Three mode bits then specified reading/writing, read-checking/write-checking, single page/double page transfers. For input/output transfers the format was:-



Four mode bits then specified : output a character, check output buffer, input a character, send a control character (equal to carriage return, linefeed, figure shift, letter shift) to the output device. Input was via a 250 ch/sec 5 - track paper tape reader and output was to a tape punch and printer.

Central registers in the Mark I were in general implemented via Williams Tubes rather than flip-flops, thus achieving considerable economy. In order to relate to modern terminology the following notation is used when describing their action:-

ACC : the contents of the double-length main accumulator (80 bits)  
 AM : the most-significant 40 bits of ACC  
 AL : the least " " " " "  
 S : the contents of a store line, equal to the full 40 bits except that B orders use the l.s. 20 bits and control-transfer orders use the l.s. 10 bits.  
 B : the contents of a B - line (index register)  
 D : the contents of the multiplicand register (40 bits)  
 H : the digits set up on 20 console handswitches

#### The Mark I order code

The order code of the Ferranti production machine had been specified, except for a few minor details, by November 1949 (reference 6). It is based on the order code for the Manchester University Mark I as it existed in October 1949, since "all the facilities of the University machine shall be reproduced in the Ferranti machine in order that any programmes devised for the existing machine can be transliterated to work with the new machine" (reference 6). In the following list of instructions the mnemonics are intended to suggest present-day equivalent op. codes, whilst the teleprinter characters signify the bit-patterns actually used by Mark I programmers. The 5 - bit teleprinter code, when in letter shift, consisted of the 32 characters:-

/E@A:SIU½DRJNFCKTZLWHYPQOBG"MXV£

and hand-coding was carried out in terms of these symbols (reference 7, 8).

a) Main Arithmetic and logical orders

<u>Mnemonic</u>	<u>Description</u>	<u>Teleprinter</u>
LDA	load ACC (AM cleared)	T/
LDAS	load ACC, sign-extend into AM	T½
LDN	load ACC negatively	TF
STA	store AL	/S
STM	store AM	/E
STMC	store AM and clear AM	/A
SWAP	interchange AM and AL	/I
STAM	store AL, move AM to AL and clear AM	/U
STAC	store AL and clear ACC	TA
CLR	clear ACC	T:
ADD	$ACC' = ACC + S$ (signed S)	TC
ADDU	$ACC' = ACC + S$ (unsigned S)	TI
SUB	$ACC' = ACC - S$ (signed S)	TN
ADDM	$AM' = AM + S$	/J
LDDU	load D (unsigned multiplicand)	/C
LDDS	load D (signed multiplicand)	/K
MADU	$ACC' = ACC + D \times S$ (unsigned S)	/N
MADS	$ACC' = ACC + D \times S$ (signed S)	/F
MSBU	$ACC' = ACC - D \times S$ (unsigned S)	/½
MSBS	$ACC' = ACC - D \times S$ (signed S)	/D
AND	$ACC' = ACC \& S$ (S sign-extended)	TR
ORA	$ACC' = ACC \text{ or } S$ (S sign-extended)	TD
NEQ	$ACC' = ACC \neq S$ (S sign-extended)	TJ
SHLS	$ACC' = 2 \times S$ (arithmetic shift)	TK
ORS	$S' = AL \text{ or } S, = AL$	TE
ORSC	$S' = AL \text{ or } S, \text{ then clear ACC}$	TS

b) B - line (index-register) manipulation

<u>Mnemonic</u>	<u>Description</u>	<u>Teleprinter</u>
LDB	load a specified B - line	TT
STB	store a specified B - line	TZ
SUBB	$B' = B - S$	TL
LDBX	load a B - line (without modification)	TO
STBX	store a B - line (without modification)	TB
SBBX	$B' = B - S$ (without modification)	TG

c) Control transfer orders

<u>Mnemonic</u>	<u>Description</u>	<u>Teleprinter</u>
JMPA	absolute indirect unconditional jump	/P
JMPR	relative " " "	/Q
JGEA	if $ACC \geq 0$ , absolute indirect jump	/H
JGER	if $ACC \geq 0$ , relative " "	/M
JGBA	if (last-named B - line) $\geq 0$ , abs. indir. jump	/T
JGBR	if (last-named B - line) $\geq 0$ , rel. " "	/O

d) Peripheral and miscellaneous orders

<u>Mnemonic</u>	<u>Description</u>	<u>Teleprinter</u>
IOTH	I/O transfer using H as a Control Word	//
IOTS	I/O " " S " " " "	/:
NORM	add to AM the position of the m.s.one in S	/@
SADD	" " " the no. of 1's in S - (population count)	/R
RNDM	load a random number into AL	/W
LDAD	load a page-address word into AL	T@
DST1	debugging stop (1)	/L
DST2	debugging stop (2)	/G

TIME	S' = clock	/Y
HOOT	pulse the console hooter	/V
STH	S' = console handswitches H	/Z
NULL	no operation	T£

In the Mark I programming manual (reference 7) the orders were described by means of short equations. For example:-

<u>teletype code</u>	<u>equation</u>
T/	$A' = \left\{ S_{\pm} \right\} \begin{matrix} 79 \\ 0 \end{matrix}$
TC	$A' = \left\{ A_{\pm} + S_{\pm} \right\} \begin{matrix} 79 \\ 0 \end{matrix}$
/P	$C' = \left\{ S_{\pm} \right\} \begin{matrix} 9 \\ 0 \end{matrix}$

The hardware designers used a simpler notation (see for example references 3 and 4), so that the above three orders would have been expressed as:-

S, A

A + S', A

S, C

(C was the value of Control - i.e., the Program Counter). Thus when Tom Kilburn gave a series of four lectures on the University prototype Mark I (8th - 12th Nov. 1948) the following handout was provided. (Note that this represents the first version of

the 20 - bit instruction format, before programmed I/O and drum transfers had been added.)

CODE FOR CHARGE STORAGE COMPUTER

<u>Significance as an instruction</u>	<u>Binary Code</u>	<u>Code Form</u>	<u>Decimal Form</u>
s, C	00000	/	0
c + s, C	10000	E	1
s, B0	01000	@	2
s, B1	11000	A	3
s', D	00100	:	4
s', R	10100	S	5
s, D	01100	I	6
s, R	11100	U	7
s', A	00101	H	20
2s', A	11101	Q	23
-s', A	10101	Y	21
a + s', A	00111	M	28
a + s, A	00011	O	24
am + s, Am	01011	G	26
a - s', A	10111	X	29
a & s', A	11111	£	31
a or s', A	00010	$\frac{1}{2}$	8
a ≠ s', A	01111	V	30
al, S	10010	D	9
am, S	11010	J	11
al, S; (0), Al; Rev. A	10011	B	25
Rev. A	10001	Z	17
Test	01010	R	10
Stop	01110	C	14
am, S; (0), Am	11011	"	27
s', A	01101	P	22
al or (al + s); Al	( 00001	T	16
(	( 01001	L	18
(	( 00110	N	12
Nothing	( 10110	F	13
happens	( 11001	W	19
(	( 11110	K	15

Performance

The Ferranti Mark I had a 10 microsecond digit period. The basic machine rhythm was designed in terms of 240 microsecond 'beats', where a beat contained 20 digit periods, together with a 40 microsecond 'blackout period'. Generally speaking, store access (or 'scan') beats alternated with ALU (or 'action') beats during execution of an instruction. Control transfer and B-line orders took four beats (i.e., 0.96 milliseconds); accumulator load/store/add/logical orders took 1.2 milliseconds and multiplication took 2.16 milliseconds.

The first production Mark I was installed in February 1951 and finally dismantled in June 1959. Ferranti delivered nine Mark I or Mark I star machines between 1951 and 1957, to the following organisations:-

<u>Customer</u>	<u>Date delivered</u>
Manchester University	1951
Toronto University	1952
Ministry of Supply	1953
Royal Dutch Shell Labs. Amsterdam	1954
National Inst. for Application of Maths., Rome	1955
Atomic Weapons Research Est., Aldermaston	1954
Ministry of Supply, Fort Halstead	1955
A V Roe and Co Ltd, Manchester	1954
Armstrong Siddeley Motors Ltd, Coventry	1957

## REFERENCES

1. Lavington, S H : 'A History of Manchester Computers' published by the National Computing Centre, Manchester (1975).
2. Williams, F C and Kilburn T : 'A storage system for use with binary digital computing machines' Proc IEE, Vol 96, part 2, No 30, 1949, 183ff.
3. Williams, F C, Kilburn, T and Tootill, G C : 'Universal high-speed digital computers : A small-scale experimental machine' Proc IEE, Vol 98, part 2, No 61, Feb 1951, 13 - 28.
4. Kilburn, T, Tootill, G C, Edwards D B G and Pollard, B W : 'Digital Computers at Manchester University' Proc IEE, Vol 100, part 2, 1953, 487 - 500.
5. Pollard, B W and Lonsdale, K : 'The construction and operation of the Manchester University Computer' Proc IEE, Vol 100, part 2, 1953, 501 - 12.
6. Tootill, G C : 'Informal report on the design of the Ferranti Mark I computing machine' Ferranti internal memorandum, Nov 22nd 1949.
7. Turing, A M : 'Programmer's Handbook for Manchester Electronic Computer Mark II' 1950. (Note:- the Ferranti machine was called the Mark II by Turing, to distinguish it from the existing university prototype or Mark I. Turing's nomenclature was later abandoned and the machine became known simply as the 'Ferranti Mark I', as distinct from the 'University Mark I'.)
8. Brooker, R A : 'The Programming Strategy used with the Manchester University Mark I Computer' Proc IEE, Vol 103, Part B, Supp 1 - 3, 1956, 151 - 57.