Kolsky
Memo 5

May 28, 1958

PROJECT 7000

FILE MEMO

SUBJECT: The Effect on SIGMA Performance of Putting Instructions in the Index Memory

INTRODUCTION:

A recent Memo ("Revisions on Rules, etc" by W. Wolensky May 5, 1958) has proposed that no instructions be executable from memory locations 0-31. Since these locations include the 16 index registers, the proposal has the effect of eliminating the use of the index registers as general memory.

The idea of putting small frequently executed loops in the index memory has been discussed qualitatively many times in the past. The feeling always was that there should be many cases where the time spent transmitting the code into the indices would be paid back many-fold by the increased speed of doing the loop. In view of the present proposal it seems worth while to reexamine this proposal in more quantitative terms.

To test the effectiveness of index memory for instructions, the following runs were made on the SIGMA Timing Simulator:

(1) The Mesh Calculator with its entire code in index memory. (data references still in Main Memory.)

(2) The Monte Carlo Code with its entire code in index memory.

(3) Each of the above were run for Index transistor registers and for Index Core Memory of cycle times: 0.2, 0.4, 0.6, 0.8, and 1.0 usec.

(4) Each of the above were run for both the old "STANDARD" (contract) arithmetic speeds and the February "Recommended" speeds.

Note: These runs are unrealistic in that an index memory of unlimited size was assumed in the Simulator. For example, the entire Mesh Calculation obviously cannot fit into 16 memory cells without considerable shuffling of code. No estimate is included in these runs for the time which would be spent moving code.

RESULTS:

The graph which follows shows the results of these runs in the form of SIGMA Speed Times 704 speed vs. the Index Memory Total cycle time. The read-out time of the index memory is assumed to be one half the total cycle time except for the 0.1 usec case where it is also 0.1 usec.

1. The system is considerably more sensitive to any of the changes when its performance is high (STD vs REC times).

2. For the Mesh Calculation, which is not instruction-fetch limited, putting the instructions in Index Memory gives only a 3% improvement at STD speeds but causes about a 5% reduction with recommended speeds.

3. The Monte Carlo Code, which suffers from instruction fetch delays because of frequent branches, is improved by 33% at standard speeds (with transistor index registers) but unchanged at recommended speeds.

CONCLUSIONS:

1. If we are to have transistor index registers in SIGMA there are cases of short-tight loops in which sizeable performance gains are to be obtained by putting the code in the indices.

2. If we are to have some form of index core memory, there seems to be no speed gain to be had by putting code in the indices.

3. The time lost by transmitting the code to the indices must be subtracted from any gains due to increased performance. A given operation would have to be executed at least four times from the index memory to break even in the best case.

4. The main loss in forbidding the use of code from the index memory is one of memory symmetry. The index memory will no longer look like any other memory address. This is a difficult quantity to evaluate performance-wise. One must always keep in mind that future technology may wipe out the restrictions which we presently envision applying to memory speeds, so that we may regret asymmetries introduced now.

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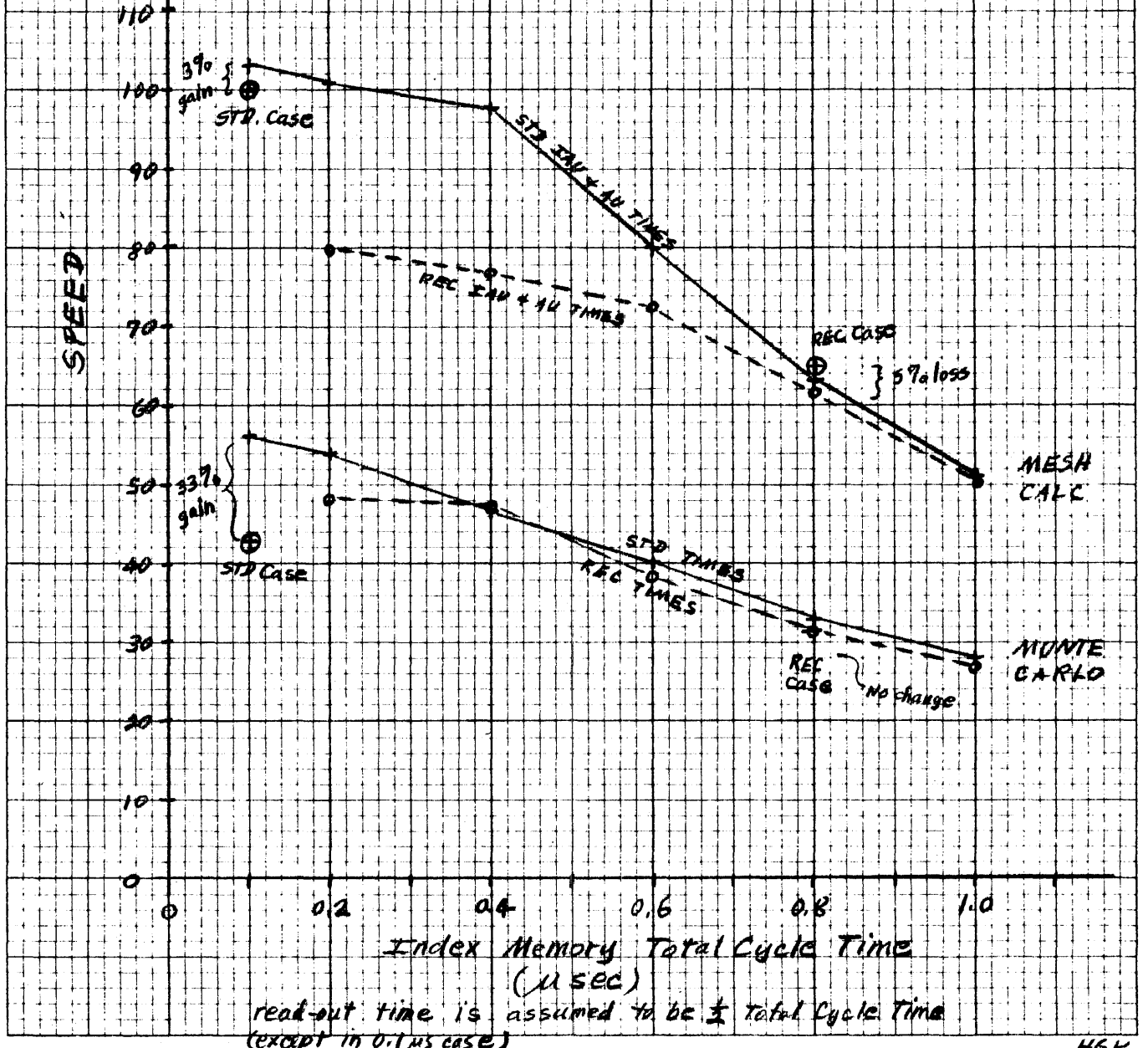
SIGMA COMPUTER SPEED VS. INDEX MEM. CYCLE TIME

For various cases in which the instructions are in index memory,

4 Main Memories 2.0 μs
2 Instr. Memories (when used)
4 levels of look-ahead
1 Index Memory
AV. acc. time STD 0.64 μs REC 1.09 μs
IAU acc. time 0.6 μs 0.9 μs



read-out time is assumed to be ½ total cycle time (except in 0.1 μs case)

HGK