SIGMA COMPUTER MEMO #20

TO: E. Bloch

SUBJECT: Sigma Bus Control Unit

DATE: December 3, 1958

This memo describes the Sigma Bus Control Unit presently under construction. The design permits attachment of a (10) Memory Booster Unit and a Harvest Booster Unit. The Standard Bus Control Unit accommodates six memories (four Main Memories and two High Speed Memories) at a .2 us transfer rate.

L. O. Ulfsparre

LOU/jam

A DESCRIPTION OF

THE SIGMA MEMORY BUS CONTROL UNIT

I. INTRODUCTION

The purpose of this report is to describe the Sigma Bus Control Unit currently under construction. While this description is intended to be complete, a list of pertinent letters covering previous work has been included for its historical and patent significance. Patent disclosure #71488-Clock Double Bus System, submitted on 6-24-57, is the original document and the information herein supplements that work. The organization of this report is outlined below for your convenience and serves as an introduction and guide to the body of the report.

7. Synchronizing Exchange requests
8. High Speed Exchange memory blocking
9. Fetch Address check
10. Store Address check
11. Memory Address too high check
12. Memory select

B. Memory Timing

C. Output Control

1. Output slot reservation scheme
2. Memory sequencing and access time
3. Return Address
4. Return Address gate selection
5. Return Address sequencing and storage
6. Panel key entry

V. SERVICE RATES AND ACCESSING TIMES

VI. HISTORY

II. FUNCTIONAL DESCRIPTION

A. Two Prime Functions

The two prime functions of the Bus Control Unit (BCU) are:

1. To regulate the transfers of MEMORY ADDRESSES, STORE DATA and STORE/FETCH commands from various accessing registers of the system to the proper memories.

2. To regulate the transfers of FETCH DATA from various memories to the proper receiving registers of the system.

B. Additional Functions

These arise either in connection with the prime functions or because of Sigma packaging considerations.

They are:

1. To transmit Memory Address error signals (STORE ADDRESS CHECK, and FETCH ADDRESS CHECK) to the proper accessing or receiving points.

2. To provide Exchanges with a programming error signal when

their Memory Address is too high. This will occur when the address selected lies beyond the physical capacity of the memories installed.

3. To perform certain comparisons on Sigma-generated addresses:

   a. High-Low comparison of Fetch Addresses with the Upper and Lower Boundary registers.

   b. Lookahead comparisons of Fetch Addresses with the Lookahead Effective Address Register.

   c. Program store comparison of the Fetch Addresses with the Instruction Counter Register and Instruction Counter Adder.

4. To provide an entry and exit for the Harvest computer. Entry is provided for Harvest Memory Address, Harvest Store Data, and Harvest Store/Fetch commands and exit is provided for Harvest Fetch Data.

5. To provide modular packaging of a standard Sigma BCU, a Memory Booster, and a Harvest Booster.

6. To provide an entry for panel key data from the Sigma maintenance panel to various receiving registers.

7. To generate and distribute Sigma clock pulses.

8. To delay gating of Store Data to memory permitting overlap of memory array decoding with the previous regeneration cycle.

III. PHYSICAL COMPOSITION

Figure 1 shows the modular composition of the bus system. It consists of three units: the standard BCU, a Memory Booster, and a Harvest Booster.

The Memory In Bus has four standard inputs and two additional inputs. Each Exchange has a Store/Fetch channel and Sigma has one Store channel and one Fetch channel. When High Speed Exchange handles tape (for the Harvest) computer) its entry becomes two channels -- one Store channel and one Fetch channel. The sixth channel is the Harvest entry channel. The Memory In Bus has a three-pronged output: two standard buses and one extension to the Memory Booster which adds two buses. Each bus feeds four memories.

The Memory Out bus has six standard memory inputs; one Sigma maintenance panel entry, and one extension from the Memory Booster. It has a three pronged output: an Exchange Memory Out Bus, a Sigma Memory Out bus,and an extension to the Harvest Booster.

Because of modularity, some split control is necessary. Input bus control is shared by the BCU and the Harvest Booster. The BCU controls five input channels and the Harvest Booster controls two channels. Memory frame decoding and Memory busy control are split between the BCU and the Memory Booster. Each BCU channel except I-box has a memory address decoder which recognizes six memories: two High Speed Memories and four Main Memories. The I-box channel can decode the full complement of memories: four High Speed Memories and twelve Main Memories. The remaining four channels (BX, HX-S, HX-F, and LA-S) complete their decoders in the Memory Booster, each recognizing two High Speed Memories and eight Main Memories in the Booster. Likewise, the memory busy triggers are distributed between the BCU and the Memory Booster.

The BCU is packaged in one rollagon frame. It contains approximately 2,850 cards utilizing 75% of the available space in the frame. 650 cards are required for additional functions arising because of Sigma packaging considerations. They are as follows: Sigma Hi-Lo and Program Store compare 370 cards, Sigma Lookahead Address register and Address compare 100 cards, and Sigma Master Clock 180 cards. The 2200 cards remaining (approximately 8400 transistors) describe the bus proper and they are used as follows:

	Memory In Slide		Memory Out Slide		
Cntl	640		410		1050 Cntl Total
Data Flow	570		580		1150 Data Total
	1210	In	990	Out	2200 Bus Total
	100	La Adr Reg	550	Hi-Lo, Prog store and clock	650 Total Extras
	1310		1540		2850

The In slide requires about 775 external lines and the Out slide 975. Only 31 lines connect the slides indicating their relative independence. The Memory Booster slide is estimated at 1,250 cards and 1,000 external lines leaving about 500 spare card spaces and no spare external lines. The Harvest Booster slide is estimated at 1000 cards and 500 lines leaving about 750 spare card spaces and about 500 spare lines.

IV. CONTROL

Fundamentally, the BCU consists of two serial buses: A serial memory in bus driven from a common point of converging input channels; and

a serial memory out bus driven from a common point of converging output channels. On the Memory In bus, the BCU selects the proper input channel according to a predetermined priority system and the proper memory gate determined by the memory address. On the memory out bus, memories are self -gating and the BCU selects the corresponding receiving register gate according to an output sequence determined at read-in time. Each bus operates at a .2 us rate.

With this introduction, we may proceed to the following sections which describe input control, memory timing, and output control.

A. Input Control

1. Synchronization with Sigma

The BCU operates synchronously with Sigma by joint use of a five megacycle sample pulse source. The corresponding .2 usec period also determines the bus transfer rate. The bus servicing sequence is determined in the slot previous to the transfer slot according to priority conditions and memory availability.

2. Overlapping Control and Transmission

In order to maintain a .2 us transfer rate, both bus priority decisions and transfers overlap. During the transfer of one request to memory, the BCU is determining which request will be transferred during the next cycle.

3. Priority

Priority is granted by the BCU if the following is true:

a. The desired memory is available (not busy).
b. The channel has higher priority than all other channels requesting available memories.

Memory availability is determined by memory busy triggers in the BCU which are set when a memory is accessed, and reset when the memory is ready to accept a new request. These triggers control the output of the memory frame decoders so that only available memory requests compete for priority.

Priority is as follows:

a. Basic Exchange (BX)
b. High Speed Exchange (HX)

c. Sigma Lookahead (LA)
d. Sigma I-box (I)

Priority has been given to Exchanges over Sigma since they must meet the rates of continuously running Input/Output units. As their usage of the bus (7%) is low, Sigma has little direct interference from Exchanges because of their higher bus priority. By using its priority to request a memory desired by the computer, the exchanges can indirectly cause much greater interference.

4. Typical Priority Sequence

Figure 2 shows a typical input control sequence illustrating a number of points: the .2 us slot; overlapping of the priority decision and transmission; effects of low priority or busy memories on access time; and use of busy triggers. In this example, Basic Exchange, High Speed Exchange, and Lookahead all make simultaneous requests for the bus. Basic Exchange has priority and gates its address to memory. High Speed Exchange waits one slot for the bus, transfers its request, and Lookahead waits two slots for the bus.

5. Delayed Data

Basic Exchange and Lookahead store data gates follow their address gates by .4 us to permit the memory overlapping function discussed in section III, Paragraph A-5. (Since the address is also required for the priority decision slot, the data may lag the address by as much as .6 us.. This may be utilized in the accessing device to convert data checking codes to the modified Hamming code used in memory.)

6. Overall Input Control

Figure 3 shows the overall input control scheme. Each channel has an independent memory frame decoder which tests for memory availability by mixing the address with the busy trigger. Take BX as an example. If its memory is available, the decoder conditions the BX Priority And-circuit. Assuming the request (REQ) trigger has been previously set by a BX request, the Sp sample sets the BX address gate single-shot which connects the BX address gate to the bus. Further, the BX decoder output inhibits all other channels from setting their gate controls. If, for instance, I-box was trying to use the bus, it would have to wait until BX or any other channel with an available memory had been serviced. By taking bus priority from I-box, the other channel might set I-box's memory busy.

Thus, even if the next slot is free, I-box must now wait for a memory cycle. This indirect effect is much greater although a sufficient number of memories can reduce this effect to a negligible amount.

7. Synchronizing Exchange Requests

As the Exchanges do not share the Sigma clock, their bus requests can come at any time with respect to the Priority sample (Sp). If one came at Sp time, it might set its own gate controls, but be too late to inhibit those with lower priority. Thus, two address channels would be gated to the bus. To prevent this, Exchange requests are synchronized by the Sr pulse, (this precaution takes an average of .1 us or one-half slot) which comes early with respect to Sp.

8. HX Memory Blocking

In Figure 3, the connection between the Sigma Memory Frame Decoders and the busy triggers must pass through a supervisory control operated by the High Speed Exchange. Normally, this control is inactive, but under certain conditions, for (Harvest) which High Speed Exchange is fetching a memory word for tape it is required. To remain within a required maximum accessing time, the High Speed Exchange prevents Sigma from using the memory that High Speed Exchange will want next.

This reservation may precede the request by as much as 2 us, but only effects one memory at a time not all of memory. Therefore, the probability of interference with Sigma is low.

9. Fetch Address Check

This signal comes from memory. It signifies either a parity error in memory address transmission or incorrect array decoding by the memory. The memory gates this out as a 73rd tag bit along with the Fetch Data to the Out bus.

10. Store Address Check

This signal comes from memory. It too signifies either an address transmission error or a memory decoding error. It is sent to the BCU which must recognize who sent the request and pass the error signal to the sender.

11. Address Too Hi Check

If the memory address requested by either of the Exchanges lies beyond the memory capacity, a signal is sent to the Exchange, and the bus service request terminated. All memory addresses sent by Sigma are first screened for validity so an address beyond memory appearing at the BCU must be a transmission error condition. To keep Sigma from hanging up, this request is sent to memory where the normal parity check sets up the normal error signals. The first memory address is conveniently used for this purpose.

12. Memory Select

When a priority And-circuit sets its address gate control, the corresponding decoder sets the proper busy trigger and Memory Select single-shot. (Figure 3 illustrates this.) The single-shot remains on after the busy trigger has interrupted the frame decoder output. Its output is sampled by a memory select pulse (Sm) which is time-coincident with the address at the memory gate.

B. Memory Timing

All memory timing begins from the Memory Select pulse. Through delay lines, all required internal and external gating pulses are generated by each memory. Memory generates its own Data Select .4 us after the select pulse during Store cycles. It also generates a busy trigger reset to bracket the proper (Sp) pulse in the BCU. The Data out gate during a fetch cycle is timed to synchronize with Sigma after passing along the Memory Out bus. Also, since memory outputs must be separated by .2 us. intervals at the BCU, the memory furtherest from the BCU determines this. The nearer ones add compensating delay to make up for shorter access cables.

C. Output Control

Since the actual memory access times will not be verified until next year, this area of control was designed to meet the rather broad limits below.

a. Minimum high speed memory access = .6 us or 3 slots.
b. Maximum main memory access = 1.4 us or 7 slots.
c. Maximum difference = .8 us or 4 slots.

An obvious but somewhat expensive solution is to use a Double Out bus with one type of memory on each bus. The expense arises

because of the double drive and double gates required by the receiving registers. An additional problem is the extra lines required by the Double bus. Therefore, a single Out bus with variable access for High Speed Memory. Actually, the Single Out bus design selected could in principle handle any two types of memory with different accessing times.

1. Output Reservation Scheme

First of all, the Output bus is only used with fetching. An output bus slot is reserved when the fetch request is read into memory. Normally, the memory access time determines this. However, since there are two types of memories with different access times, the High Speed Memory can ask for an output slot already reserved by a main memory. In these cases, High Speed Memory yields to Main Memory and takes the first slot available Prior reservations by either Main Memory or an earlier High Speed Memory request may exist.

2. Memory Sequencing and Access Time

Maximum access to Main Memory determines the system's ability to service Exchanges. Request sequence may be important to preserve if a second request is made from a register before the first request has been returned. Since Main Memory slot reservations are always prior to High Speed Memory slot requests, neither its access time nor output sequence are affected by this reservation scheme. This is true of High Speed Memory accesses only if Main Memory fetches do not interfere. Since the Sigma systems' maximum fetching ability uses only one-half of the bus slots, the High Speed Memories average access time should be within one slot from the minimum. The maximum access time for High Speed Memory is equivalent to a Main Memory access time. Thus, using the current figures of .6 us access and 1.0 us access, High Speed Memories access is usually within .8 us but could be as high as 1.0 us. Generally, sequencing is preserved but there is one exception. Negative sequencing across the type boundary will reverse the sequencing at the boundary. A positive sequencing of addresses which cross memory-type boundaries should not cause any difficulties since the faster memory has the lower address.

3. Return Address

This reservation scheme described above is accomplished through controlling the readout sequence of the RETURN ADDRESS

which is stored in the BCU until needed. The return address is a three-bit code which specifies which register gate should read the data on the Out bus. It is listed below:

Basic Exchange	(BX)	BCD P
		000-1
High Speed Exchange	(HX)	001-0
Sigma Instruction Register	(Y_1)	010-0
Sigma Instruction Register	(Y_2)	011-1
Sigma Operand Register #1	(LA_1)	100-0
Sigma Operand Register #2	(LA_2)	101-1
Sigma Operand Register #3	(LA_3)	110-1
Sigma Operand Register #4	(LA_4)	111-0

A fourth bit allowing eight more return registers is planned for Harvest. The return address is made up at the BCU when the fetch request is made. The I-box supplies bit D and Look-ahead supplies bits C, D, and P.

4. Return Address Gate Selection

Figure 4 shows the gate controls for the Out bus. Assume, for the moment, that the Return Address Out bus provides properly sequenced and timed return addresses. These are sampled every .2 us and timed to send a Sigma gate select one slot before the corresponding data is expected at the Sigma register. This pre-selection gives the Sigma register time to request priority on its Data Check bus. Since the Exchanges do not require pre-selection or synchronization, the decoded gate control select pulse is delayed about .3 us. The error output of the return address parity checker is sent to the interrupt mechanism as a bus control check. Parity is also used in the decoder to prevent gate selection if a single error is present.

5. Return Address Sequencing and Storage

The mechanism in figure 4 consists of eight Return Address registers with sequentially selected inputs and outputs such that the difference between the input gates and output gates determine the storage time. An eight position closed ring is used to provide commutation. For main memory, the required storage time is 6 slots. (This is one less than the memory access because of pre-selection.) As Figure 4 illustrates, when fetching main memory at (Io) time, Return Address register select single shot (SS_7) is set causing the return address to read into Register 7. It remains there until (0_6) time when it is gated to the return address decoder where it is used to pre-select a

return register. A Main Memory fetch at (I_1) time would be used at (0_7) time and so on. As registers are selected, their status triggers are set. This forms the basis for selecting the first available output slot for a High Speed Memory fetch. For instance, the condition of status triggers 7, 0, 1 and 2 determine at (I_4) time which slot will be used to read out of memory. The High Speed Memory Read Out Slot selector has eight sets of five And circuits which select the first empty slot. High Speed Memory must be advised of this selection so that it may gate data into the proper output slot. This information is sent on the Readout Delay bus to the memories. High Speed Memory must also use this information to delay Memory Reset so that a new fetch will not interfere with the previous one. If the current times of .6 us and 1.0 us are verified by construction, then six registers and a six-by-three selector could be used. Thus the principle is easily modified to suit ones' needs within the broad limits previously defined. If it was known that only one type of memory would ever be used a delay line would provide sufficient storage since readout times would be constant. If High Speed memories are an optional feature, then the Status Decoders and High Speed Memory Read Out slot selector can be removed or added as necessary.

Should the read out ring producing the I and O gates fail, (none or two or more on) then the Bus Control Check single - shot is set and the interrupt mechanism alerted.

6. Panel Key Entry

The control for Sigma Panel Key entry is via I-box and made to look like a fetch. Instead of fetching from memory, however, the Panel Key data is read into the Out bus during any slot not used by a memory readout. Empty return address register status controls this gate as well as the Panel Key Return Register gate control selection.

V. SERVICE RATES AND ACCESS TIMES

As figure 5 shows, the minimum access time including checking is 2.2 us. The letters M, B, and C denote places where the access time might be increased while waiting for a busy memory, a busy bus, or a busy checker. An Accept is available in .4 us if the memory or bus are not busy. For the Exchanges, a response can come in .3 - .5 us under the same conditions. This time is indeterminent because of their asynchronous operation with the BCU. Consequently, their best access time to main memory without checking is 1.7 - 1.9 us, which compares with Sigma's 1.8 us access (without checking). Store responses are also .4 us and provide the start signal for a .4 Data

gate to the BCU. (Anything outside this .4 us range is satisfactory also.

Table 1 shows the service rate and bus usage of the various accessors. In the case of Exchanges the minimum and maximum access times and the required maximum access are shown. Here it can be seen that Basic Exchange required maximum access is easily met (3.7 us out of an allowable 4.5 us) while High Speed Exchange requests are barely met (5.7 us out of 5.8 us). Blocking the computer access can reduce worst case to 3.7 us. This would allow the High Speed Exchange to replace their full word byte register with a half-word byte register. Of course, this would reduce the maximum allowable access by one byte time (1.7 us) to 4.1 us. Although the exact timing has not been established, another situation requiring blocking is chain read tape or chain write tape. In summary then the system can service the Exchanges even under worst case conditions.

The Computer's accessing problem is quite different from the Exchange's required maximum access. The computer's chief requirement is a high average processing rate, fetching 8-10 times more frequently than the Exchanges. To overcome a minimum initial access time of approximately .2 us, all of the device in the system use multiple buffering. I-box has two Instruction registers, Lookahead has four Operand registers and Harvest has its Streaming registers. Another important factor is interleaving of memory addresses in different memory frames. This helps average access, too, provided instructions and operands are not in the same memory group.

A third factor is the number and use of memories. Consider the following: I-box fetches two half-word instructions (one full word) every 1.6 us (12 1/2% of the bus slots). It also fetches two operands every 1.6 us (25% of the bus slots). Assume that the instructions are stored in two interleaved memories and the operands in four interleaved memories. Used at a maximum rate, two High Speed Instruction memories would require 66 2/3% of the bus slots. Therefore, even with a maximum usage by the Exchanges of 7%, there is ample capacity to provide a high average rate of instruction. If two main memories are substituted, they would require 20% of the bus slots. Here maximum Exchange usage brings the requests close to maximum capacity. Buffering can compensate for interferences and still provide a high average rate. If four Operand Main Memories are used at maximum rate, 40% of the bus slots are required. Thus, even with maximum Exchange interference, there is sufficient capacity to provide a high average processing rate.

Obviously these three factors,computer buffering, interleaving, and the number and use of memories interact and compensate for each other. Naturally proper balance is desirable and this is an important system consideration. The BCU's chief function here is to provide sufficient slots to provide a smooth steady flow with a minimum of conflicts. Since the Sigma system uses only 50% of the slots and Harvest 90% of the slots, the .2 us slot seems adequate to handle Sigma's conflicts or Harvest's streaming traffic.

The bus can theoretically service three High Speed Memories at their maximum rate or ten Main Memories at their maximum rate. The combination of two High Speed Memories and four Main Memories can also be serviced at their maximum rate. Because it is unlikely to achieve 100% accessing efficiency, more memories can be added without creating a bus bottleneck.

It is my belief that the bus design has been optimized to meet the requirements of Sigma and the Exchanges. Packaging allowances in the BCU for Harvest data paths and the bus capacity are such that it seems feasible to handle the Harvest System by adding a Harvest Boost control unit. Detailed analysis of Harvest's problem may prove that another packaging arrangement may be more desirable for a Harvest bus. However, this "one-two" approach (Sigma first - Harvest second) has produced concrete results where a three-in-one design approach served to define the range of the problem.

VI HISTORY

Below are listed a number of internal letters pertinent to the present bus design which has been optimized for Sigma. Missing are several other abortive proposals to attain a compromise three-in-one design, which would be low in cost for a Basic computer and high in performance for Harvest.

Letters 1 and 3 define the major problems and describe the basic bus design. Letters 2, 4 and 10 discuss checking. Letter 6 represents an early estimate of the bus. Letters 7, 9 and 13 discuss memory addressing. A return Addressing scheme is proposed in Letter 11. Letters 8 and 12 describe the bench work. A Harvest proposal is set forth in 14. External communication is listed in 15.

LETTERS

1. R. T. Blosk and E. D. Foss (6-6-57)-Description of a clock controlled double bus system Memory Bus File Memo #1; Project Stretch Memo #61.

2. R. T. Blosk (7-1-57) - Memory Bus File Memo #2 - Summary of Meeting discussing Memory Bus Checking.

3. R. T. Blosk, E. D. Foss, R. E. Merwin, and J. H. Pomerene (7-2-57) - Patent Disclosure #71488 - Clock Controlled Double Bus System.

4. L. O. Ulfsparre (7-3-57) - Design of a Memory Bus Hamming Checker.

5. R. T. Blosk, J. W. Fairclough (7-26-57) - Description of an Improved Bus System Memory Bus File Memo #3; Project Stretch File Memo #63.

6. L. O. Ulfsparre (8-16-57) - Memory Bus Estimate.

7. S. G. Tucker (10-2-57) - Addressing Scheme - Basic Computer Memo #3.

8. L. O. Ulfsparre - (11-6-57) - Memory Bus Progress Report.

9. S. G. Tucker (12-2-57) - Memory Addressing Scheme.

10. R. T. Blosk (12-16-57) - Hamming Checking/Correcting in the Basic System.

11. L. O. Ulfsparre (1-27-58) - Proposed Memory Return Addressing Scheme.

12. C. R. Doty, Jr. (5-14-58) - Memory Bus Bench Test.

13. L. L. Headrick (1-31-58) - Memory Addressing Scheme.

14. R. M. Meade (6-25-58) - Parallel Data Transmission; Harvest File Memory #12.

15. L. O. Ulfsparre (11-3-58) - Numerous miscellaneous memos describing bus external communication lines.

A number of people have been associated with the bus design in the last year and one-half.

1. R. E. Merwin, E. D. Foss, R. T. Blosk and J. W. Fairclough are associated with the early phases of design.

2. R. C. Kuenstner, S. L. Lindauer, and I (May-July '57) carried the design through its three-in-one phase) (July '57 - May '58)

3. Foss, Blosk, J. H. Pomerene and I discussed checking. (July '57 and Dec. '57)

4. C. R. Doty, Jr. performed the bench tests.

5. I planned synchronous Sigma design and Variable Access Single Out Bus. (May - Oct. '58)

6. E. Bloch directed Sigma optimizing and packaging (Aug. '58)

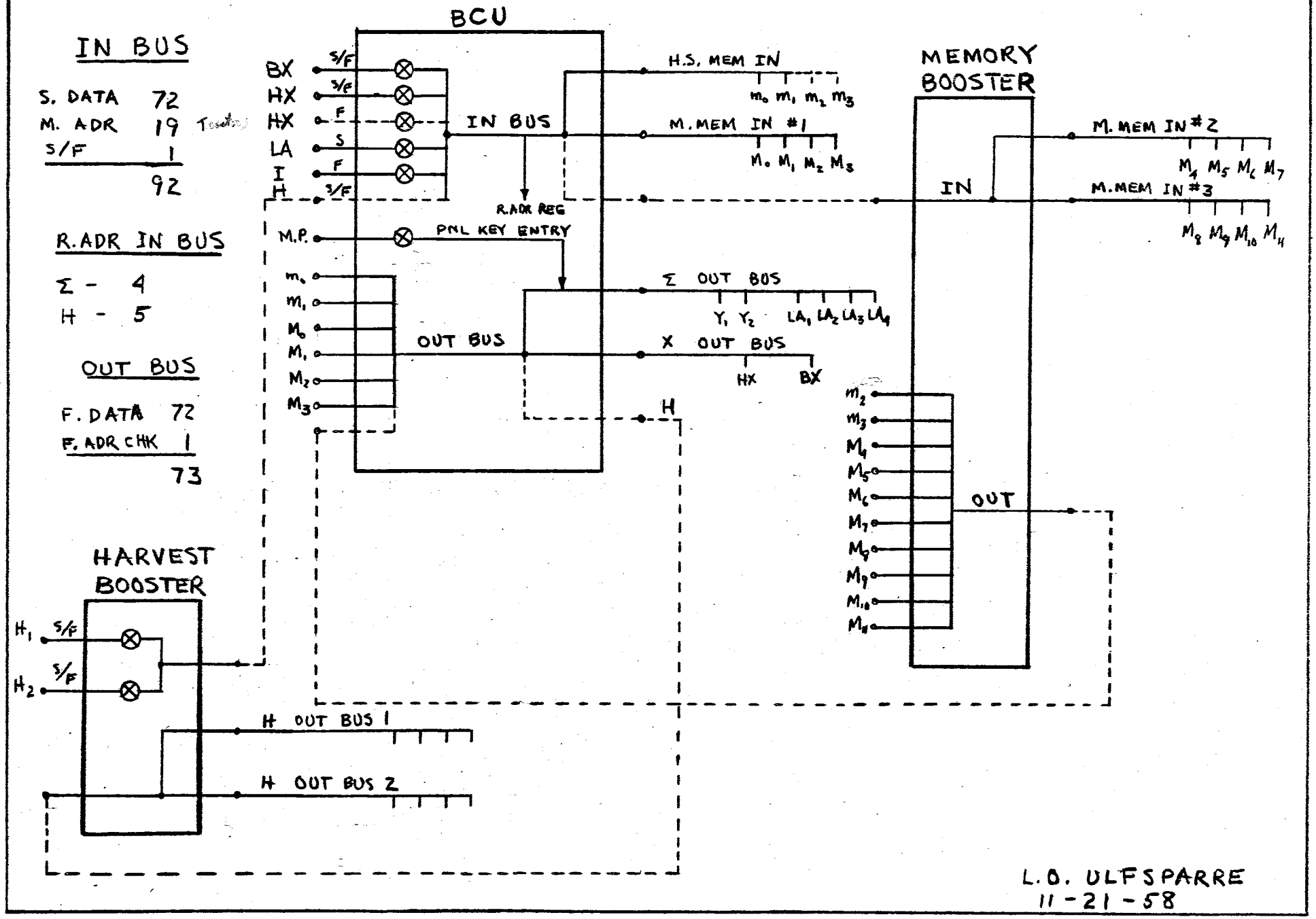
7. M. R. Marshall and P. Soltanzadeh did the detail design and frame layout (Aug. '57 - present)

8. G. E. Werner is overseeing construction and testing of the model and design of the Sigma Clock. (Aug. '57 - present)

L. O. Ulfsparre
December 1, 1958

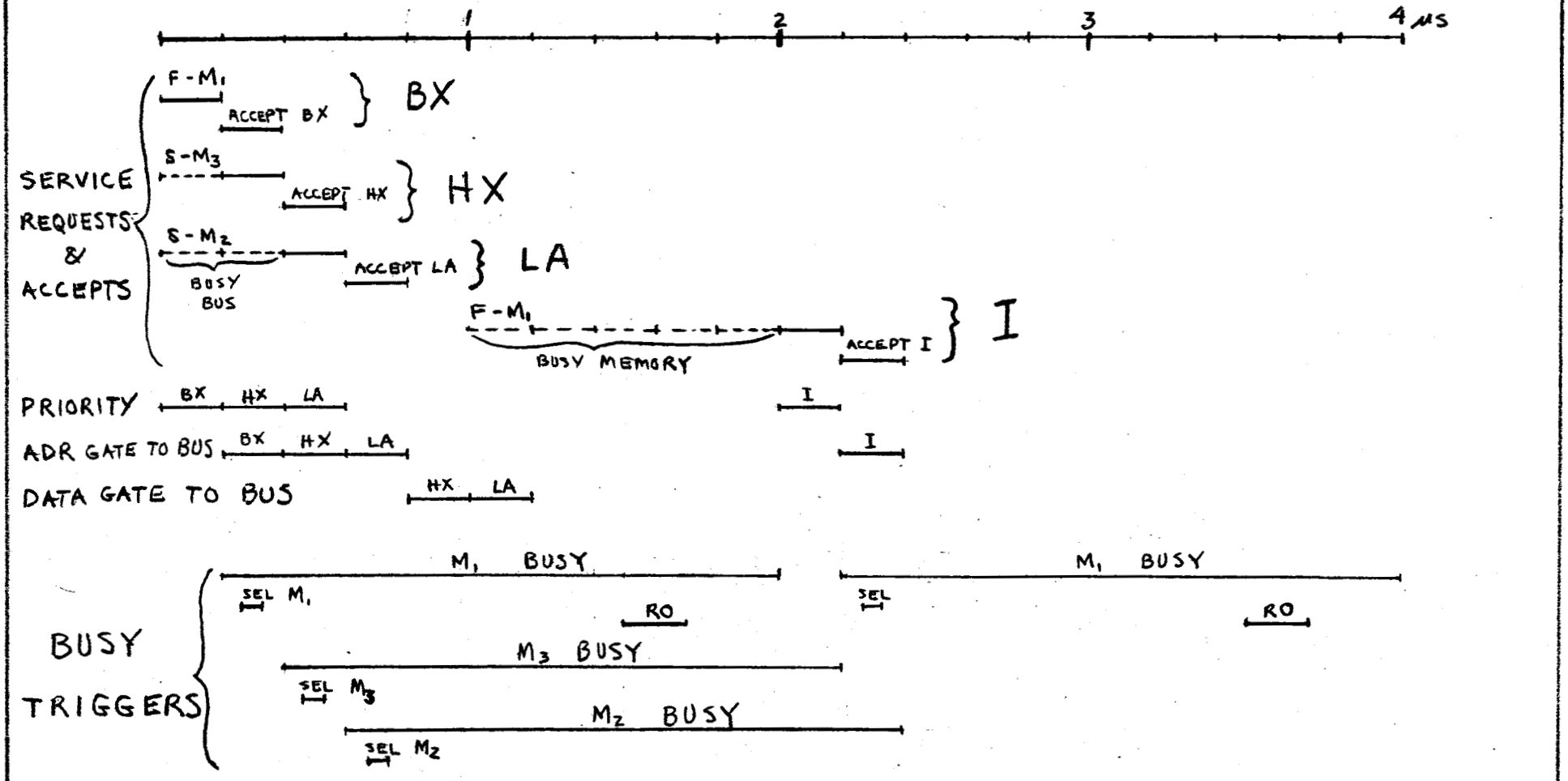
LOU;jam

FIGURE 1 - BUS COMPOSITION



L.O. ULFSPARRE
11-21-58

FIGURE 2 - TYPICAL PRIORITY SEQUENCE



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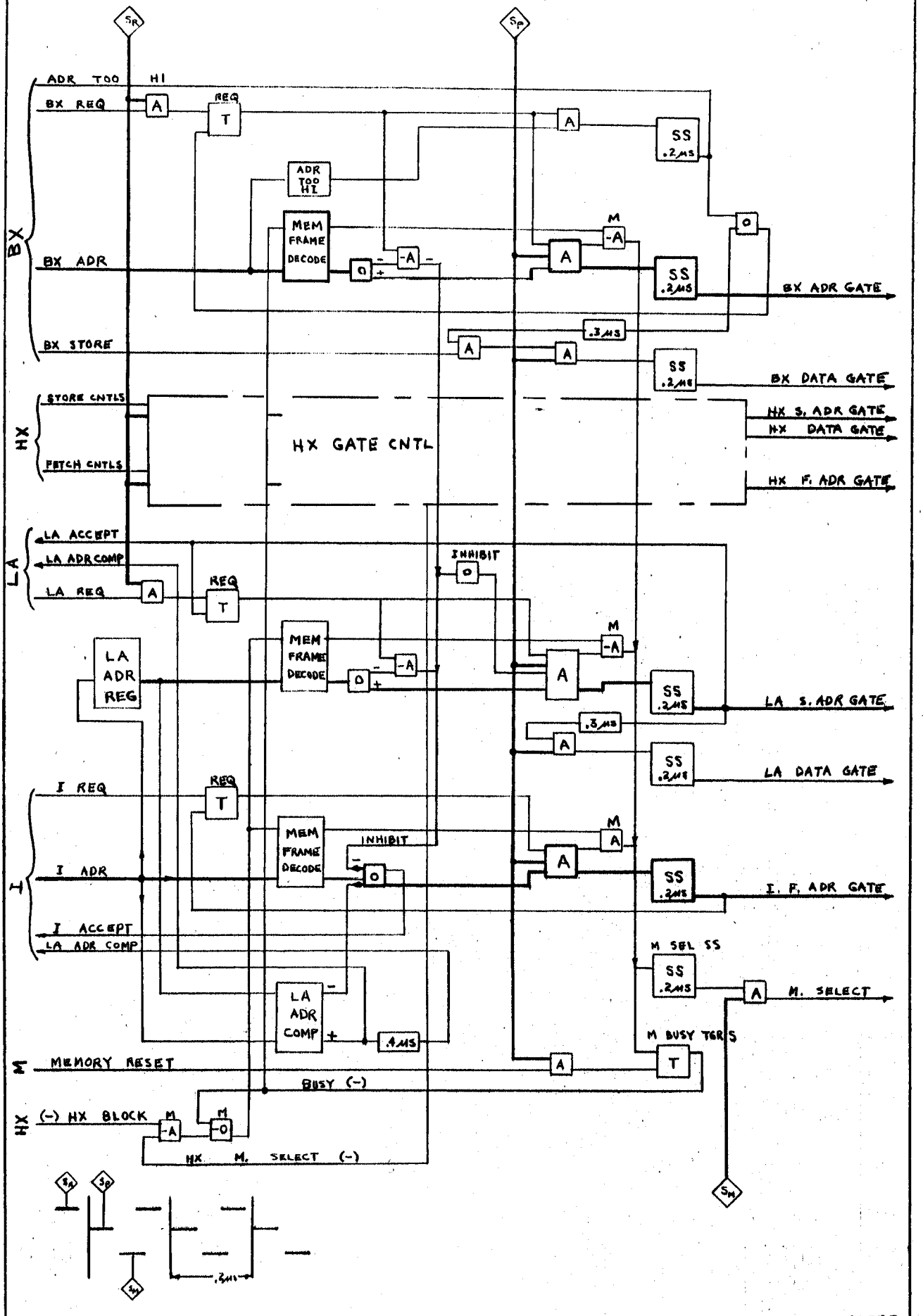
11-21-58

FIGURE 3 - GATE CONTROLS FOR MEMORY IN BUS



10-23-58 L.O. ULFSPARRE

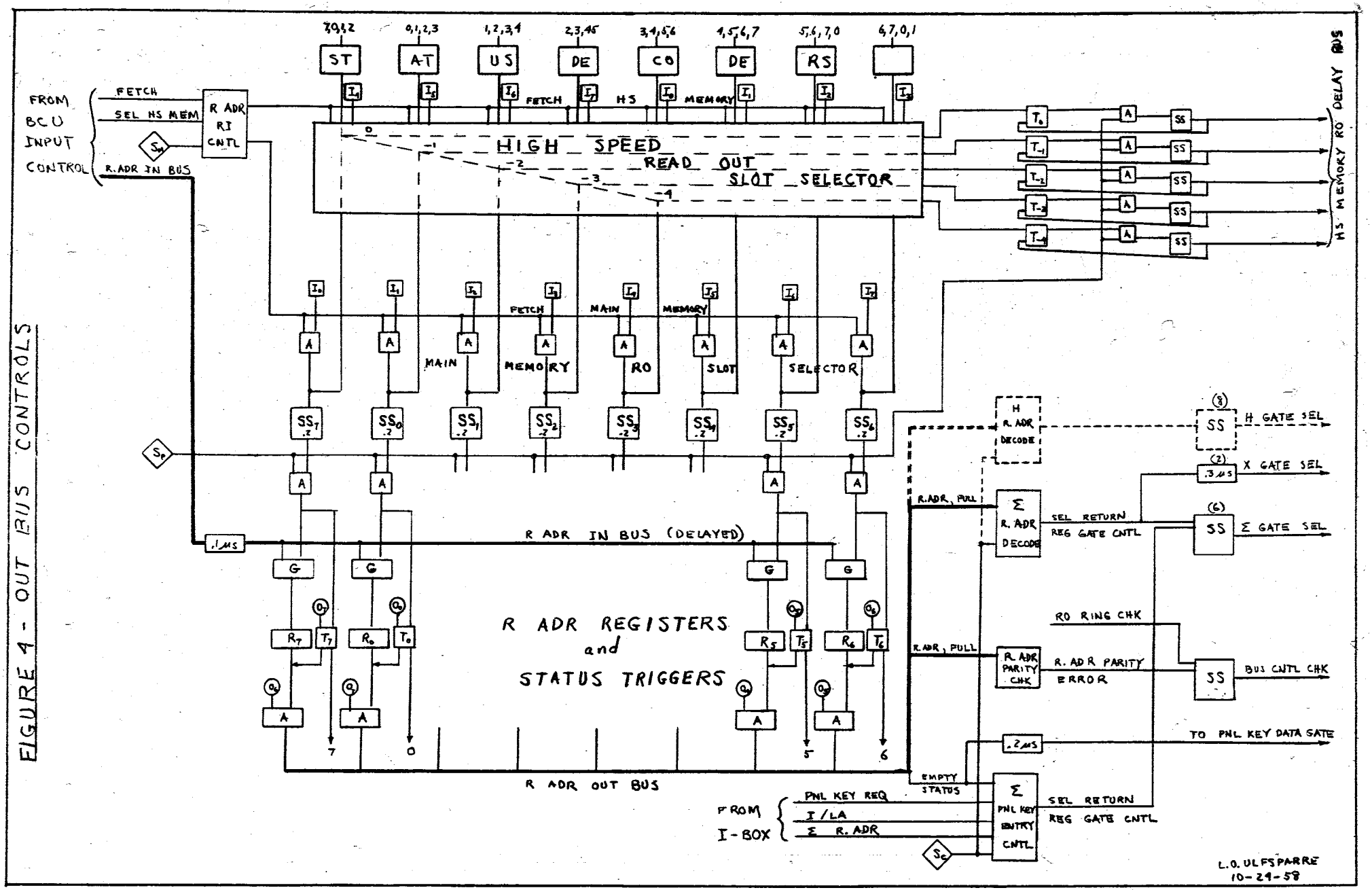
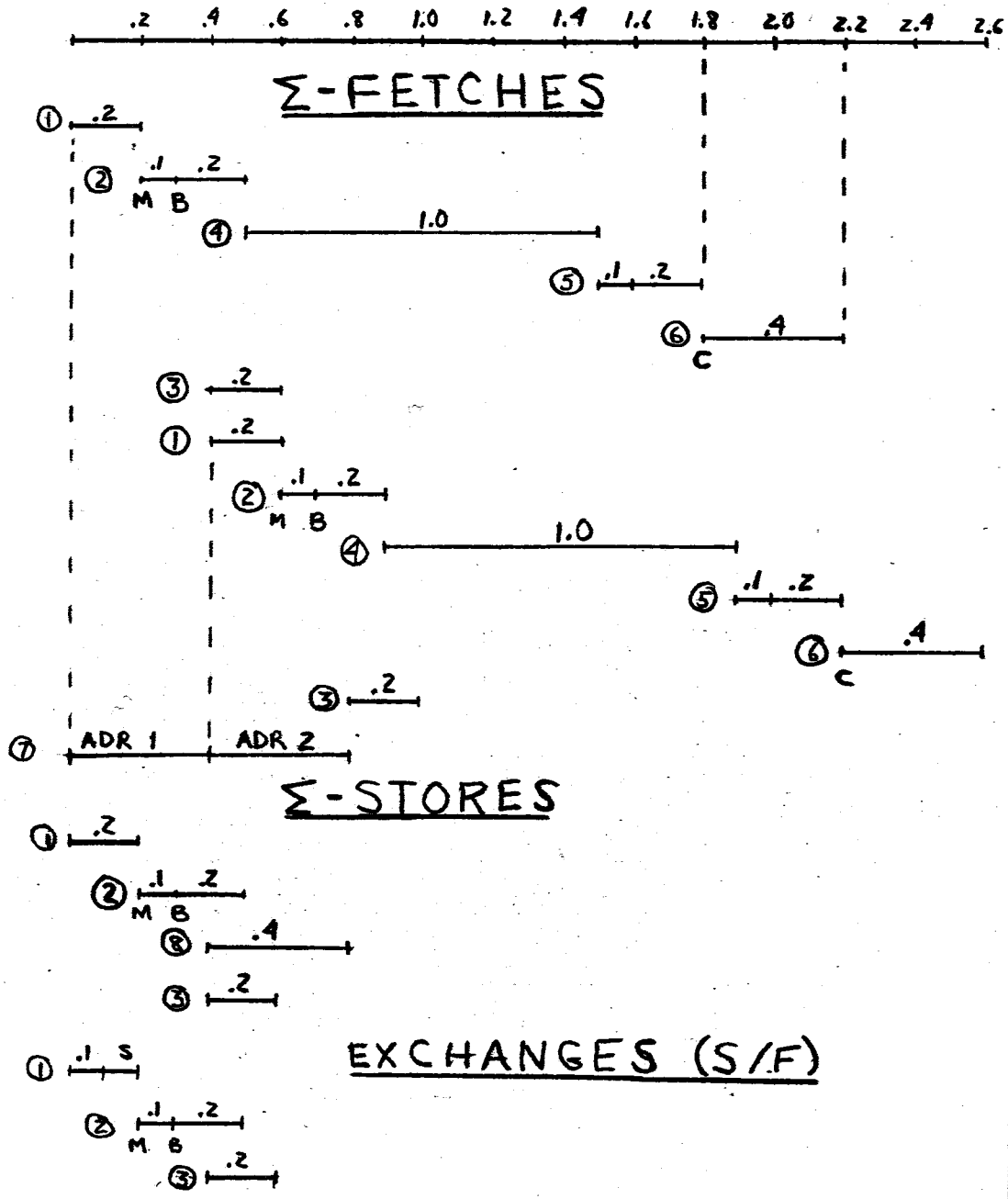


FIGURE 4 - OUT BUS CONTROLS
7,0,1,2
0,1,2,3
1,2,3,4
2,3,4,5
3,4,5,6
4,5,6,7
5,6,7,0
6,7,0,1
ST
AT
US
DE
CO
DE
RS
FROM BCU INPUT CONTROL
FETCH
SEL HS MEM
R.ADR IN BUS
R ADR RI CNTL
HIGH SPEED READ OUT SLOT SELECTOR
HS MEMORY RO DELAY BUS
MAIN MEMORY RO SLOT SELECTOR
R ADR IN BUS (DELAYED)
.1 μs
R ADR REGISTERS and STATUS TRIGGERS
R ADR OUT BUS
H R. ADR DECODE
H GATE SEL
X GATE SEL
Σ R. ADR DECODE
SEL RETURN REG GATE CNTL
Σ GATE SEL
RO RING CHK
R. ADR PARITY ERROR
BUS CNTL CHK
TO PNL KEY DATA GATE
.2 μs
EMPTY STATUS
FROM I-BOX
PNL KEY REQ
I/LA
Σ R. ADR
Σ PNL KEY ENTRY CNTL
L.O. ULFSPARRE
10-29-58

FIGURE 5 - ACCESS TIMES



① XMITS REQ TO BCU

② BCU FRAME DECODES & XMITS TO MEMORY

④ MAIN MEMORY ACCESS

⑤ MEMORY SYNCS & XMITS TO SIGMA

⑥ SIGMA CHECKS DATA

③ ACCEPT RETURNS TO REQUESTER

M - POSSIBLE HALT FOR BUSY MEMORY

B - " " " " BUS

C - " " " " CHECKER

⑦ ADDRESS GATES IN SIGMA

⑧ DATA GATES IN SIGMA

S - SYNCHRONIZATION TIME
0 - .2 μs OR .1 μs AVERAGE

L.O. ULFSPARRE
10-22-58

TABLE 1 - BUS USAGE & ACCESS

	BUS USAGE			MINIMUM ACCEPT RESPONSE	REQ'D MAX FETCH ACCESS	MAXIMUM MAIN MEM ACCESS	MINIMUM HS MEM ACCESS
	SERVICE RATE	SLOTS	%				
BASIC EXCHANGE	10 μs (max)	1/50	2%	.3μs	4.5μs	3.7μs	1.3μs
HIGH SPEED DISC EXCHANGE	3.5μs (max) 4.0μs (avg)	1/20	5%	.3μs	5.8μs	5.7μs	1.3μs
			X- 7%				
LOOKAHEAD	.6μs (max) 4.8μs (F.P. AVG)	1/24	4.2%	4μs	—	—	—
INST-BOX	.4μs (max) 3/1.6μs (F.P.AVG)	3/8	37.5%	.4μs	—	—	1.4μs
			Σ-41.7%				
		Σ SYSTEM	48.7%				
1 H.S. MEMORY	.6μs (max)	1/3	33⅓%				
1 MAIN MEMORY	2.0μs (max)	1/10	10%				
2 HSM & 4 M.M.		20/30+13/30	107%				
6 MAIN MEMORIES		6/10	60%				