SIGMA COMPUTER MEMO #19

MEMO TO: E. Bloch

SUBJECT: The use of a single address register in the Lookahead and the forwarding mechanism provided.

DATE: November 11, 1958

A. The lookahead address register contains, in general:

1. The address of the memory to which data is to be stored.

2. The address of the last memory from which a fetch was initiated if 1 does not apply.

For a floating point operation only one store instruction can be loaded but word boundary crossover can be accomodated. This is accomplished by keeping the next address in the working address register.

B. When the lookahead address register is utilized as in A-1, the following statements are implied in the present system.

1. Although other fetches may be initiated, they must all be compared with the lookahead address register.

2. Operand fetches, on comparison with the lookahead address register, will set up a forwarding mechanism to send the word to the loaded instruction when the operand becomes available.

3. Instruction unit fetches, on comparison with the lookahead address register, will be prevented from occurring until the operand becomes available in memory.

C. When the lookahead address register is utilized as in A-2, the following statements are implied in the present system.

1. Each new fetch will have its address entered in the lookahead address register.

2. Operand fetches, on comparison with the lookahead address

register, will set up a forwarding mechanism to send the word to the loaded instruction when the operand becomes available.

D. Index memory can be modified by the instruction unit ahead of sequence time. It is only necessary to store the old unmodified index value in the lookahead until it can be disposed of by the fact that an interruption did not occur previous to the modification. In this case, the index address is stored in the operation code field. There are, therefore, four index address pseudo-storing mechanisms.

The index memory is now, "ahead of the program", as it must be to index future instructions. Any storage into the index memory by an execution unit, not instruction unit must hold up the index memory until execution is achieved.

E. The forwarding mechanism consists primarily of tag triggers indicating the particular level that the lookahead address register is associated with, the particular level that the information must be forwarded to, and the controls for effecting the transfer.

Examples of the usage of the single address register are shown in the examples below where the program steps are broken down into per level forms of communication. Levels are here designated A, B, C and D.

I. VFL Add to Memory
No. Program

1. VFL Add to Mem 1000
2. VFL Add to Mem 1000
3. VFL Add to Mem 1000-1001
4. VFL Add to Mem 1001
5. VFL Add to Mem 1001

No. Level Per level program
1A VFL Add to Memory
1B Fetch 1000
1C Store 1000
2D VFL Add to Memory
2A Fetch 1000 (forwarded from C)
2B Store 1000

SIGMA COMPUTER
MEMO #19

November 11, 1958

3C VFL Add to Memory
3D Fetch 1000 (forwarded from B)
3A Fetch 1001
3B Store 1000
3C Store 1001
4D VFL Add to Memory
4E Fetch 1001 (forwarded from C)
4F Store 1001 etc.

II. Floating Point Sequence

No. Program Step

1. Count and Branch
2. Load 1000
3. Subtract 2000
4. LCMD 3000
5. Cmpy 5000
6. Store 6000
7. Count and Branch
8. Load 1001
9. Subtract 2001
10. LCMD 3001
11. Cmpy 5001
12. Store 6001

No. Level Per level program step

1A Old index value
2B Load 1000
3C Subtract 2000
4D Fetch 3000
4A Store to M.R.
5B Cmpy M.R. (forwarded from A)
5C Cmpy 5000
6D Store 6000
7A Old index value
8B Load 1001
9C Subtract 2001
10D Fetch 3001
10A Store to M.R.
11B Cmpy M.R. (forwarded from A)
11C Cmpy 5001
12D Store 6001

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