

J. Kolesky

SIGMA COMPUTER MEMO #6

SUBJECT: The Cascode Multiple Gate

BY: O. L. MacSorley

DATE: February 24, 1958

The cascode multiple gate was used as part of the transistorized byte selector unit in the Harvest Data Flow Model. Later a special-purpose single-output model of it was approved for use by the Memory Group.

The purpose of this memorandum is to discuss the general cascode gate and some of its applications. This circuit is compatible with the present transistor standard circuits, and it is recommended that it be included in the approved circuit list.

The cascode gate operates in the same manner as the present standard units, except that it has two levels of control in a current path instead of one. Since most of the delay in these circuits occur when the current is transformed into a voltage to control the next current, this means that in some applications the cascode gate can perform two levels of logic before transforming the current into a voltage. This permits a reduction in the time required to perform some logical operations. In other applications it has other advantages, most of which can lead, either directly or indirectly, to an improvement in operation speed. Some of these will be described later.

Figure 1 shows a typical example of the gate in detail. As may be seen, the circuit may be divided into two major parts. These are shown separately in Fig's. 2, 3 and 4. The coupling networks used are shown in Figure 5.

Figures 2 and 3 show the emitter current block. These represent controllable current sources which replace the current determining resistor of the present standard circuits. This has been called the Emitter Current Block because it supplies emitter current to the other block. Since these work about +6 volts or -12 volts, one of the special coupling networks shown at the top of Figure 5 is required between the output of an N-type or P-type logical block and the input of an Emitter Current Block. The transistor 'T₃' may be omitted if no logical operation is required at this level.

SIGMA COMPUTER
MEMO #6

February 24, 1958

The second block has been called the Logical Current Unit because it controls the path of the current produced by the Emitter Current Block in accordance with the circuit logic. This block differs from the present logical block in that its current source is external and that all collector connections are brought out separately. Its outputs require the same coupling networks and have the same driving capabilities as the conventional N-type or P-type logical block.

One particularly useful application of the Cascode Multiple Gate is as a shifter on the output of a register. This application requires the use of a number of 'and' circuits on each output of a register, each producing a different amount of shift. Applications requiring as many as eight possible degrees of shift have been encountered. Using conventional circuits this would require the insertion of a driver ahead of the logic, which makes a total of nine cards, twenty-six transistors and eight units of current. Since only one shift position would be required at one time, the circuit shown in Figure 1 could be used for this purpose. Assuming that single level control only is required, the Emitter Current Block would contain two transistors. The Logical Current Unit would require a total of nine transistors, one more than the number of 'and' circuits. Assuming three transistors per card, this would be three cards. This makes a total of four cards, eleven transistors, and one unit of current. For a hundred-bit unit this makes 400 cards, 1100 transistors, and 100 units of current as against 900 cards, 2600 transistors, and 800 units of current. Since cards take space, and space takes time, there is also a time improvement factor.

Figures 6 and 7 show a particularly useful special connection of the Multiple Cascode Gate. It has three inputs and two outputs. With two of these inputs connected together it becomes an exclusive 'or' that does not require both true and complementary inputs and does not have the possibility of spikes of excessive currents in the output as a result of improper phasing of the inputs. Figure 8 shows the exclusive 'or' circuit in block form.

If the three inputs are kept separate, the circuit becomes a carry signal generator for an adder. For this it requires that the signals $(A_1 + \bar{B}_1)$, B_1 , and C_0 be available to get C_1 . This circuit is shown in block form in Figure 9.

Figure 10 shows a full adder using these circuits. It requires a total of 20 transistors per bit. It should be noted that when using this adder circuit in a ripple carry adder, the carry path is one logical level per bit.

Figure 11 shows a variation of the Carry Generator circuit which may be used with the adder if desired. It gives the same outputs, but does not require the

SIGMA COMPUTER
MEMO #6

February 24, 1958

previous formation of $(A_1 \nabla B_1)$.

Figure 12 shows a signal distribution system in block form, together with the same circuit using only the present standard circuits.

The above has shown some of possible uses of the cascade multiple gate. It is not proposed as a special circuit or as a new type of circuit to displace the present standards, but as a variation of the present circuits that has sufficient special advantages and wide enough potential usage to be included in the approved standard circuit listing.

The circuit breakdown, method of representation, and block names were developed for this report, and are not approved standards.

O. L. MacSorley

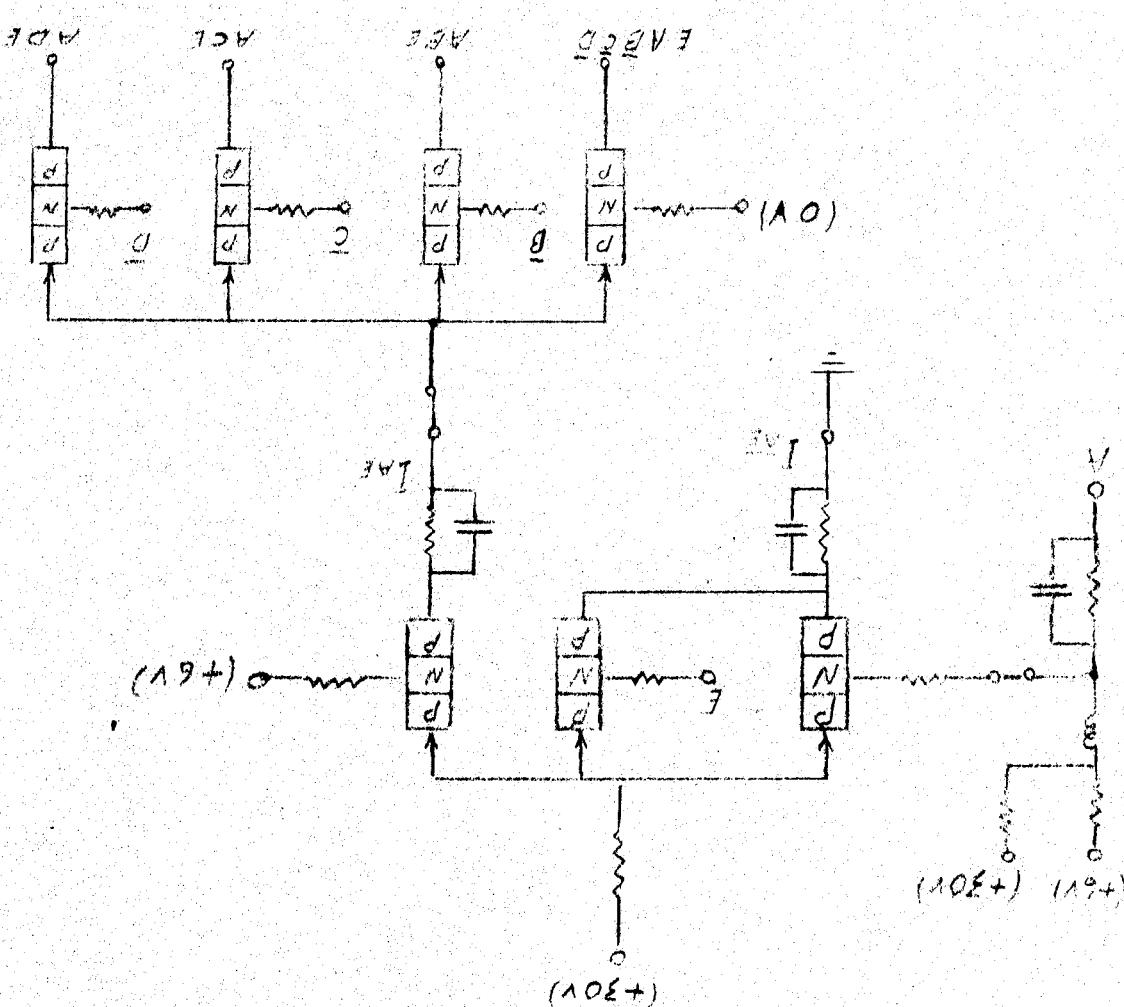
O. L. MacSorley

OLMS:bjn

858
FEBRUARY 13, 1958
O.L. MAC GEE, JR.

FIGURE 1

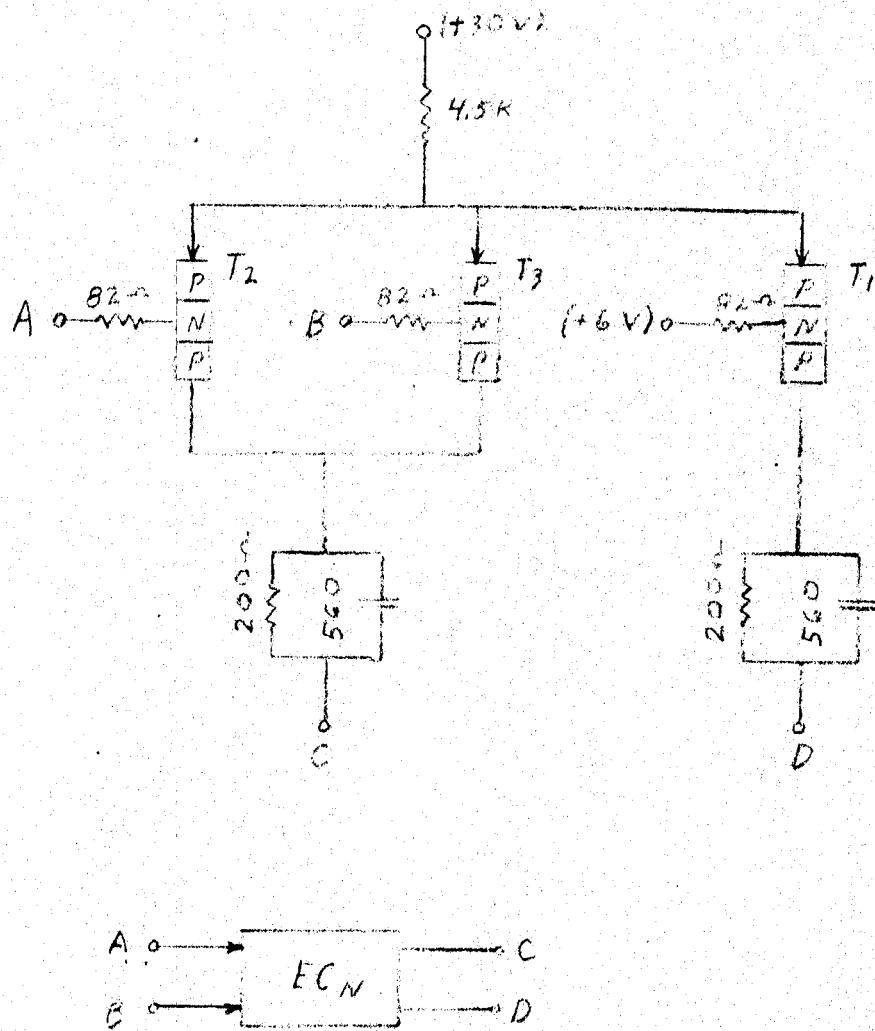
The F-input transistor may be omitted if desired.
The output of the circuit is shown in Figure 1.



Cascode Multiple Gate

(Gates omitted)

Emitter Current Block
(N-Type)



This is a current switching block.
When A and B are both up, current
will be supplied to D .

If A or B is down, current will be
supplied to C .

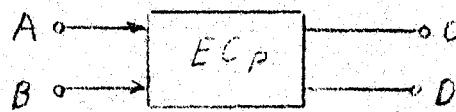
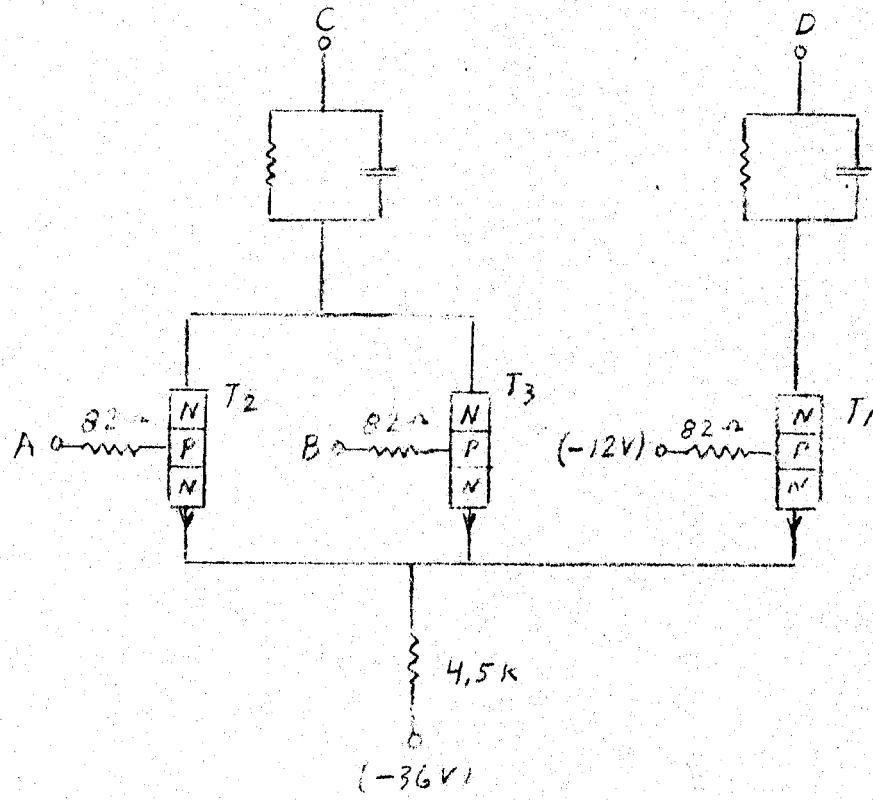
C and/or D are current sources for
a Logical Current Unit (N-type).

Transistor T_3 may be omitted if desired.

Figure 2

O. L. Mac Sorley
February 19, 1958

Emitter Current Block
(P-type)



This is a current switching block.
When A and B are both down, current will be supplied to D.

If A or B is up, current will be supplied to C.

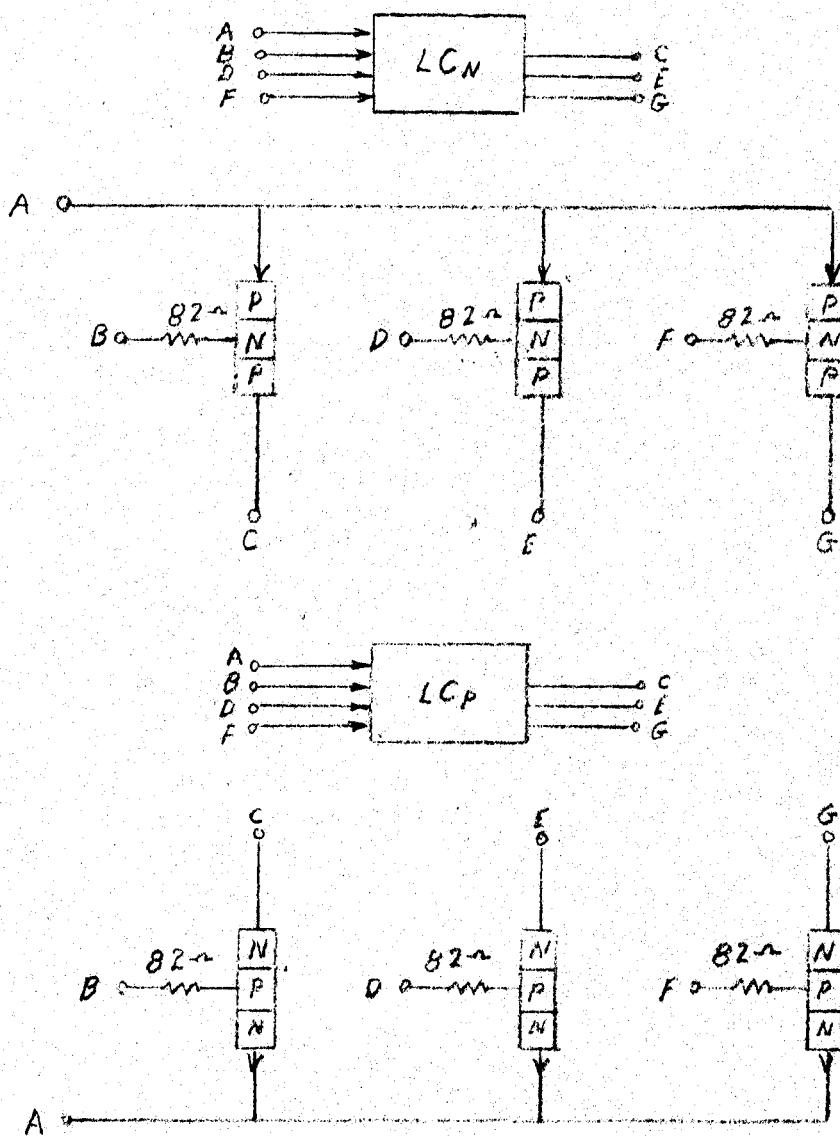
C and/or D are current sources for a Logical Current Unit (P-type).

Transistor T₃ may be omitted if desired.

Figure 3

O. L. Mac Sorley
February 19, 1958

LOGICAL CURRENT UNIT



On the logical block, the top input is always the emitter current input.

The other inputs are base inputs. The output for a particular transistor is shown in line with its input. Thus B and C are in line, also D and E, and F and G.

Figure 4

O. L. Mac Sorley
February 19, 1958

LOADS
(COUPLING NETWORKS)

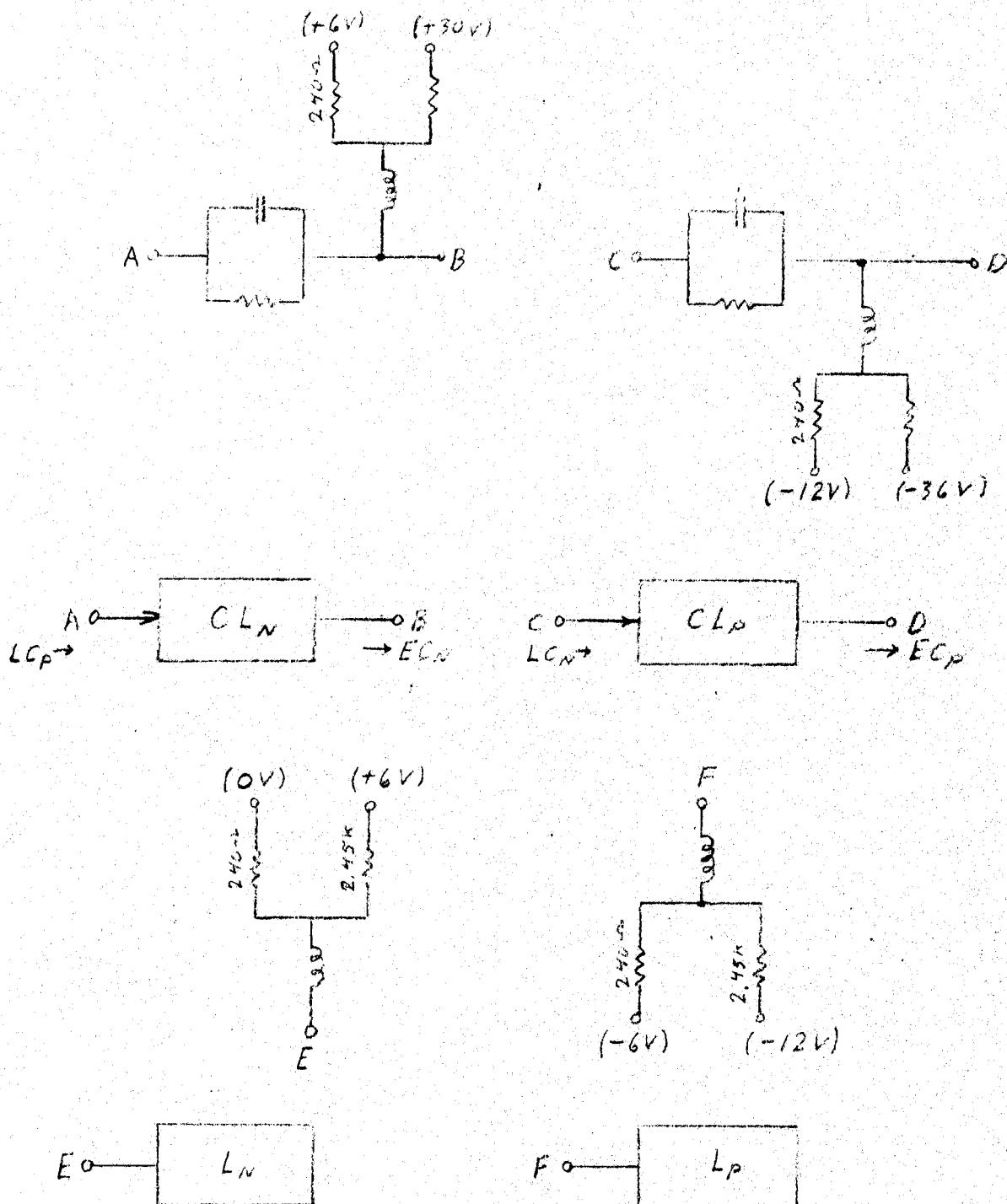
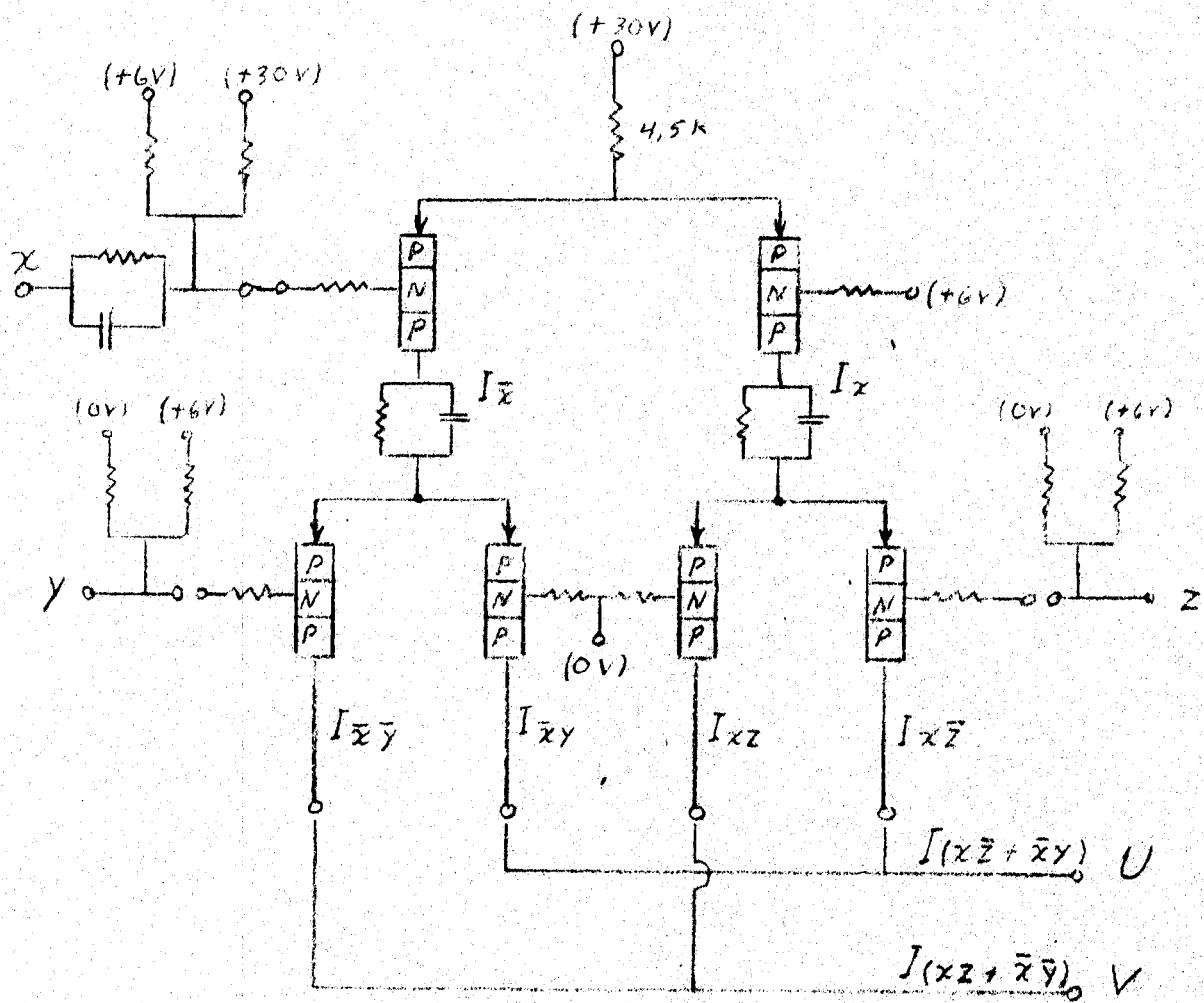


Figure 5

O. L MAC SORLEY
FEBRUARY 19, 1958

CASCODE MULTIVIBRATOR GATE (N)
(Special Application)



$$U = X\bar{Z} + \bar{X}Y$$

$$V = XZ + \bar{X}\bar{Y}$$

$$\text{Let } Y = Z = A \quad X = B$$

$$U = B\bar{A} + \bar{B}A = A \vee B \quad V = BA + \bar{B}\bar{A} = (\bar{A} \vee B)$$

$$\text{Let } X = (A \vee B), \quad Y = \bar{B}, \quad Z = C_0$$

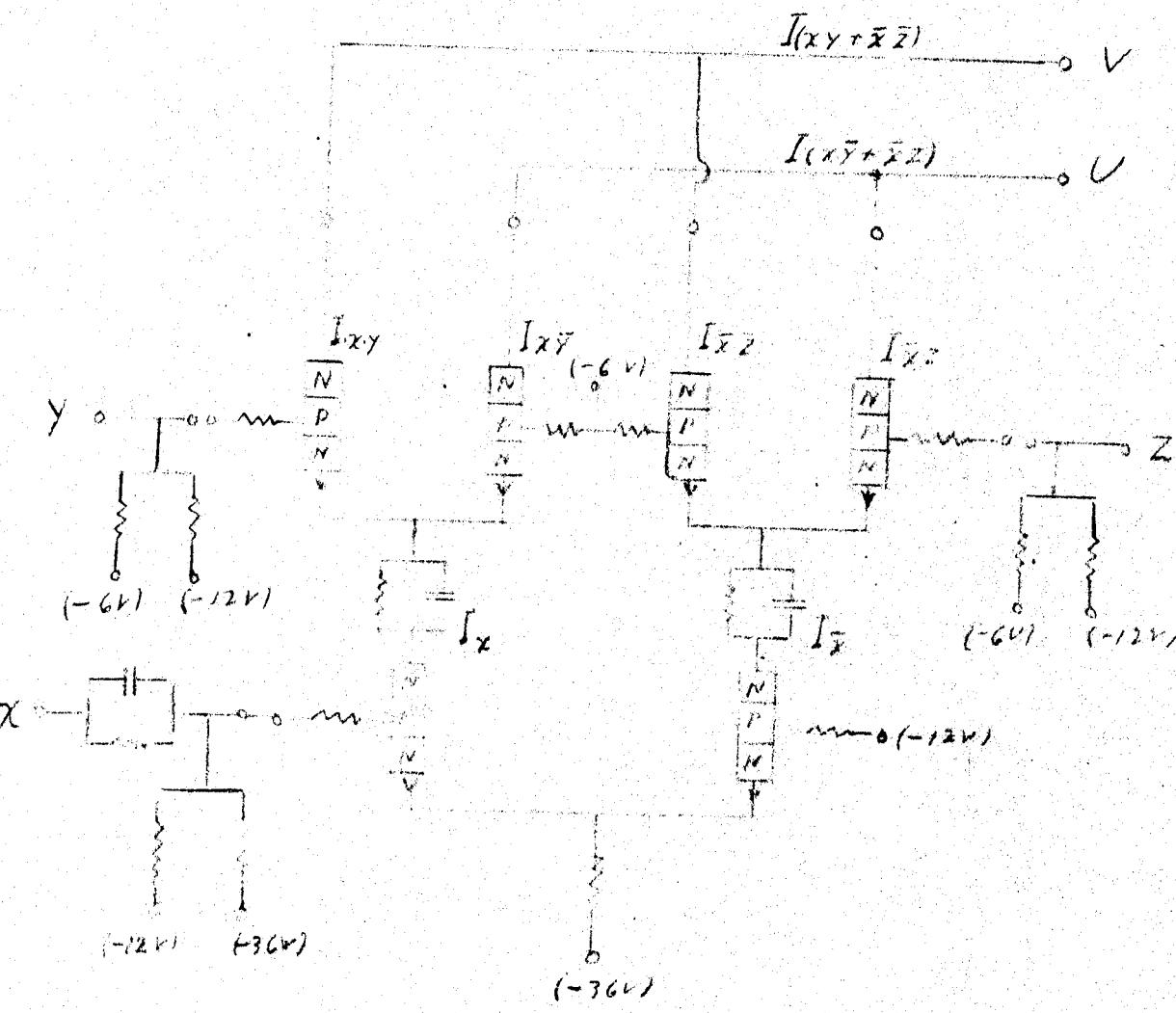
$$U = (A \vee B,) \bar{C}_0 + (\bar{A} \vee B,) \bar{B} = A, \bar{B}, \bar{C}_0 + \bar{A}, B, \bar{C}_0 + \bar{A}, \bar{B}, \bar{B}, + A, B, \bar{B}, \\ = A, \bar{B}, \bar{C}_0 + \bar{A}, B, \bar{C}_0 + \bar{A}, \bar{B}, C_0 + \bar{A}, B, \bar{C}_0 = \bar{C}_1$$

$$V = (A \vee B,) C_0 + (\bar{A} \vee B,) B = A, \bar{B}, C_0 + \bar{A}, B, C_0 + ABB + \bar{A}\bar{B}B \\ = A, \bar{B}, C_0 + \bar{A}, B, C_0 + AB\bar{C}_0 + A, B, C_0 = C_1$$

Figure 6

O. L. NIAC SORLEY
FEBRUARY 18, 1958

Cascaded Multiple Gate (PM)
(Special Application)



$$V = XY + XZ$$

$$V = X\bar{Y} + \bar{X}Z$$

$$\text{Let } Y = Z = A, \quad Z = B$$

$$\text{Then } V = BA + AB = A \oplus B$$

$$U = BA + \bar{A}\bar{B} = A \oplus B$$

$$\text{Let } X = (A, \oplus B), \quad Y = \bar{C}_o, \quad Z = B,$$

$$\text{Then } V = (A, \oplus B) C_o + (\bar{A}, \oplus B) B = A\bar{B}_o C_o + A, B, C_o + A, B, \bar{C}_o = C_o$$

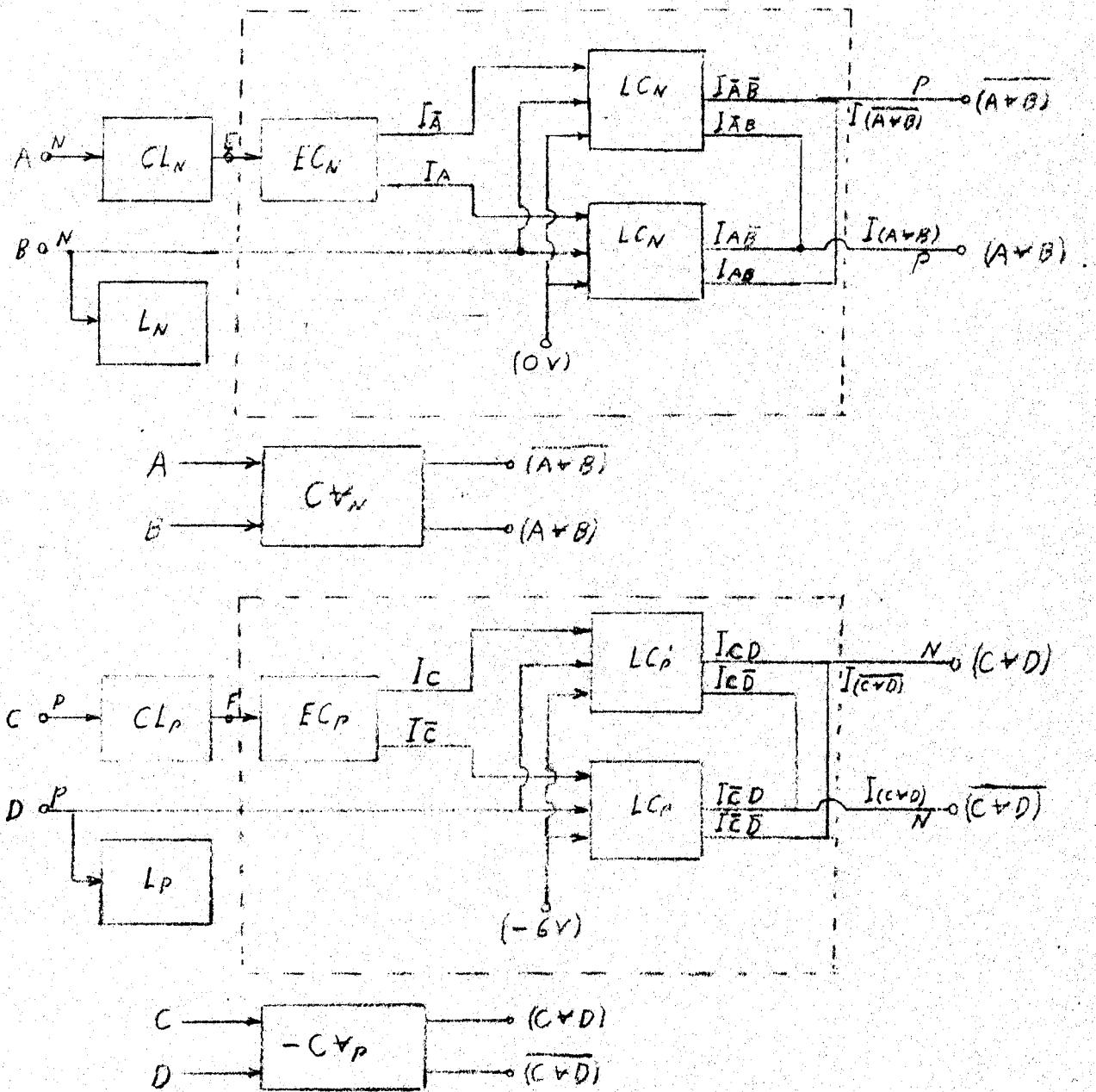
$$U = (A, \oplus B) \bar{C}_o + (\bar{A}, \oplus B) \bar{B} = A\bar{B}_o \bar{C}_o + \bar{A}, B, \bar{C}_o + \bar{A}, \bar{B} = \bar{C}_o$$

Figure 7

D. in. M. S. J. 1958

February 21, 1958

Cascode Exclusive OR



Note that a second logical block may not be connected at point A or C.

A second EC may be connected at E' or F. A second logical block may be connected at B or D.

Figure 8

O. L. MAC SOLLEY
FEBRUARY 19, 1958

Carry Generating Circuit
(A + B) AVAILABLE

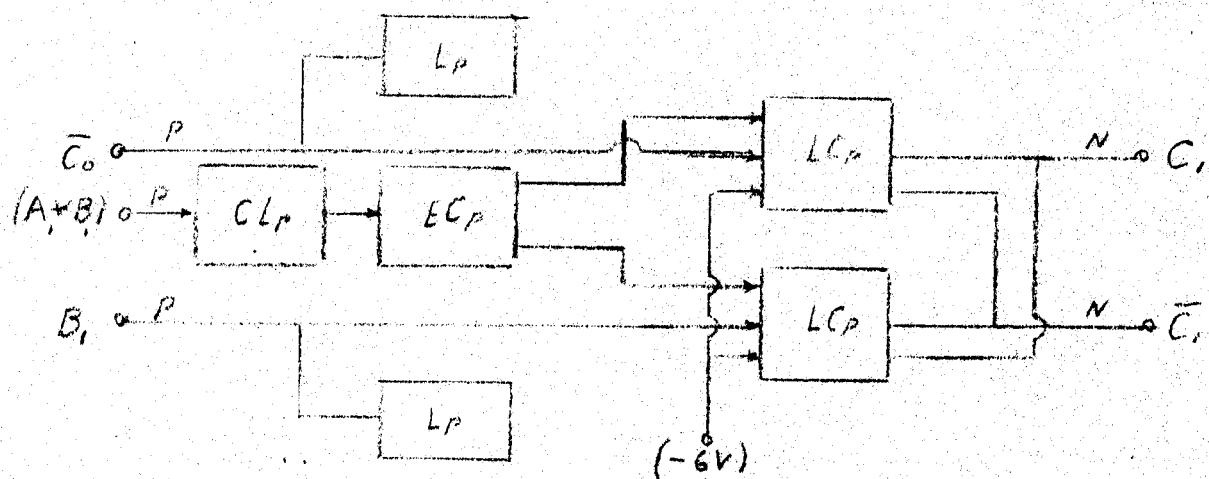
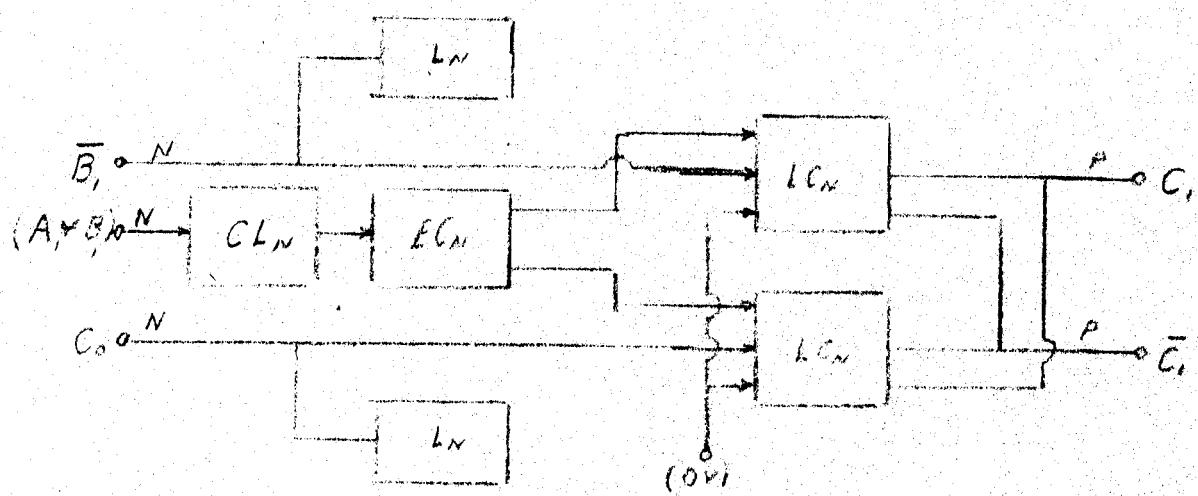


Figure 9

O. L. MAC SORLEY
FEBRUARY 21, 1958

Full Address (One Octet)
(20 Transistors)

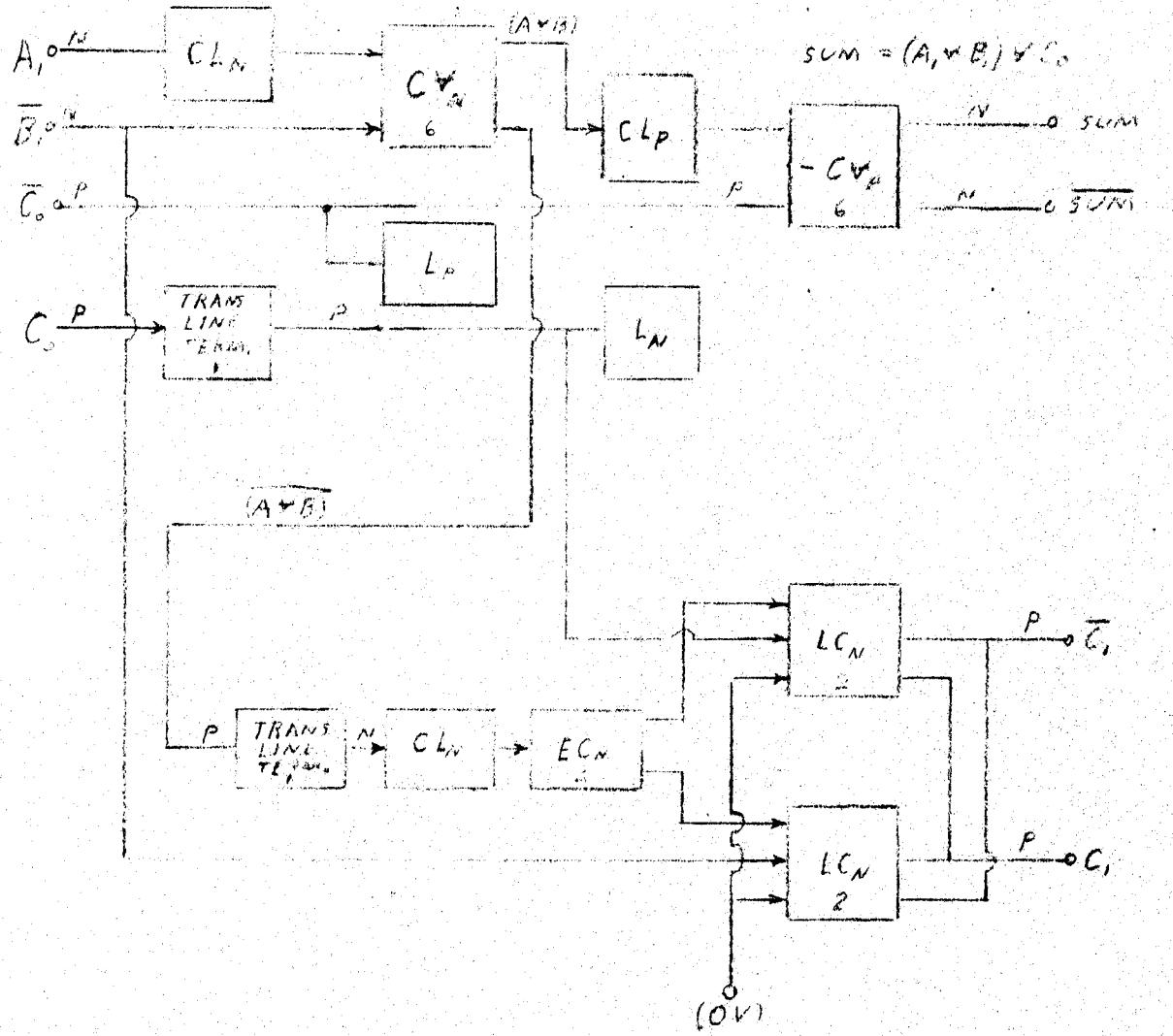
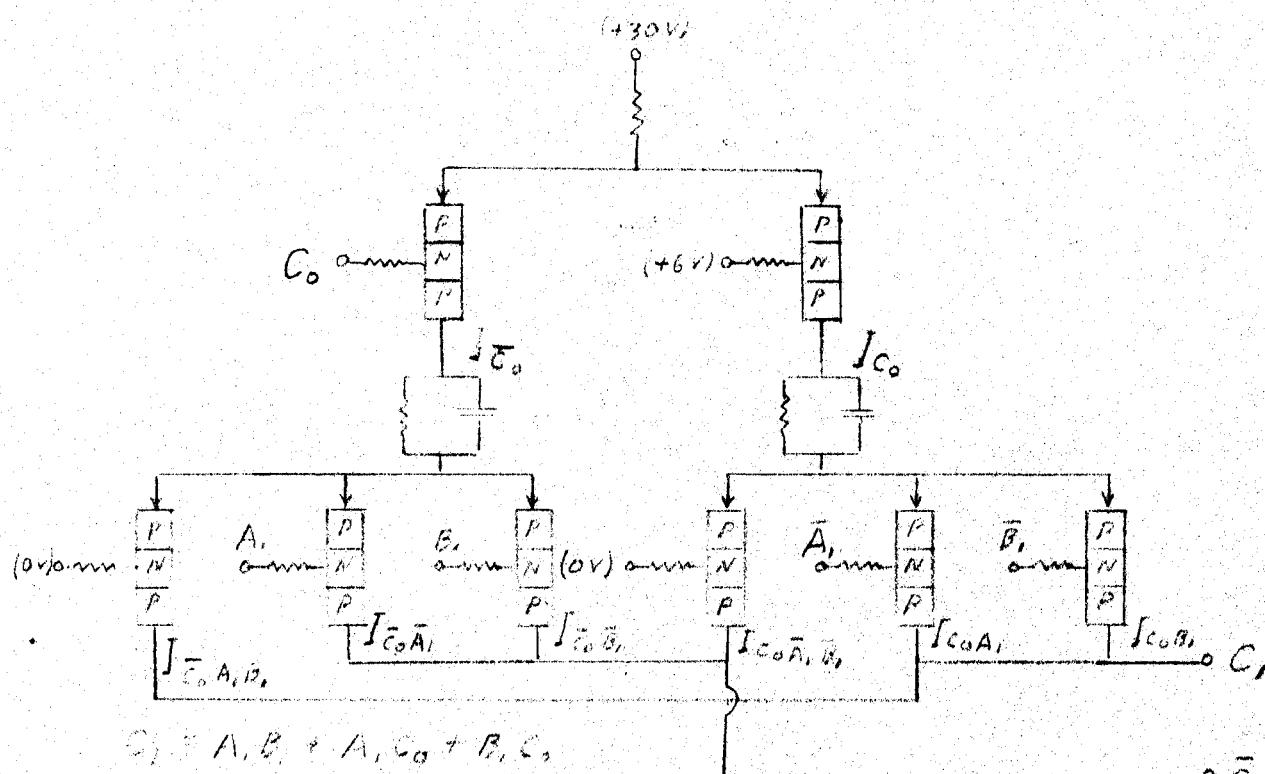


Figure 10

D.L. MAC SORLEY
FEBRUARY 22, 1958

Carry Synchronizer



$$C_o = A_1 B_1 + A_1 C_o + B_1 C_o$$

$$\bar{C}_o = \bar{A}_1 \bar{B}_1 + \bar{A}_1 C_o + \bar{B}_1 C_o$$

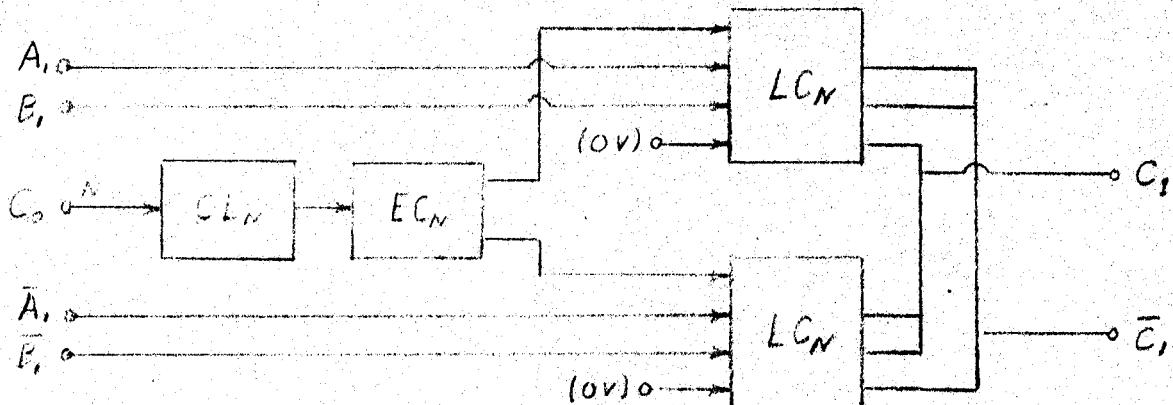
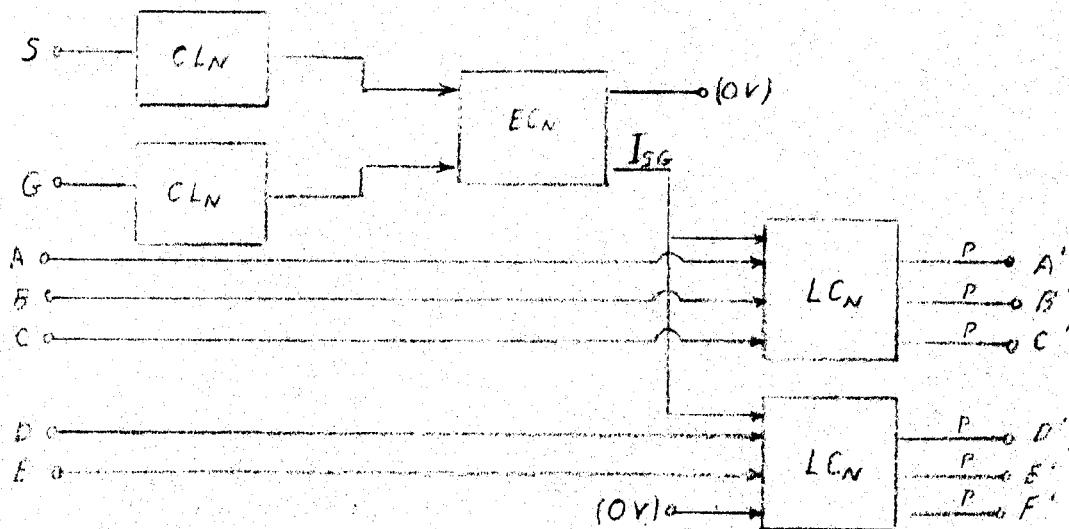


Figure 11

O. S. Macmillan
February 20, 1958

Cascade Multiple Gates
(Typical Examples)

(12 TRANSISTORS)



EC supplies current to the LC unit when S(signal) and G(gate) are both up.

A, B, C, D, E direct current to their respective outputs when down. Not more than one may be down at any one time. F' receives current when all inputs are up.

Equivalent Circuit using Present Blocks

(22 TRANSISTORS)

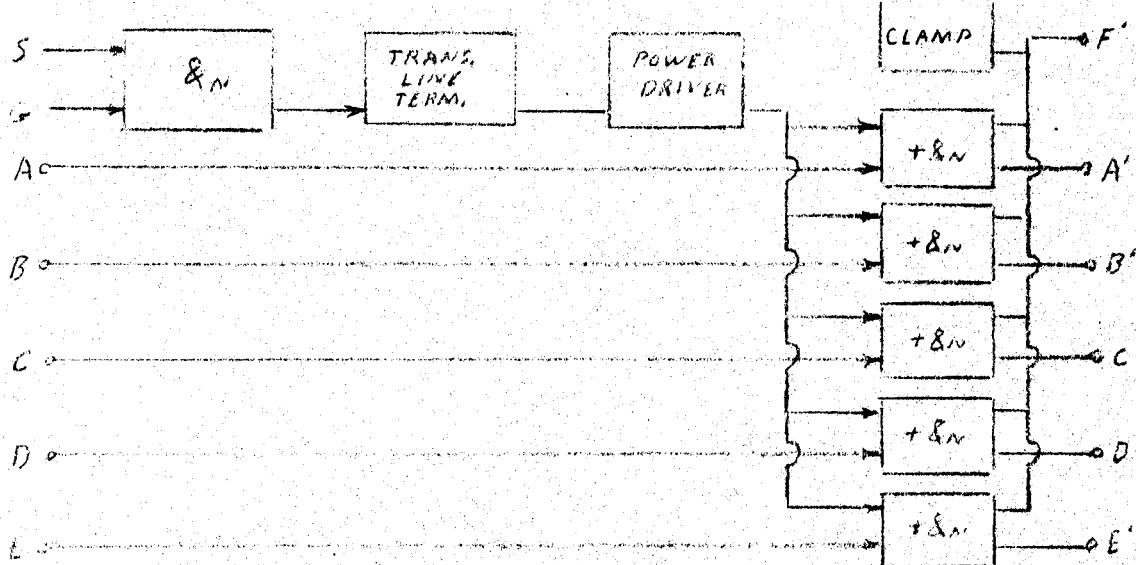


Figure 12

O. S. Max. - WORKS
February 20, 1958