H. Kolaky

SIGMA COMPUTER MEMO #2

SUBJECT: Proposal for a Sigma Lookahead System.

BY: R. J. Bahnsen and J. F. Dirac

DATE: December 31, 1957

I. Introduction

The purpose of this memo is to describe the functional operation of the Sigma Lookahead System and the interconnections implied with other units of the Sigma-Basic System.

II. Design Objectives

The Sigma Lookahead System will act as high speed memory buffer for indexed instructions, store operations in general, and data memory accessing for the Sigma Arithmetic and Basic Execution Units. The Lookahead System must coordinate and sequence the effects of overlap operation of the Basic Instruction and Execution Units, Sigma Arithmetic Unit, and instruction and data memory references. Figure 1 illustrates the information connections of the Sigma Lookahead System with other units.

III. Necessary Relationships with other Units.

Note: The term "normally" as used below means the function performed when the Basic System is operating alone.

A. Basic Instruction Unit I Box

1. Stores and indicator register modifications normally performed by the Basic Instruction Unit are buffered in the Lookahead System registers. It is necessary for the I box to keep an "updated" indicator set that is influenced by themselves so that indicator branches may be properly executed if the branch refers to one of these indicators. The addressable indicator register is modified at some later time by the Lookahead System which, when operating, executes all stores.

2. Instruction counter values must be compared with effective addresses stored in the Lookahead System when a store is contained in the Lookahead. This must be

done before a memory reference is initiated to prevent procuring an old unaltered instruction from memory.

3. For the same reason, index addresses from the I or J fields must be compared when an "unexecuted" store exists in the Lookahead before the index register can be gated out for usage. When the compare exists, the Basic Instruction Unit procures the information from the Lookahead System directly when the information is ready.

4. Indexed addresses which are to be stored in the Lookahead System must be compared with address sections of Lookahead System storage registers. This comparison must be completed and control equipment set before I box can continue processing. The comparison prevents superfluous and incorrect memory references.

5. The Memory Bus and Hamming checker generator normally shared between the Basic Instruction and Execution Units is utilized by the Basic Instruction Unit alone.

6. The internal bus normally shared by Basic Instruction and Execution Units is split into two parts. It is restored when the Lookahead System is empty and bypassed.

7. Index registers and data sections of Lookahead System storage can be gated onto the I box internal bus.

8. Effective address and operational tags are generated in the Basic Instruction unit to facilitate processing in the Lookahead System. Examples of conditions which must be recognized before insertion into the Lookahead System are:

    a. A full word instruction occupying a full level of a lookahead register.
    b. A word boundary crossover.
    c. A Progressive indexing indication.
    d. An internal bring.
        (i) refers to an address whose contents will be modified directly by the I box.

(ii) which refers to an address whose contents will not be modified by the I box

e. An internal store
f. An external store
g. An "add to memory"
h. An "empty Lookahead" signal.
i. A "breakin or interrupt requested, house-clean Lookahead so I can continue" signal.
j. Generally speaking, elementalized instructions.

9. Basic Instruction Unit processing must be contingent upon control signals indicating available storage space and information in the Lookahead System.

10. Indicator branches which are indicated by bit positions not influenced by the I box are not in the updated indicator register. These tests must be delayed until the Lookahead System is empty. See note following figure 9.

11. Instruction counter values corresponding to one plus the address of the indexed instruction must be supplied to the Lookahead System with the indexed instruction. This value of the instruction counter is the address to be stored during an interrupt procedure.

12. I box instructions which result in indicator changes must store such indicator changes in the Lookahead System. Actual changes of the indicator register are thus deferred until the proper time when they are executed by the Lookahead System.

13. Index register modifications which are buffered in the Lookahead System as internal stores are assumed to include parity bits.

B. Sigma Arithmetic Unit

1. Recognition of the operation code will be made by the Sigma Arithmetic Unit.

2. Sigma Arithmetic Unit processing must be contingent upon control signals indicating available storage space and information in the Lookahead System.

3. This unit will set information into Basic Execution Unit's registers A, B, C or D as required by the Sigma arithmetic operation.

4. The operand specified by the effective address of the Sigma instruction will be located in the data section of the same lookahead register when the start main arithmetic unit operation signal is initiated.

5. Information to be stored in a memory address will be loaded into the Lookahead System register provided.

C. Basic Execution Unit

1. The memory references normally initiated by the unit will not be available when the Lookahead System is attached and functioning.

2. Recognition of the operation code will be made by the Basic Execution Unit.

3. Basic Execution processing must be contingent upon control signals indicating available storage space and information in the Lookahead System.

4. The unit will recognize a lookahead system level tagged as CI (continuous instruction) as a full word instruction to be obtained in the data section of the lookahead register.

5. The unit will recognize a TW tag on the CI tagged instruction as indicative of a data word boundary crossover and will then wait for the successful acquisition of the next two levels of lookahead for actual data words.

Memory Bus Request Analyzer

1. Separate 0.5 and 2.0 microsecond memory OUT buses are required for the Basic Instruction Unit and Lookahead System service to prevent information return coincidence.

2. Separate bus request mechanisms are required for the Basic Instruction Unit and Lookahead System. The Lookahead System should have priority over the Basic Instruction Unit.

3. The Memory IN bus information lines will only be required by the Lookahead System when it is functional.

4. Information coming from memory will be gated directly to a specific register indicated by the return address. This will generally be one of five data registers in the Lookahead System or two registers in the Basic Instruction Unit. Lookahead System registers are planned for acceptance of data at any time.

IV. Lookahead System Storage Register Bits

Figure 2 shows a typical Lookahead System storage level with input and output gates. A listing of bit allocations is given below. Also given below is an explanation of the function performed by each section of the lookahead storage register.

A. Nomenclature and Number of Bits

Instruction Counter (plus one)	19 bits
Effective Address	18
Parity or Hamming Bits	8
Data	64
Operation Code	10
Indicators	19
Indicator Control Bits	3
Forwarding Address	5 or 3
Control Bits as follows	
F (orwarding) bit	1
C (ompare) Bit	1
OK Bit	1
Hamming Bit	1
Internal B ring Bit	1
Internal Store Bit	1
External Store Bit	1
Continuous Instruction Bit	1
Two Word Bit	1

B. Definition of Functions Stored

1. Instruction Counter (plus one)

This value represents the instruction address immediately following the instruction whose operation code, effective address, and data are stored at the same level of lookahead.

2. Effective Address

The effective address in a lookahead register indicates the memory location of the operand to be used in the execution of the instruction stored in this lookahead register.

3. Parity or Hamming Bits

Used with the data bits, these will be set for Hamming code upon arrival at the Lookahead System before verification by the checker, or immediately before initiating a store request to the Bus System. At all other times, for computer availability, they will contain parity bits appropriate for 8 bit bytes.

4. Data Bits

These bits contain the information located in or to be stored at the memory location specified by the effective address in the same level of lookahead. The OK bit setting indicates whether or not the information is present in the data section. The H bit and store bits are also used to indicate the "condition" of the data present.

5. Operation Code

This value specifies the operation required at the particular level of lookahead.

6. Indicators

Because of possible program interruption, it is important to insure, with a Lookahead System, that indicator bits are set in their proper time sequence. Therefore it is neces-

sary to store the indicator bits modified by the Basic Instruction Unit in the Lookahead System. Since some branching may be done on these indicator signals by the I box, however, a "pseudo" or "updated" indicator register of the same number of bits must be kept in the I box for its own interrogation. The bits are assumed to be the following:

(1)	Control Check	Bit 0
(2)	Memory Check	Bit 2
(3)	Operation Code Invalid	Bit 16
(4)	Operation Code Valid for S Only	Bit 17
(5)	Operation Code Valid for H Only	Bit 18
(6)	Address Invalid	Bit 19
(7)	Execute Exception	Bit 20
(8)	Instruction Location Match	Bit 22
(9)	Instruction Location Non-Match	Bit 23
(10)	Effective Address Match	Bit 24
(11)	Effective Address Non-Match	Bit 25
(12)	Index Flag	Bit 26
(13)	Index Count = 0	Bit 50
(14)	Index Result 0	Bit 51
(15)	Index Result = 0	Bit 52
(16)	Index Result 0	Bit 53
(17)	Index Comp. Result Low	Bit 54
(18)	Index Comp. Result Equal	Bit 55
(19)	Index Comp. Result High	Bit 56

7. Indicator Control Bits

These bits determine whether the status of indicator bits 50, 51 to 53, or 54 to 56 is to be effected by the operation.

8. Forwarding Address

This address specifies what other level of the lookahead system the data at this level is to be sent in the event of a comparison of effective addresses. The forwarding is

performed immediately after the execution of the arithmetic operation indicated and before an external store is initiated.

9. F (orwarding) Bit

The Forwarding bit indicates whether or not the forwarding of data present at a level should take place to another level.

10. Compare Bit

The compare bit indicates that the effective address contained at that level should be compared with interrogating information. (i.e.: instruction counter, new effective address)

11. OK Bit

The OK bit indicates that the data specified by the effective address

a. has arrived from memory (or)
b. has been set by the Basic Instruction unit for storage in an index register. (or)
c. has been set by an arithmetic unit for storage.

The particular condition involved is determined by the condition of the store bits.

12. H Bit

The H bit indicates whether (1) the information is in parity form or (0) in Hamming code form or unusable by the computer.

13. Internal Bring Bit

The internal bring bit designates that the effective address refers to an internal register and fetching is delayed until immediately previous to execution.

14. Internal Store and External Store Bits

The store bits at a particular level of lookahead designate the operation contained at that level in the following manner:

IS	ES	Instruction
0	0	No store instruction
0	1	Store to External Memory
1	0	Store to on Internal Register
1	1	An Add to Memory Will become an internal or external store

15. Continuous Instruction Bit

The continuous instruction bit designates the lookahead register level containing a full word instruction applicable to the Basic Execution unit.

16. Two Word Bit

The two word bit designates a word boundary crossover when set with the continuous instruction bit. When the bit is set with no continuous instruction bit, it indicates a level of lookahead where information is stored to be used in the execution of an instruction which was contained in an "earlier" level of lookahead.

V. Lookahead System Control Elements or Commutators

A. General

There are four commutating elements associated with the lookahead storage registers. They are:

1. Instruction Unit Counter
2. Memory Reference Counter
3. Hamming Check Counter
4. Main Arithmetic Unit Counter

The value of each of these counters indicates a lookahead register (the register whose address corresponds to the counter value) which is to be operated upon by the particular unit. The counters are cyclic. That is, after reaching its maximum value the counter returns to its initial value and again counts up. The counters are interlocked such that no counter is allowed to pass any other counter. This keeps the counters in sequence, the sequence being listed above.

B. Description

1. Instruction Unit Counter

This commutator designates the lookahead register to be used by the Basic Instruction Unit as a buffer for execution commands, index modifications and indicator settings. If an external store bit is on at the level indicated by this commutator, the store must be initiated before the level becomes available to the Basic Instruction Unit.

2. Memory Reference Counter

This commutator designates the lookahead register for which a bring memory reference is to be initiated. This commutator "skips" the levels where an external store, internal bring or store, or instruction continuation is indicated.

3. Hamming Check Counter

This commutator designates the lookahead register whose data field is to have:

a. Hamming checked and parity generated.
b. Parity checked and hamming generated.

It is planned that the commutator will skip internal stores and brings.

4. Main Arithmetic Unit Counter

This commutator designates the lookahead register on which the Basic Execution Unit or Sigma Arithmetic Unit is operating. Internal stores will be executed at this level. When the lookahead Register Address in the Main Arithmetic Unit Counter equals the Lookahead Register Addresses in all other counters and the operation is complete, the Lookahead System is empty if no external stores are in the Lookahead System.

VI Lookahead System Functioning

Figure I illustrates the functional interconnections of the Sigma Lookahead System with the other units of a complete Sigma System. Figure 2 illustrates the format of a particular storage level of the Lookahead System with the gating to be used into and out of the particular level. Referring to these diagrams, the functional relationships are as follows:

A. Basic Instruction Unit or I Box

This unit sends instruction counter, operation code, and effective address values after procurement and manipulation to the Sigma Lookahead System. This is shown in figures 3 and 5. In addition, index register modifications must be stored in the Lookahead System for eventual execution in their proper sequence. The data and parity bit information gating is shown in figure 4. Indicator changes and control bit settings are also required for information storage in the Lookahead System. The gating to accomplish this is shown in figures 6 and 7.

B. Bus Control Unit

This unit receives memory store or bring requests from the Sigma Lookahead System as well as the Basic Instruction Unit. The effective addresses are those previously indexed by the I box. The return address with the memory request specifies the particular Lookahead System register to which the data is to be returned. If the memory bus control does not prevent the simultaneous return of information from 0.5 and 2.0 microsecond memory, then separate input data buses are required as shown in figure 4.

C. Basic Execution Unit or E Box

This unit recognizes operation codes which it is to perform via the gating shown in figure 5. The operand is obtained directly from the Lookahead System by means of the data gating shown in figure 4. Store type instructions require the transmission of data words back into the Lookahead System for eventual storage by that System into main memory.

D. Sigma Arithmetic Unit

This unit performs in the same manner as the Basic Execution Unit on those instructions which it is designed to handle.

SIGMA COMPUTER
MEMO #2

December 31, 1957

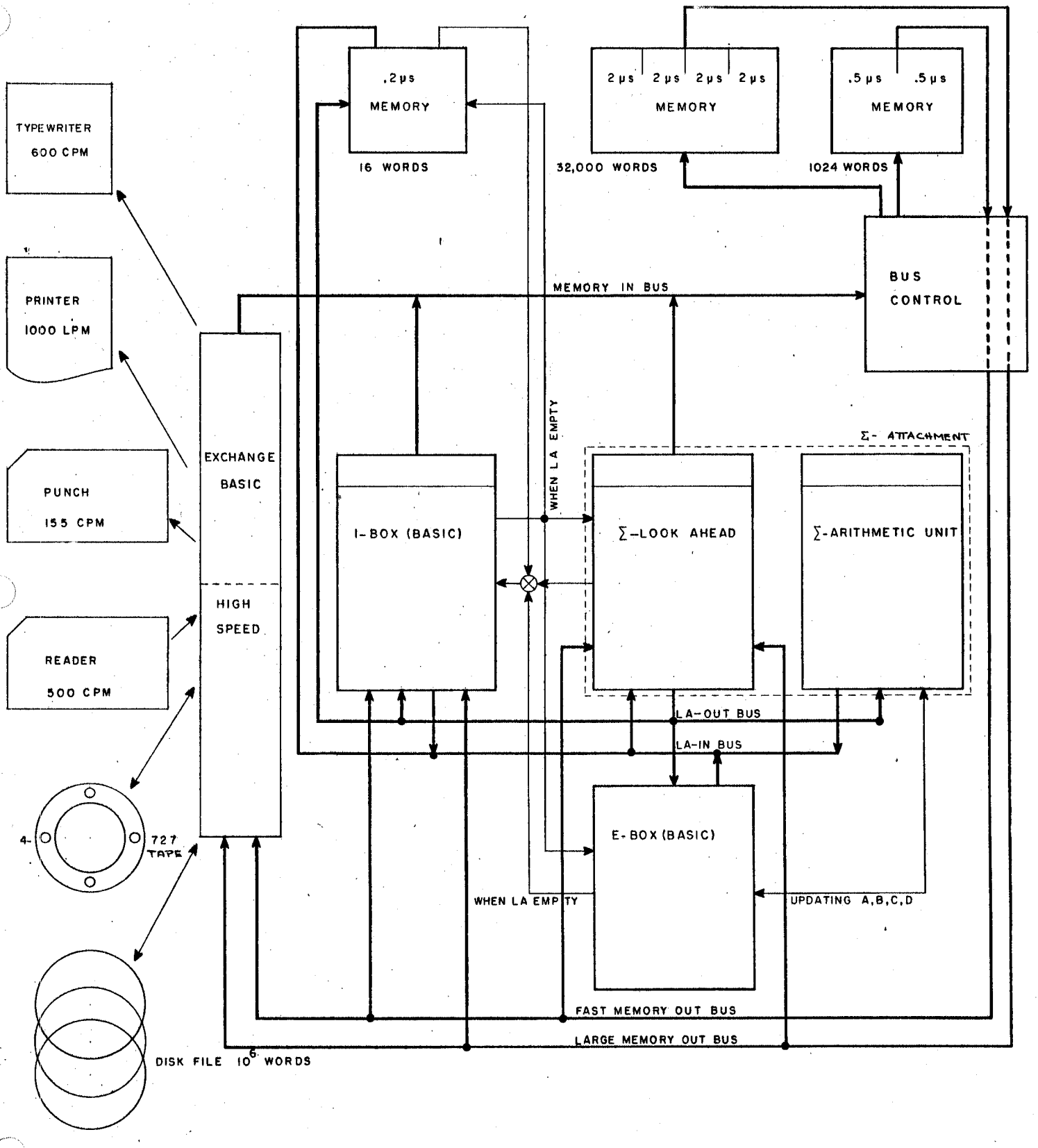
The graphical description of the particular counters' (or commutators') functions contained within the Lookahead are shown in figures 8 through 12. The interlocks with the Basic Instruction Unit's operation for particular I box functions are shown in figures 13 through 19.

SIGMA COMPUTER
MEMO #2

December 31, 1957

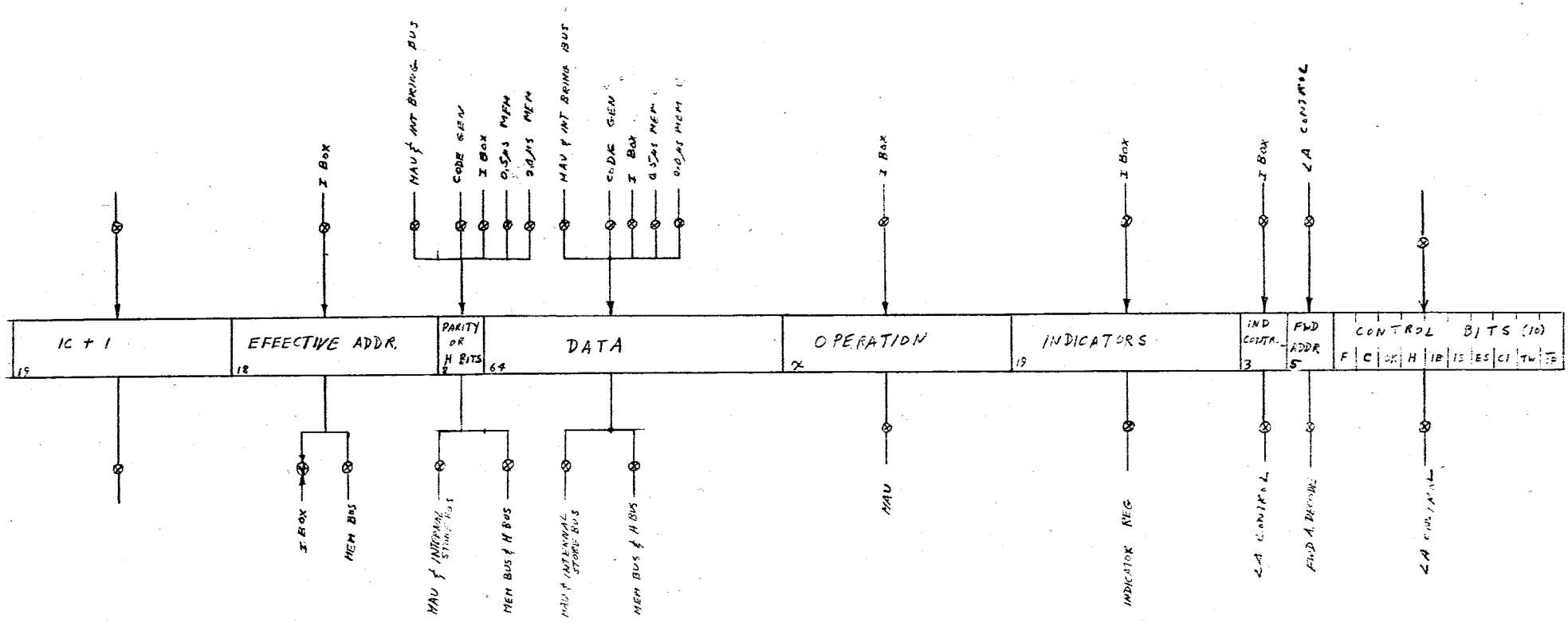
Note: Some desire for an assumed mode of indicator branch handling has been indicated. This mode would mean that the Basic Instruction Box would not wait for the decision of certain indicators such as accumulator positive before executing the conditional branch. The indicators for which this might be desirable are indicator bits 57 through 63. After the branch operation was assumed by the Basic Instruction Unit, it would be verified in the Lookahead System. If the assumption were incorrect, the corrective procedure would be essentially that which occurs after a program interrupt. That is, the lookahead is wiped out, and enough time is allowed so that "bogus" information directed to specific registers can return from memory and be disallowed. Since the corrective procedure is thus time consuming, it is better to wait until the Lookahead System is emptied so that the indicator is in its proper state before attempting to branch rather than assuming the branch unless the probability that a branch will occur is high. To achieve this the Basic Instruction Unit would have to load the conditional branch instruction into the Lookahead System in a modified form. The indicator bit to be tested of the possible seven would be indicated in the data field of the lookahead register. Two control bits, i.e. $\overline{OP}$ and CI, would have to be set.

SIGMA SYSTEM



INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME									X PRINT TO ENG. SPEC. NO.	
DESIGN	E.B	12-2057	MODEL							7000.20.1
DETAIL	RAM	12-27-57								00.00.01.0
CHECK			DRAW							
APPRO			CHECK							

FIG. 1



→ IBOX$_I$ on FWD

MAU$_I$ on EWD

FIG. 2

LOOK AHEAD SYSTEM ADDRESS GATING

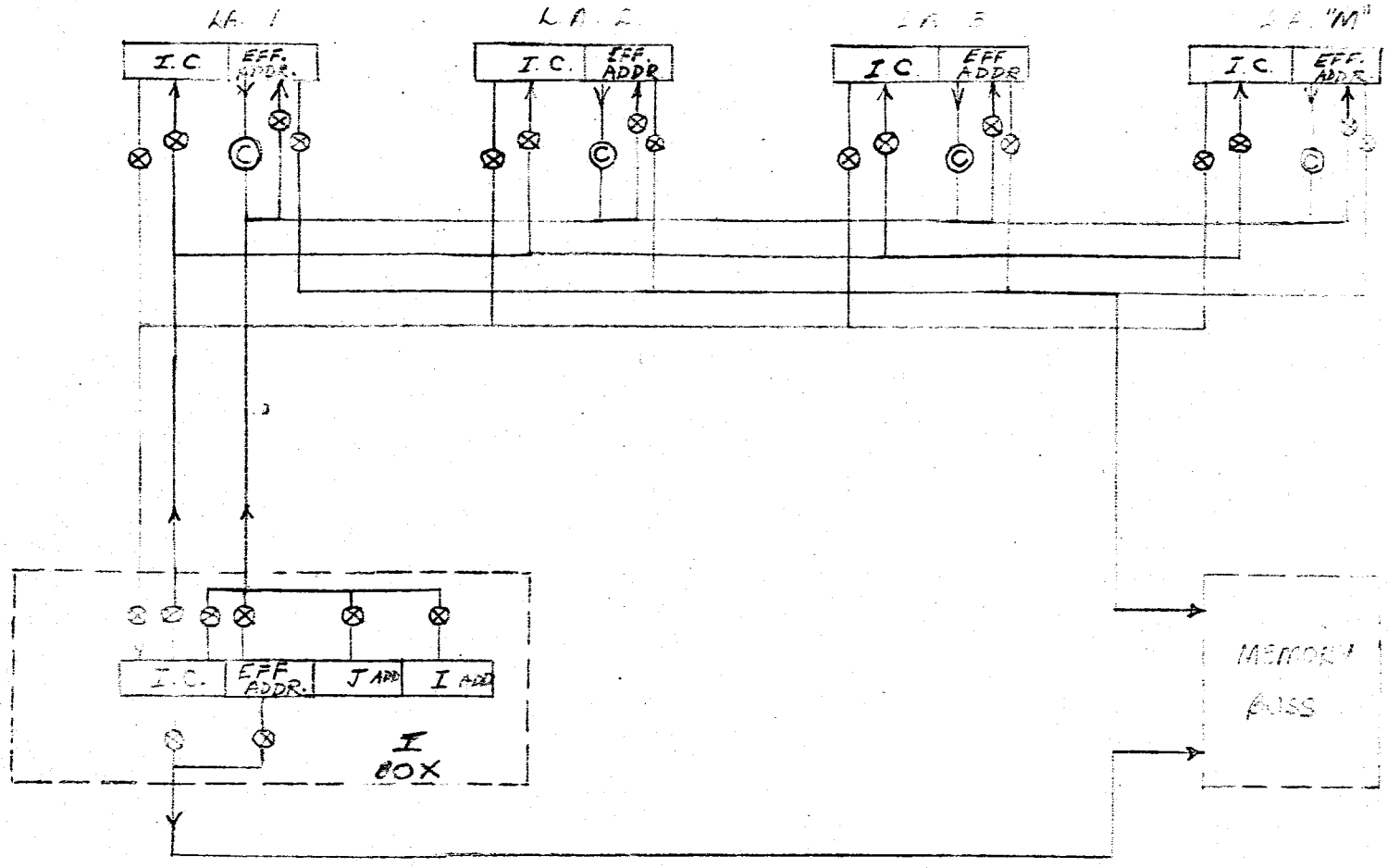


FIG. 3

GATING OF DATA FOR LOOK AHEAD

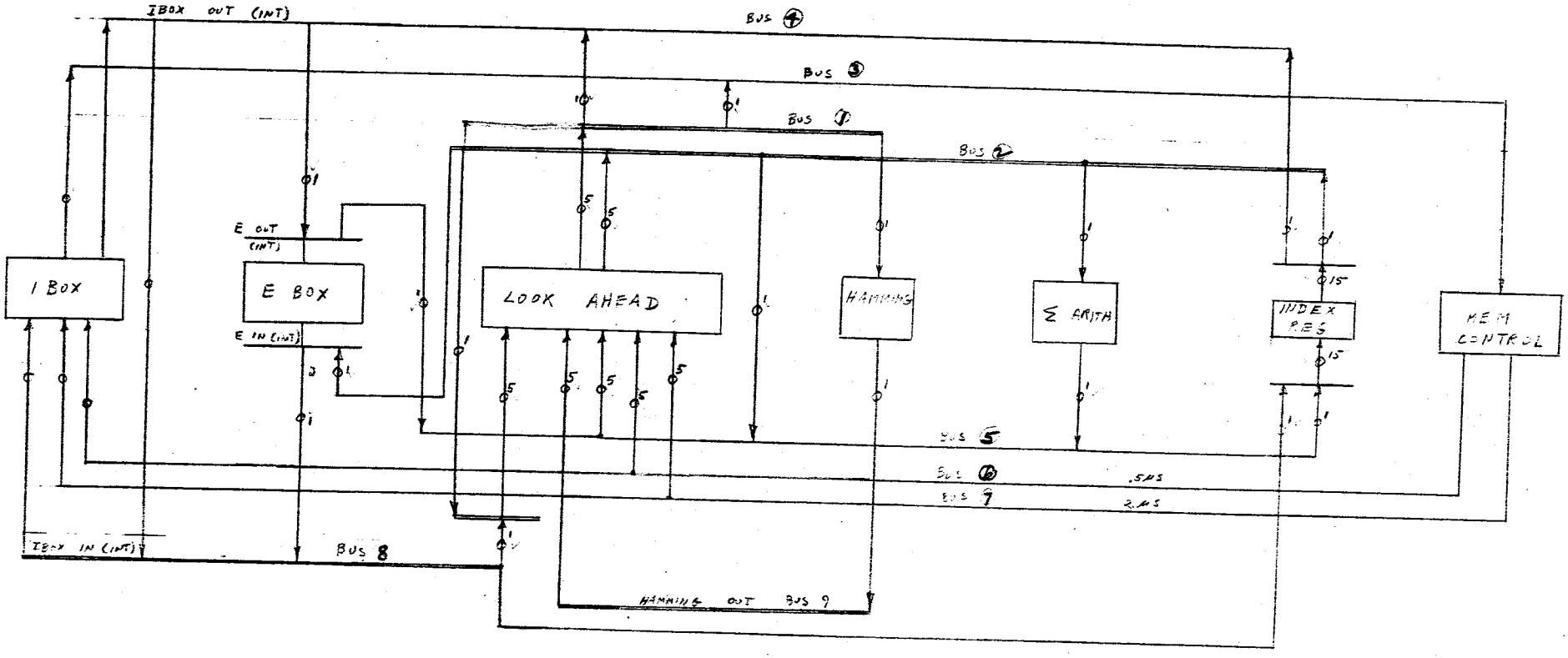


Fig. 4

LOOK AHEAD SYSTEM OPERATION CODE GATING

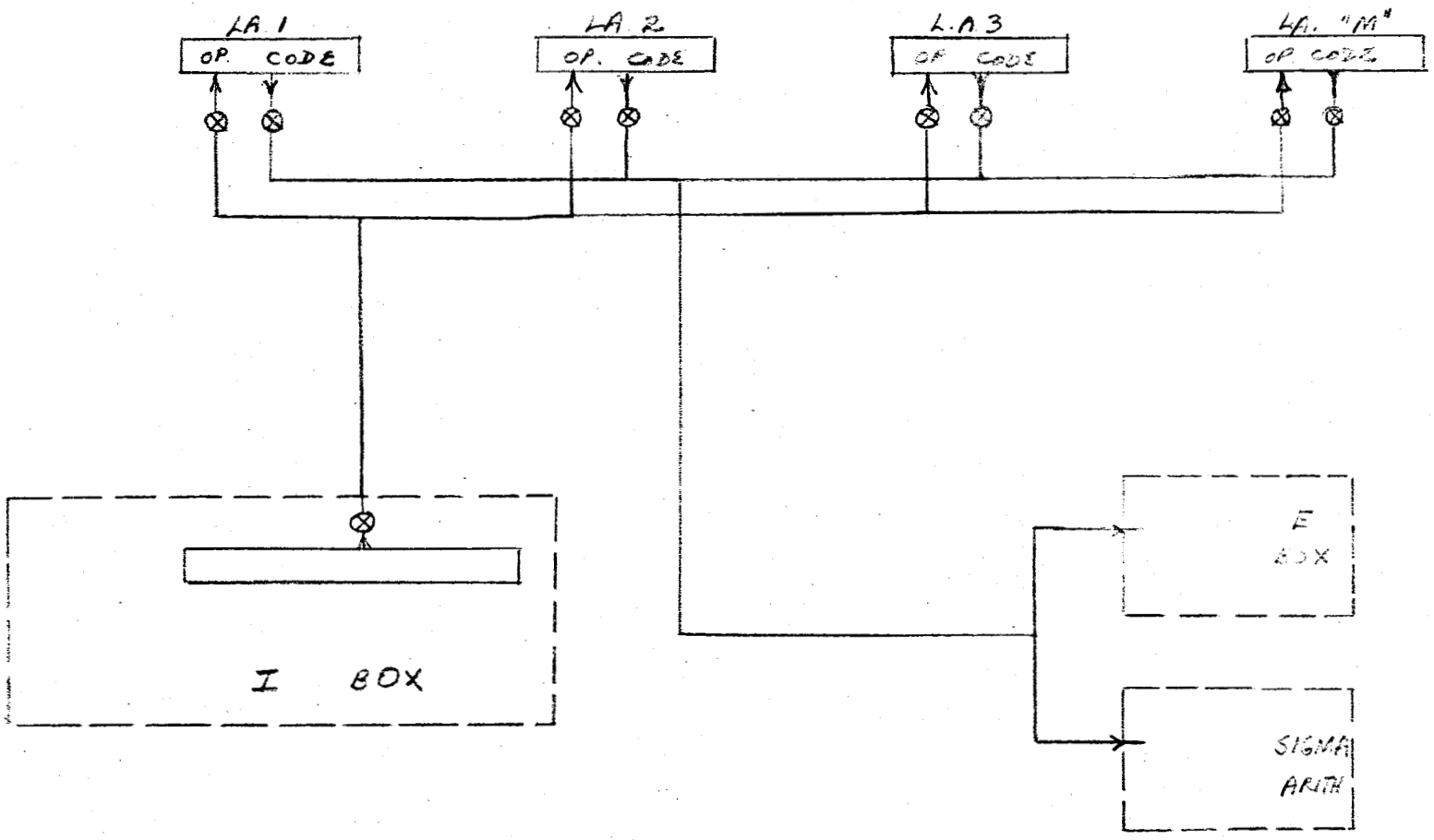


FIG. 5

LOOK AHEAD SYSTEM INDICATOR GATING

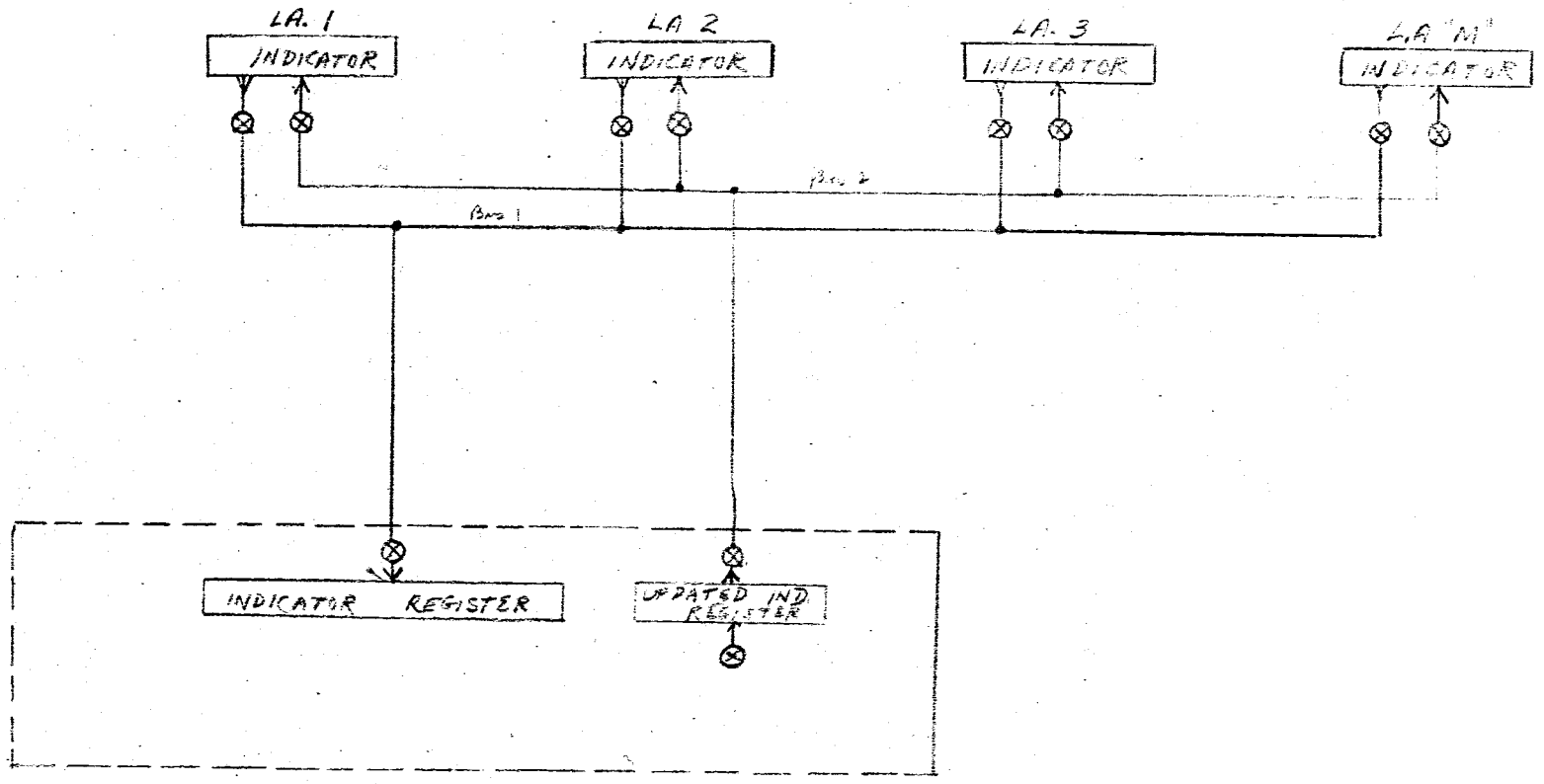


FIG. 6

LOOKAHEAD SYSTEM CONTROL GATING

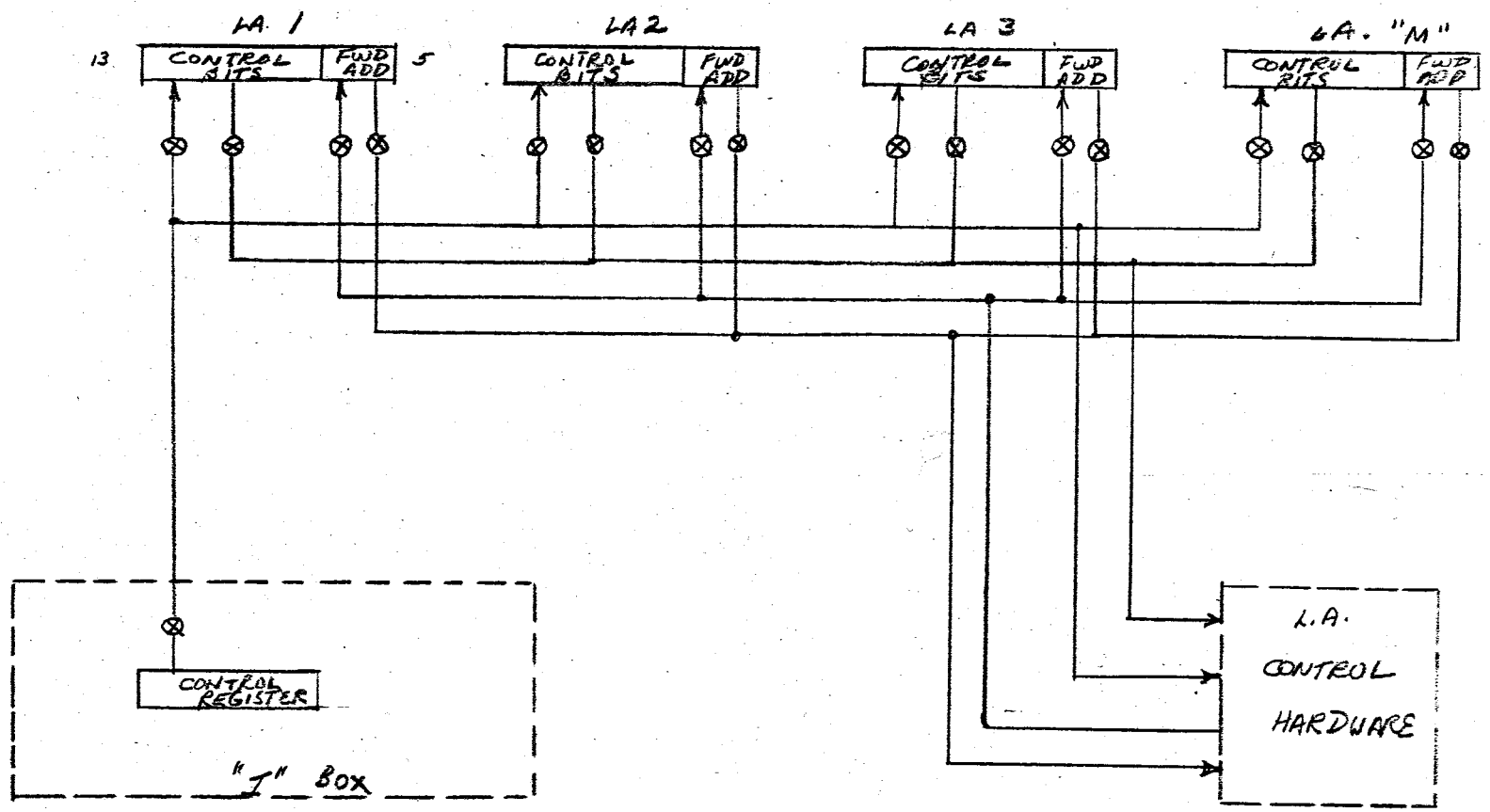


FIG. 7

SIGMA COMPUTER
MEMO #2

December 31, 1957

Index to Notation Used In Flow Diagrams

I	-	Interlock regulating the advance of a particular counter.
IAUC	-	Indexing Arithmetic Unit Counter
MRC	-	Memory Reference Counter
HCC	-	Hamming Check Counter
MAUC	-	Main Arithmetic Unit Counter
$( )_m$	-	m refers to the Lookahead System level currently designated by a counter
$( )_n$	-	n refers to the Lookahead System level compared with
$( )_{l.a.}$	-	l.a. refers to the particular quantity being contained in any Lookahead System register.
$( )_I$	-	I refers to the setting of a control trigger in the Basic Instruction Unit.
F	-	Forwarding bit
ES	-	External Store
BT	-	Break in or program interruption required. This requires "housekeeping" by the Lookahead System before the actual interruption is processed.
$\overline{OP}$	-	No operation bit
H	-	Hamming or parity bit. On designates information in parity form. Off designates the information is in hamming code form or other
PX	-	Progressive indexing trigger located in Basic Instruction unit which notifies Lookahead System that an index valve must be stored in the Lookahead System.
CI	-	Full word instruction signal
TW	-	Two word bit indicating a data word or words necessary for execution of full length instruction.
IB	-	Internal bring bit designates no pre-accessing to memory can be made much ahead of actual usage time.
IS	-	Internal Store bit designates an addressable register referred to for storing.
OK	-	OK bit designates that information is in the data section of the Lookahead System register in a form appropriate to the stage of operation.
C	-	Comparison bit designates that the effective address of a particular level in the Lookahead System should be used in a comparison.
c	-	comparison agrees or $\overline{c}$ does not agree.
S	-	A store is contained (generally anywhere) in the Lookahead System.
FA	-	Forwarding address.

INDEXING ARITHMETIC UNIT COUNTER OPERATION

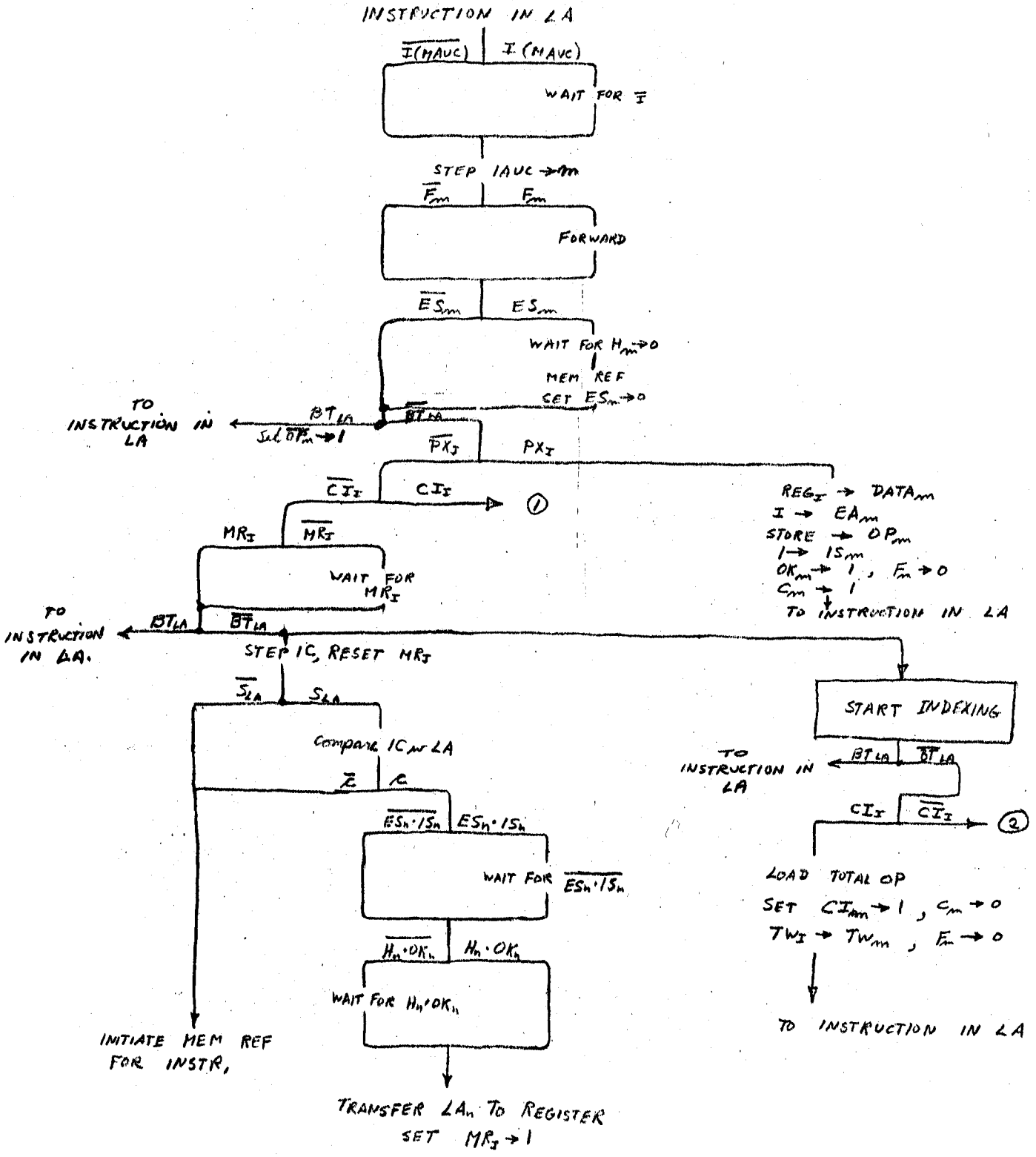
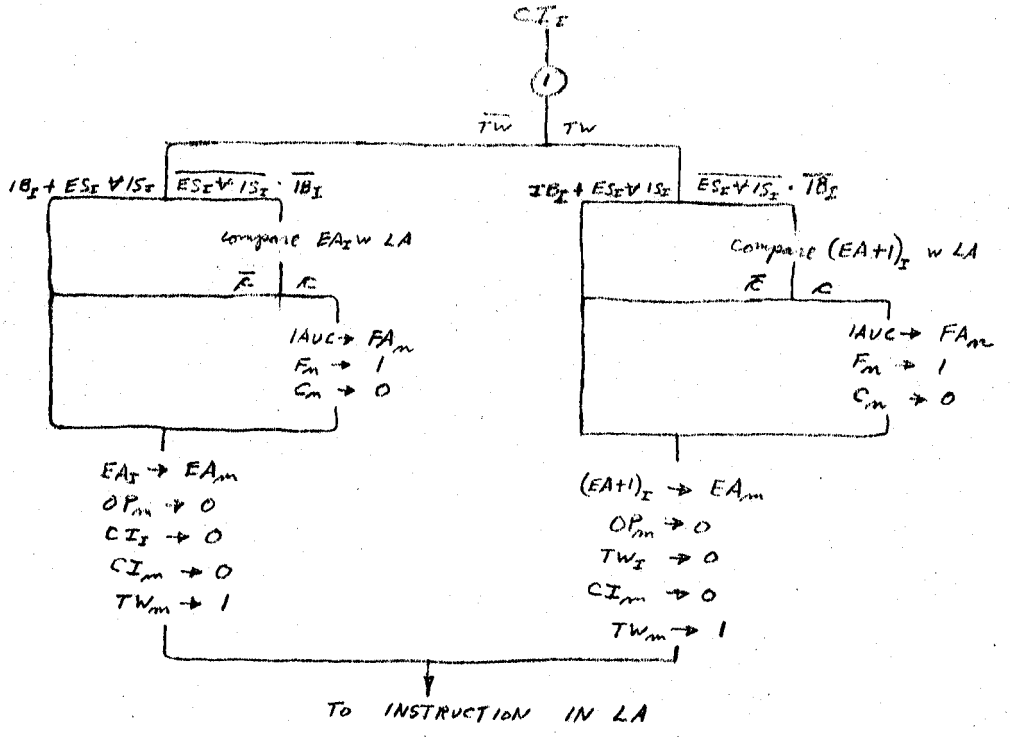


FIG. 5

INDEXING ARITHMETIC UNIT COUNTER OPERATION (CONTINUED)



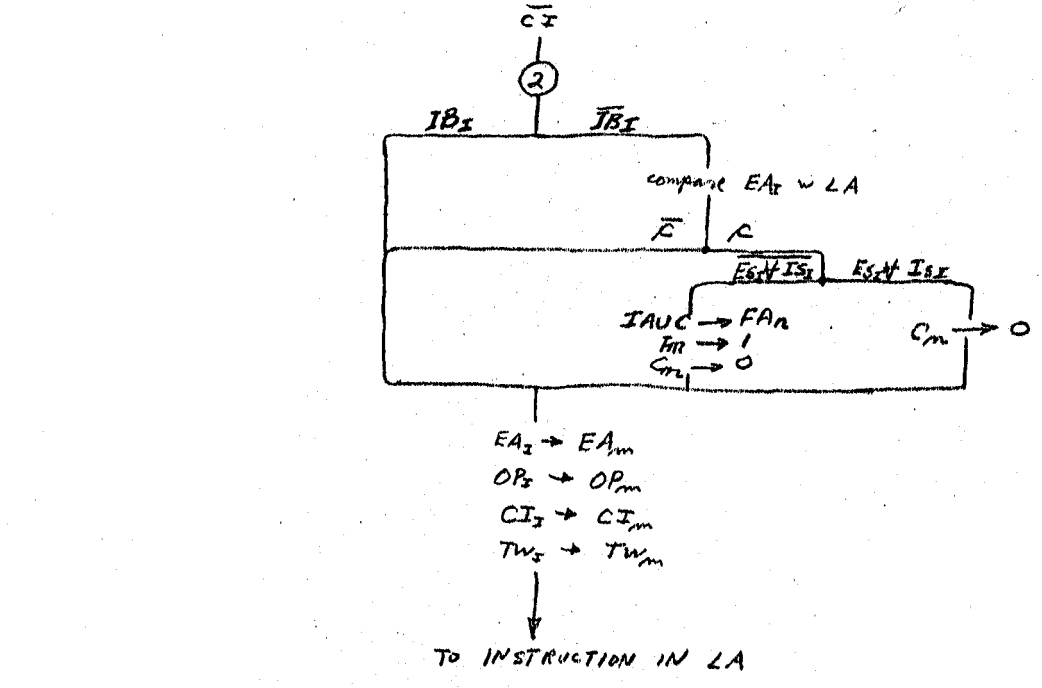


FIG. 9.

MEMORY REFERENCE COUNTER OPERATION

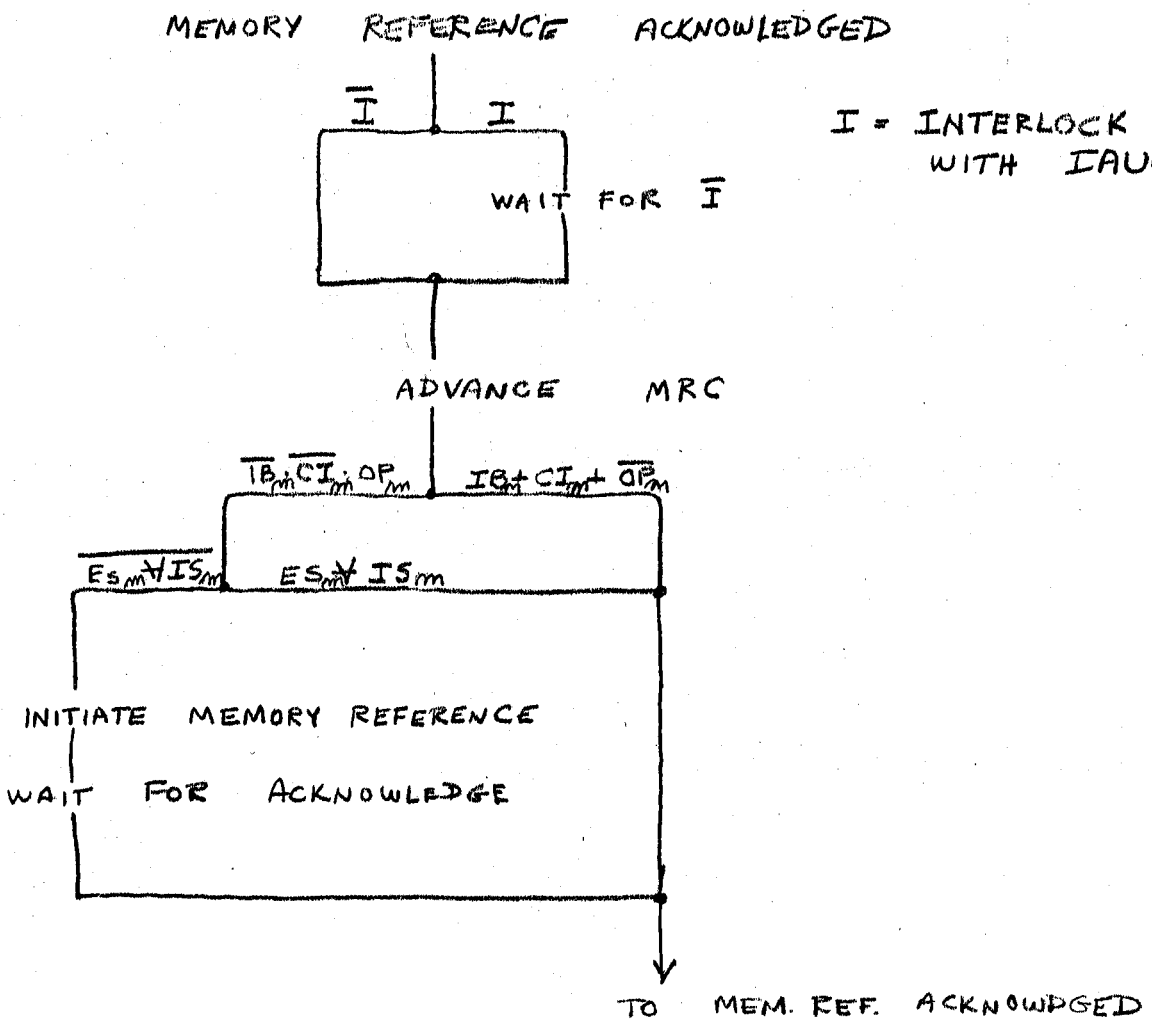


FIG. 10

HAMMING CHECKING COUNTER OPERATION

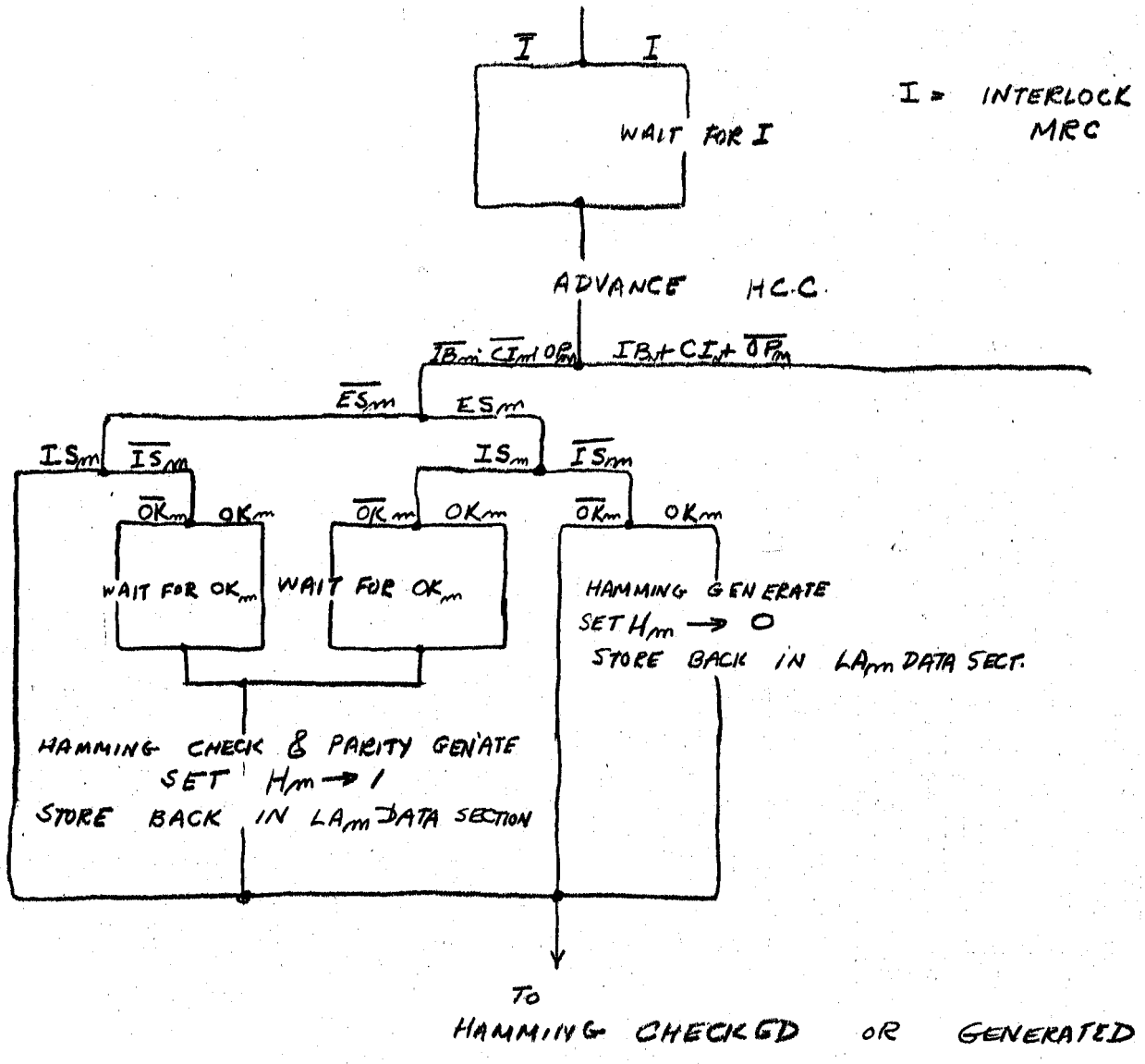


FIG. 11

MAIN ARITHMETIC UNIT COUNTER OPERATION

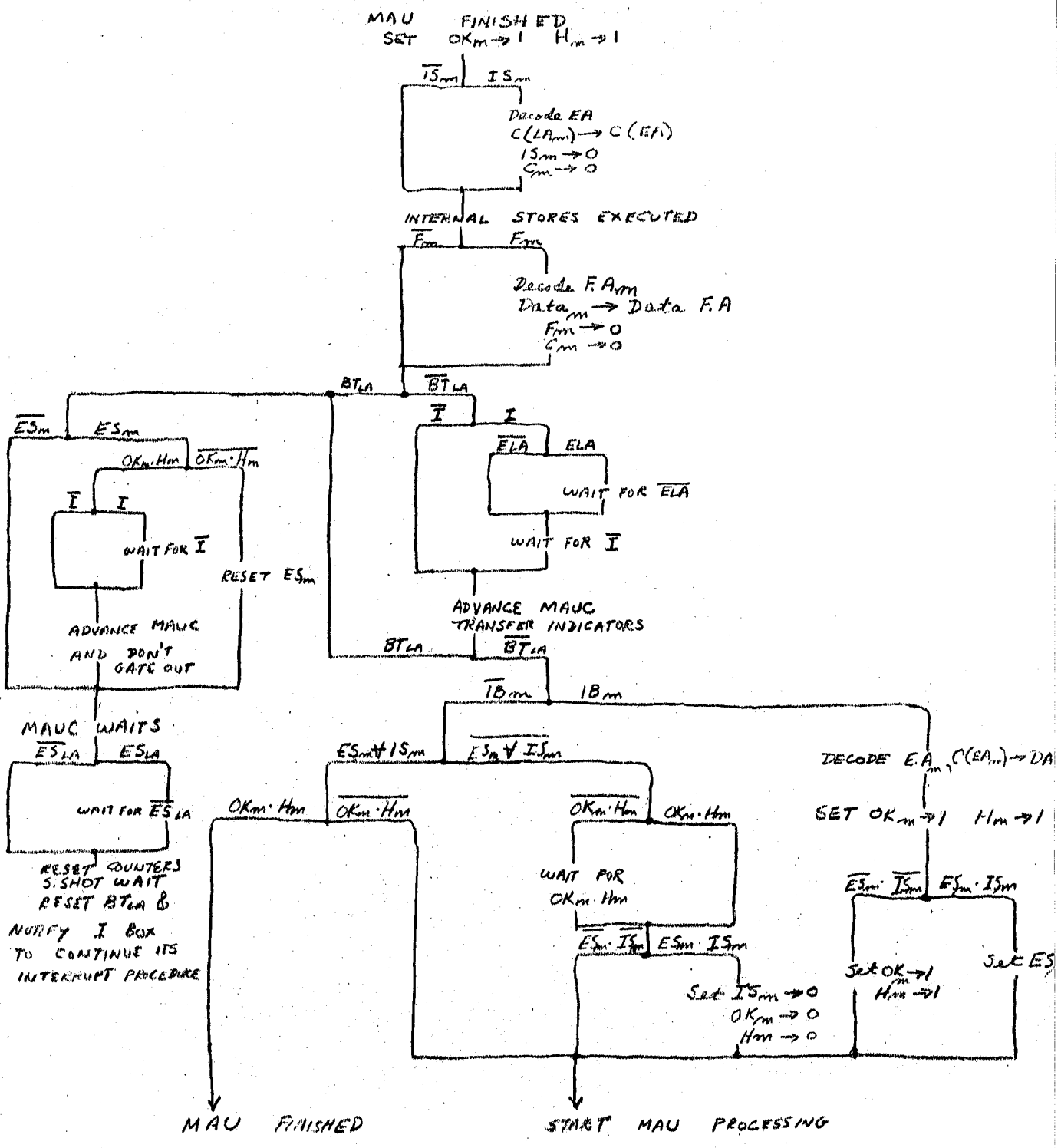


FIG. 12

START INDEXING VARIATIONS

1. ADDRESS MODIFICATION

2 PROGRESSIVE INDEXING

3 LOAD INDIRECT

INDICATOR BRANCH

GEOMETRIC REFILL

CONDITIONAL GEOMETRIC REFILL

4. DIRECT OR IMMEDIATE INDEX ARITH METIC

5. COUNT AND BRANCH

6. GEOMETRIC LOAD.

FIG. 13

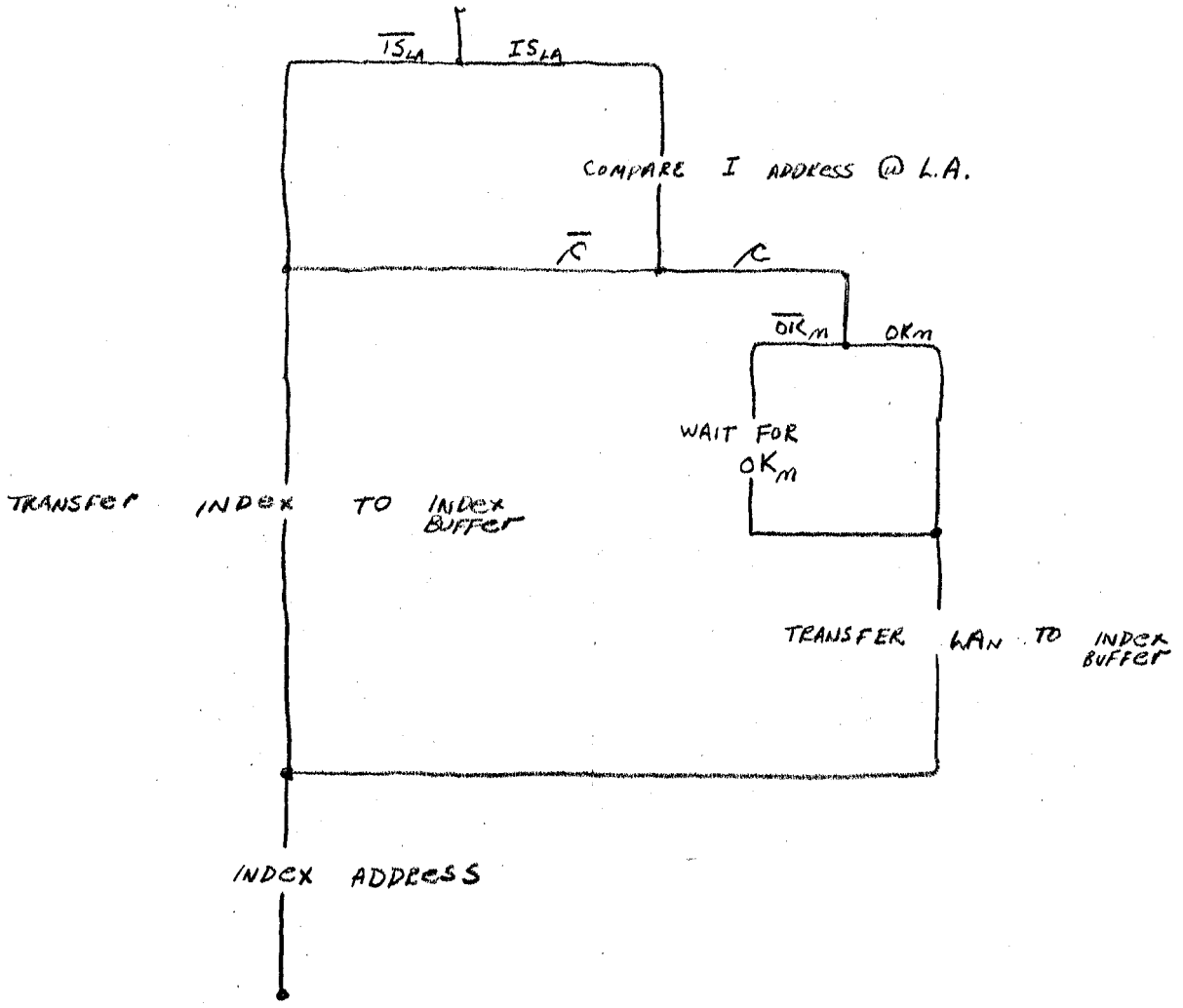

START INDEXING
1. ADDRESS MODIFICATION
$\overline{IS_{LA}}$
IS_{LA}
COMPARE I ADDRESS @ L.A.
$\overline{C}$
C
$\overline{OK_m}$
OK_m
WAIT FOR OK_m
TRANSFER INDEX TO INDEX BUFFER
TRANSFER WAN TO INDEX BUFFER
INDEX ADDRESS

FIG. 14

START INDEXING

2. PROGRESSIVE INDEXING

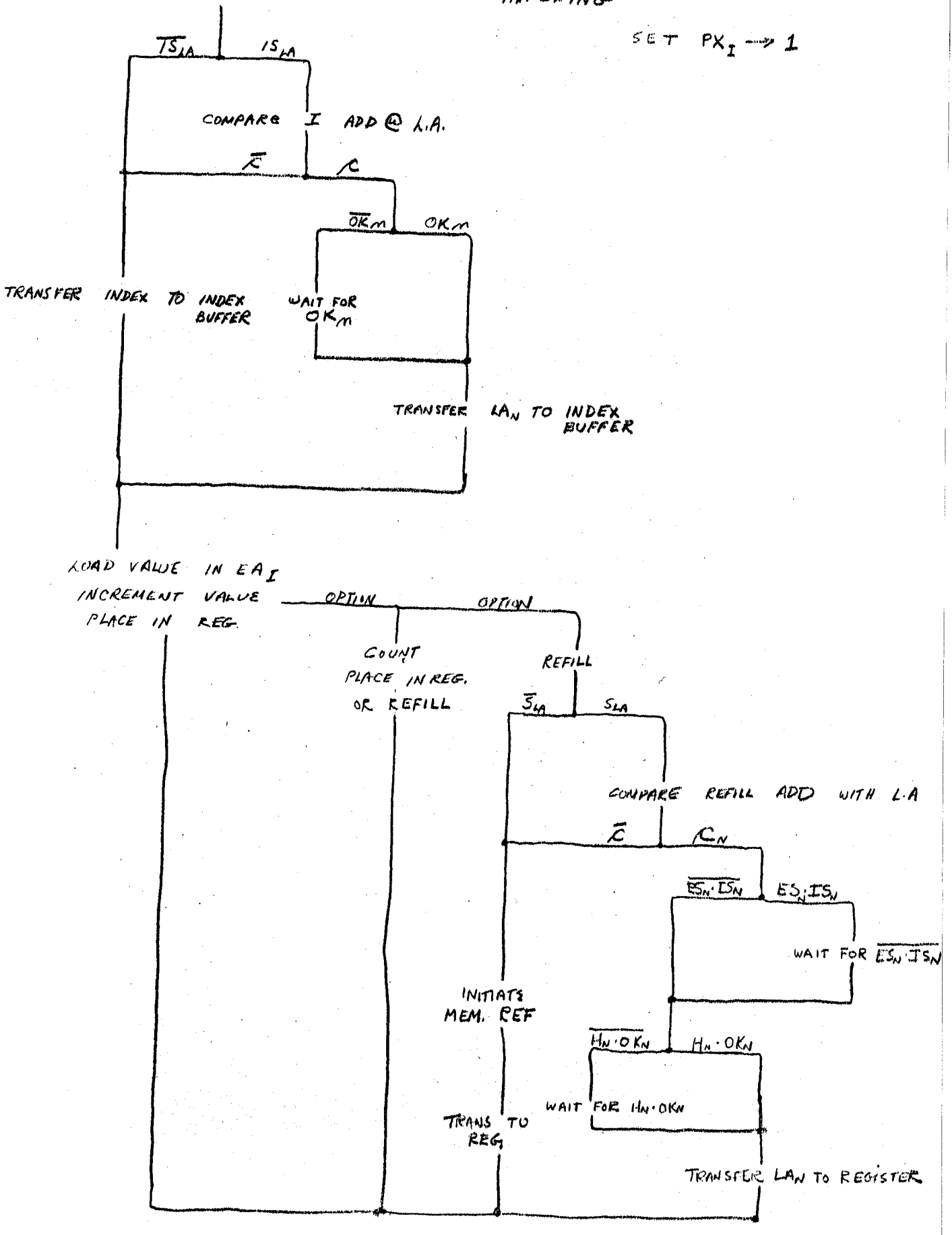


FIG 15

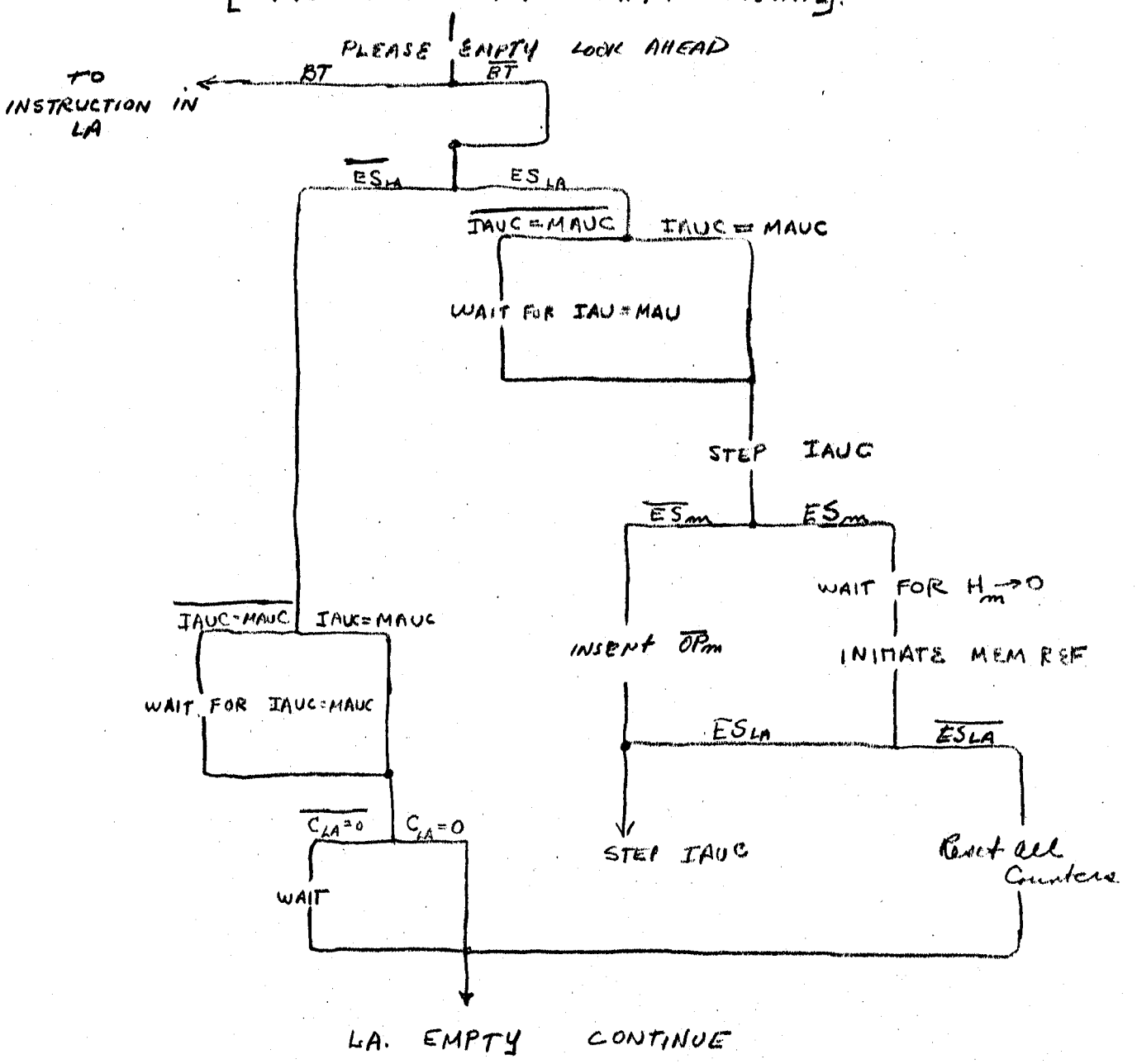
START INDEXING

3. INDIRECT ADDRESSING (OR) LOAD INDIRECT

7. INDICATOR BRANCH *

9 GEOMETRIC RECALL

COND. & GEOMETRIC REFILL

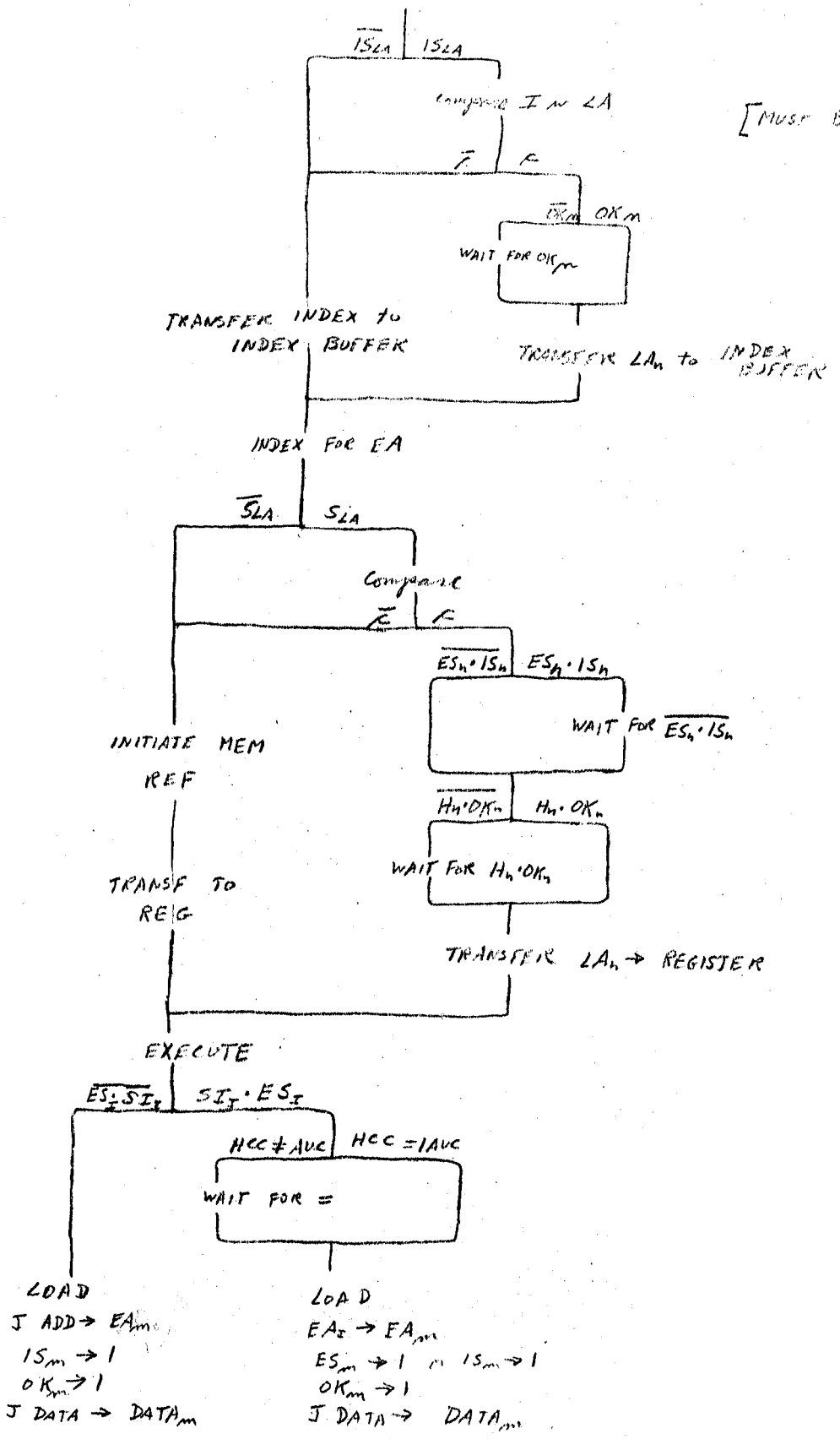


* ONLY WHEN THE INDICATOR REFERRED TO IS IN THE B REGISTER OR NOT SET BY BASIC INSTRUCTION UNIT.

FIG. 16

START INDEXING

4. DIRECT INDEX ARITHMETIC



[MUST BE REPEATED FOR JADDX

FIG. 17

START INDEXING.

5. COUNT AND BRANCH

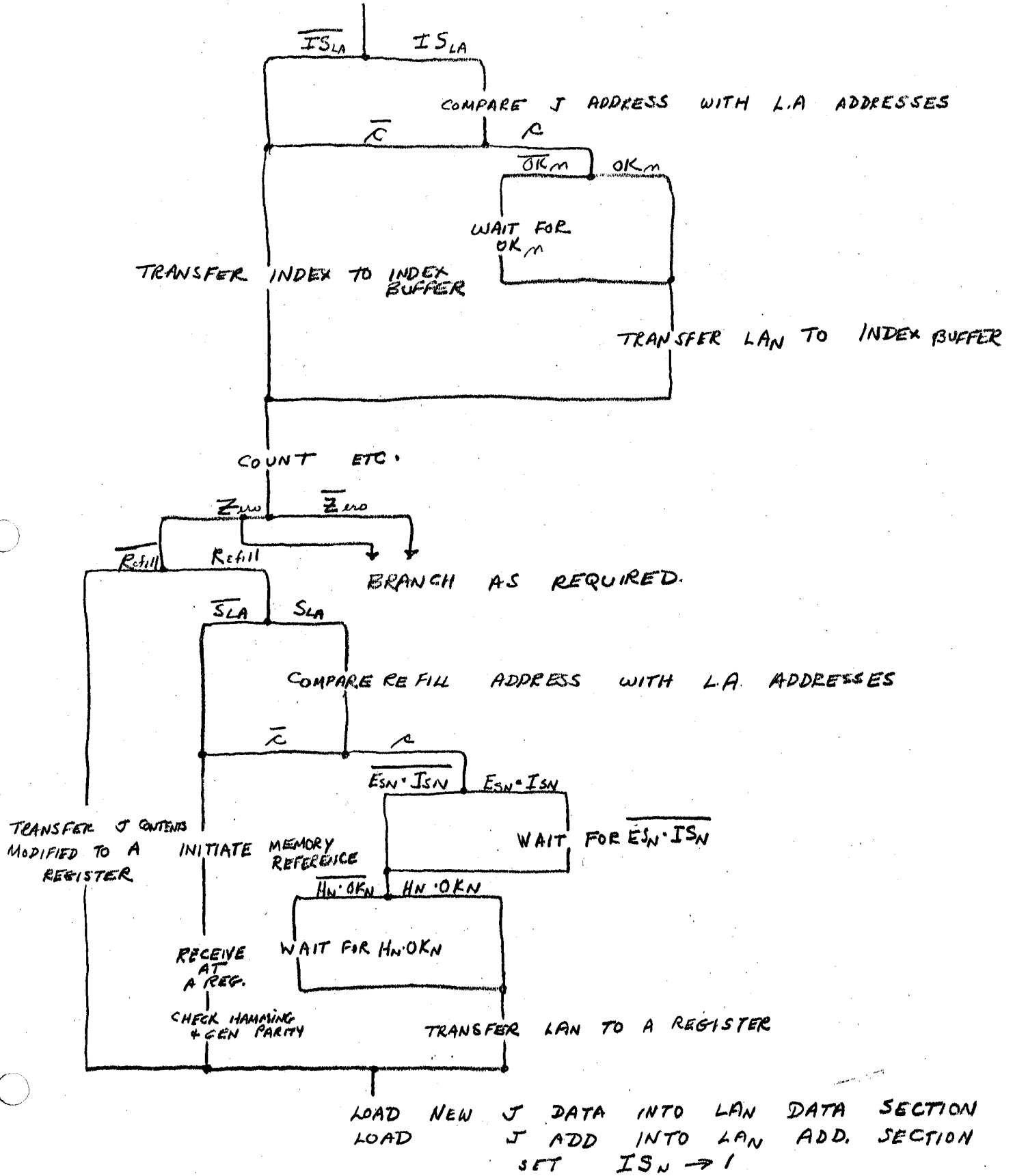


FIG. 18

START INDEXING.

6. GEOMETRIC LOAD

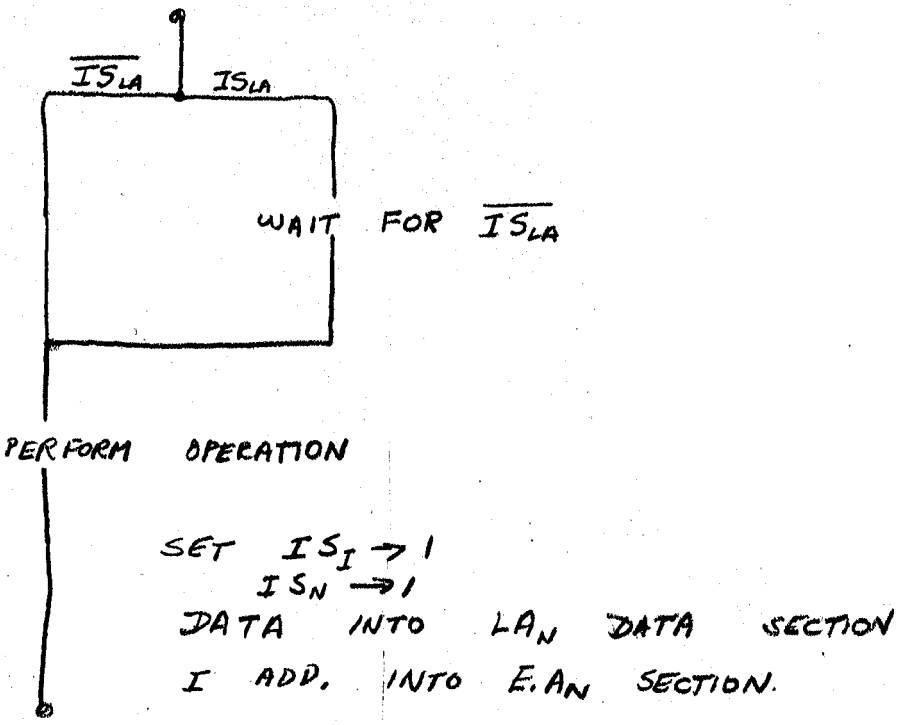


FIG. 19

SIGMA COMPUTER
MEMO #2

December 31, 1957

R J Bahnsen

R. J. Bahnsen

J. F. Dirac

J. F. Dirac

RJB:JFD:bjn