April 7, 1958

FILE MEMO

SUBJECT: First Report on Simulation of the Project 7000 "Base" Computer

by E. W. Coffin

I. Introduction

This memo provides an evaluation of the Project 7000 "Base" computer performance as derived from the use of a simulation program on the 704. As Drs. Kolsky and Cocke have indicated in their Sigma Simulation reports, dated February 6, 1958 and March 12, 1958, evaluation of an asynchronous computer's performance requires more complex techniques than would be required for a synchronous machine.

The "Base" simulation program attempts to process the requirements of instruction processing and data handling on a time scale of 0.1 microsecond allowing the continuous flow of information as expected in the actual computer. The program as written reflects the machine organization philosophy of the period October 1957 through early 1958. In order that timing evaluations might be obtained by processing sample problems, it was necessary to hold alterations in the program design to those reflecting major changes in the machine organization. In some cases this has been made possible by adjusting the timing interlocks to approximate the effects of current thinking.

For the problems processed, it is felt that the overall picture is realistic but it is acknowledged that minor details may not completely reflect current design philosophy.

II Test Problems

The problems selected for testing and evaluation constitute the same basic set as described in the Kolsky-Cocke Memos. The descriptions are repeated here for conciseness.

(a) Mesh Calculation: This is an actual hydrodynamics problem, typifying computing at Los Alamos, supplied by Dr. H. G. Kolsky. It is characterized by:

1. a large number of Floating Point operations.
2. relatively few branches or decisions.
3. data references which are mostly indexed.
4. the use of index registers for temporary storage in half the arithmetic operations.

(b) Monte Carlo Calculation: This problem is a portion of an actual neutron diffusion problem supplied by Dr. S. G. Campbell. It is typical of the class of problems requiring a large number of logical decisions and having the characteristics:

1. relatively little arithmetic.
2. many index and data controlled branches
3. many non-indexed references.

(c) Westinghouse Reactor Problem: This problem is the inner loop of the numerical solution of a neutron diffusion equation proposed by Westinghouse Atomic Power Division. It is typical of the type of calculation performed by Westinghouse and is characterized by:

1. a moderately tight inner loop.
2. a large number of Floating Point operations, all indexed.
3. a relatively low number of branches.

In simulating this problem two different programs were used. Program #I utilizes the Cumulative Multiply order, giving effective double precision results. Program #II uses the sequence Multiply, Add to Memory, giving single precision results.

(d) Composite Test Problem: This problem was constructed by Messrs. Ziller and Heising of Applied Programming as a standard problem for comparing computers. It was constructed to compare effectiveness in:

1. fixing a floating point quantity.
2. evaluate a small polynominal using indexing.

Of all problems run-to-date on the simulator. This one may be said to be the most artificial. The arithmetic ratios were carefully set to meet "standard" conditions.

(e) Solution of Simultaneous Equations: This problem, programmed by Mr. D. W. Sweeney, uses the Jordan process for solving simultaneous equations while obtaining the matrix inverse. This was extrapolated to the solution of 20 simultaneous equations.

(f) Double-Precision Solutions of Simultaneous Equations: This program uses the same method as (e). The set of test equations considered was again a 20 x 21 set.

(g) File Maintenance: The portion of this problem analyzed by the simulator was a loop for developing a printed line as programmed by Miss E. McDonough. The loop substitutes blank BCD characters for leading zeros and arranges the information in a specified format for subsequent printing from tape. This problem is characterized by:

1. a large percentage of full word VFL instructions.
2. a moderate amount of cross-boundary references.
3. the use of index and indicator controlled branches.

III The "Standard Base Computer"

We have defined a "Standard" system to include the following features:

(a) Machine Components

1.	Number of Main Memories	2
2.	Number of Index Registers	15

(b) Computer Speeds

1. Arithmetic Unit Times

	Base*	Sigma*
Floating Load and Store	0.8 usec	0.4 usec
Floating Add	3.0 usec	0.7 usec
Floating Multiply	8.0 usec	1.5 usec
Floating Divide	16.0 usec	2.5 usec
Floating Cumulative Multiply	18.0 usec	2.8 usec

* These Arithmetic unit times are those recommended by Mr. S. W. Dunwell in a memo February 14, 1958.

VFL Load, Add, Count, Store	(1.3 + .26N) usec
VFL Multiply	$(4.5N_R(1.4 + .26N_D))$ usec

where N = Number of bytes in data to be mixed with Accumulator contents

N_R = Number of bytes in multiplier

N_D = Number bytes in multiplicand

The VFL Arithmetic times were estimated by Product Development.

2. Instruction Processing

Index Adder	0.6 usec
ECC Checking	0.6 usec
Parity Checking	0.3 usec

(c) Memory Speeds

1. Index (core) Memory

Read Out Time	0.4 usec
Memory Cycle Time	0.8 usec

2. Fast Memory Times*

Read Out Time	0.4 usec
End Signal Time	0.4 usec
Memory Cycle Time	0.6 usec

* The program's ability to use Fast Memory was required so that overall effects on the system could be fully examined. This ability enabled us to evaluate Sigma conditions with no additional levels of look-ahead. Its use was confined to "Instruction" memory.

3. Main Memory Times

Read Out Time	1.2 usec
End Signal Time	1.8 usec
Memory Cycle Time	2.1 usec

4. Bus Speeds

Buses to and from the memory units were considered to have a 0.2 usec slot (either read or write) available every 0.3 usec. Decode and switching time in the central control unit was assumed to be 0.2 usec.

IV Results

Each of the processed problems, except the File Maintenance problem was run over a range of Arithmetic Speeds varying from Standard (1.0) in increments of 20%. Each of these variations was also run for memory configurations of 0, 1 and 2 Fast Memory units with 1, 2 and 4 Main Memory units.

(a) Appendix I gives a series of graphs in which each problem is considered alone for all variations. The abscissa represents comparison to the Type 704 speed and the ordinate represents the variations from Standard Arithmetic Unit speeds. Each curve is labeled "d_1 - d_2" where d_1 is the number of Fast Memory Units considered and d_2 the number of Main Memory units. Curves are given for 0-1, 0-2, 0-4 and 1-1 memory systems. Curves for other combinations of Fast and Main Memory units were generally identical to the 1-1 combination. Where a variation occurred it was plotted.

(b) Appendix II is a series of graphs showing the speed of all problems operating with a fixed memory configuration. Again the abscissa represents comparison to the Type 704 speed and the ordinate the variation is Arithmetic Unit speeds.

(c) Appendix III graphically shows the effect of memory changes for the Standard Arithmetic Unit speed. The abscissa shows the comparison to Type 704 speeds and the ordinate the variations in memory configuration. The graph is separated into three sections, each section representing a condition of Fast Memory with three conditions of Main Memory.

(d) Appendix IV is a graph showing the effect of memory changes on the problems run using Sigma Standard Arithmetic Unit speeds with 0 levels of look-ahead. These curves may serve as a lower bound on considerations of Sigma simulations as given by Drs Kolsky and Cocke.

(e) Appendix V is a series of graphs which show the percentage changes in the Base System speeds as increments of 20% are applied to the maximum flow of input-output. Graphs are given for variations in the maximum rate of the Base Exchange and the High Speed Exchange separately, followed by variations

with both Exchanges operating. Each graph shows percentage change in the Mesh Calculation speeds where the Arithmetic Speeds are taken as standard. Main Memory is allowed to vary over 1, 2, and 4 units for each condition examined. It should be noted that an attempt at randomness is addressing memory units was achieved by starting the addresses referred to by the Exchanges at an odd value for the Base Exchange and an even value for the High Speed Exchange at the beginning of the first simulation run. Succeeding runs continued the sequence unless it was required to read in the program because of an interruption. Therefore, the configuration of addresses for a particular problem is unknown.

(f) Appendix VI is a set of graphs showing the performance of the Base system against the LARC for the solution of simultaneous equations. The abscissa represents comparison to the LARC speed and the ordinate gives the variation in Arithmetic Unit speeds. In the comparisons the LARC was assumed to use single-precision hardware in the single precision study and double precision hardware in the double precision study. The Base system double-precision program utilizes the programmable double-precision features of its hardware.

(g) The results for the File Maintenance are best discussed in tabular form and appear as item 6 in the Summary.

V. Summary

Several points of special interest are observable from the graphs given in the Appendices. They are itemized below.

(a) The Base System with one Main Memory unit stands distinct as a lower bound. The two and four Main Memory unit systems tend to produce a relatively compact grouping. At standard AU speeds we note the following relationships.

Problem/ Memory	Memory 0-1	Memory 0-2	% increase 0-2 over 0-1	Memory 0-4	% increase 0-4 over 0-1	% increase 0.4 over 0-2
Mesh	14.7	16.2	10.2	16.6	12.9	2.5
Monte Carlo	13.4	14.1	5.3	14.1	5.3	0.0
Westinghouse I	15.4	16.4	6.5	16.4	6.5	0.0
Westinghouse II	18.6	19.2	3.3	19.5	4.9	1.5
Test	16.9	18.7	10.8	18.7	10.8	0.0
Sim. Equ.	14.4	15.3	6.2	15.9	10.5	3.9
			Ave. 7.1		Ave. 8.5	Ave 1.3

This table indicates that at Standard Arithmetic Unit speeds we get an average of 7.1% increase in performance when going from a 1 to 2 Main Memory system while we get only an average of 8.5% increase in performance when going from a 1 to 4 Main Memory system. However, in going from a 2 to 4 Main Memory system we note only an average of 1.3% increase in performance.

(b) In general it was found that 1 Fast Memory, used for instructions only, coupled with 1 Main Memory produced the upper limit on operating times for all Arithmetic Unit speeds and all problems. Other combinations of Fast and Main Memory units gave results which were identical to the "1-1" curve drawn.

Two problems showed changes from this pattern and the appropriate curves are shown. These problems were the Mesh problem and the Test problem.

For the Mesh problem we have 1 Fast Memory and 1, 2 or 4 Main Memories producing results for the curve labeled "1-1". With 2 Fast Memories and 1, 2 or 4 Main Memories we have the curve labeled "2-1".

For the Test Problem 1 or 2 Fast Memories coupled with 1 Main Memory produced results for the curve labeled "1-1". With 1 or 2 Fast Memories and 2 or 4 Main Memories we have the curve labeled "1-2".

This would indicate that the use of Fast Memory without any look-ahead facilities rapidly leads to a computer and/or instruction process limit state i.e., that the Central Processing Unit dominates the computer.

The increase in performance of a 1 Fast Memory unit system coupled with Main Memory is shown below. Fast Memory was used for instructions only in these runs.

Problem	Memory 0-1	Memory 0-2	Memory 1-1	% increase over 0-1	% increase over 0-2
Mesh	14.7	16.2	18.3	24.7	13.1
Monte Carlo	13.4	14.1	15.9	18.7	13.1
Westinghouse I	15.4	16.4	16.8	9.1	2.5
Westinghouse II	18.6	19.2	19.6	5.3	2.3
Test	16.9	18.7	19.0	12.4	1.7
Sim. Equ.	14.4	15.3	16.4	13.9	6.2
			ave.	14.0%	ave 5.4%

(c) These graphs further indicate a fairly general increase in performance with decreasing arithmetic speeds. If we consider a 2 Main Memory unit system as standard then the following table results.

Problem	AU Speed Std.	AU Speed .8 Std.	% increase over Std.	AU Speed .6 Std.	% increase over Std.
Mesh	16.2	18.2	12.2	20.6	27.1
Monte Carlo	14.1	15.0	7.1	15.7	11.3
Westinghouse I	16.4	19.1	16.3	22.8	39.0
Westinghouse II	19.2	21.9	14.1	25.4	32.3
Test	18.7	21.2	13.4	24.1	29.0
Sim. Equ.	15.3	17.0	11.1	18.9	23.3
			ave. 12.4%		ave. 27.0%

The values under AU Speed are relative performance against the 704.

d. With the information noted in the last two tables an examination of the results obtained by using reduced Arithmetic Unit speeds in calculation and one unit of Fast Memory for instructions may be of interest. Such a table is given below. Here we consider the increases from 0-1 and 0-2 memory configurations operating at standard Arithmetic Unit speeds to a 1-1 memory configuration operating at .8 of Arithmetic Unit standard and .6 of Arithmetic Unit standard.

Problem	AU Std. 0-1	AU Std. 0-2	.8 AU Std. 1-1	% increase over 0-1	% increase over 0-2
Mesh	14.7	16.2	20.9	42.3	29.0
Monte Carlo	13.4	14.1	17.2	28.5	22.0
Westinghouse I	15.4	16.4	19.8	28.5	20.7
Westinghouse II	18.6	19.2	22.7	22.1	18.2
Test	16.9	18.7	21.6	27.7	15.5
Sim. Equ.	14.4	15.3	18.3	27.0	19.5
			ave.	29.4% ave	20.8%

Problem	AU Std. 0-1	AU Std. 0-2	.6 AU Speed 1-1	% increase over 0-1	% increase over 0-2
Mesh	14.7	16.2	24.1	64.0	48.5
Monte Carlo	13.4	14.1	18.6	38.7	32.0
Westinghouse I	15.4	16.4	24.0	56.0	46.3
Westinghouse II	18.6	19.2	26.9	44.5	40.0
Test	16.9	18.7	24.8	46.7	32.5
Sim. Equ.	14.4	15.3	20.8	44.5	36.0
			ave.	49.2 ave	39.2

All figures under Arithmetic Standard average performance relative to the 704.

We see from this that the Base System is definitely improved by the use of Fast Memory. If further adjustments could reduce the Floating Point Arithmetic Speeds the Base System could increase its performance range from (14 to 19.5) times 704 upward to (18.5 to 27) times 704.

(e) In the comparison of the LARC and Base systems it is interesting to note the following table. The times given for Base are those developed from a 0.2 memory configuration operating at standard Arithmetic Unit speeds. The system of equations solved was a 20 x 21 system.

	Base	LARC
Single	223.110 ms	300.48 ms
Double	667.332 ms	710.40 ms

From the curves we note that only for the 1 Main Memory case does the Base system fall slightly below LARC in performance of double-precision.

The comparison of LARC with Base operating at Sigma Standard Arithmetic Unit speeds but no Fast Memory or "look-ahead" may be of interest.

	1 Memory	2 Memory	4 Memory
Single	1.86	2.08	2.23
Double	2.01	2.36	2.43

(f) File Maintenance - Two sections of this problem were actually processed through the simulator. One section dealing with the editing of a print line to develop a specified format stands out as a general problem of particular interest.

The table given here shows a direct comparison of the 705-3, 709 and Base systems under two conditions. First-relative measures of the compute time for the three systems is shown without consideration of input-output. Next-relative measures of the three systems is given in which the Base system has 4 - 729-3 tapes operating concurrently, the 709 has 2 - 729-1 tapes operating concurrently and the 705-3 has 1 - 729-1 and 1 - 729-3 tapes operating concurrently. Here we are showing the change in the relative speeds due to I/O use of bus and memory units during the computer processing time for the print editing process.

Base System Main Memory Units	Without I/O		With I/O	
	705-3	709	705-3	709
1	9.4	8.7	10.3	8.8
2	10.4	9.7	11.8	10.0
4	11.1	10.3	12.6	10.7

The total computing time for this problem on the Base system was extrapolated from the portions run. The results given below indicate the relative processing capabilities of the three systems. It should be borne in mind, however, that actually all three systems are tape limited. A complete analysis of the conditions of this problem has been given in Technical Report #9 and an Application Study dated 3/18/58 in the Project 7000 file. Both reports were prepared by Miss E. McDonough.

Base System Main Memory Units	Without I/O		With I/O	
	705-3	709	705-3	709
1	14.2	13.2	16.1	13.7
2	16.1	14.9	18.4	15.7
4	17.2	16.0	19.9	17.0

The total processing time for the three systems showing the full effect of the tape limited condition is:

System	Total time us.	Relative
705-3	1950	5.7
709	3175	9.3
Base	340	1.0

The table below is given to provide an indication of the effects of a practical Input-Output operation on the operating speed of the Base central processing unit.

Main Memory Units	% Increase in Running Time for Print Edit
1	+3.8%
2	+1.2%
4	+0.8%

VI Conclusion

(a) Evaluation of the information produced by these Base system simulation runs indicates a system whose usage of various component elements is relatively well balanced. The "Standard" system indicates that the machine organization simulated will operate from 14 to 19.5 times faster than the 704 for the technical problems considered. For a class of problems giving heavy use to the VFL instructions we find a relative increase of 13 to 16 times the 709.

(b) The limited programming experience obtained through the writing of programs for simulation runs indicates that the instruction set has sufficient power and flexibility to make the choice of a particular instruction an important element of programming. Detailed knowledge of the internal processing operations will be more useful to the programmer who attempts to exploit the system to the fullest, than with any system previously developed.

(c) As indicated in the summary, the system contains sufficient latent power in its organization to make possible an upgrading of performance should consideration of other systems in the product line or competitive systems make this requirement feasible.

(d) One note of caution - The print line editing portion of the File Maintenance problem indicates that large volume data translation and/or preparation may prove a serious drag on the system. Here performance drops to approximately 9-10 times 709. This may be quite important in considering problems to be processed by the Sigma or Harvest Systems. Further studies will be conducted on related problems of "on-line" card reading, card punching and printing.

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EWC/jcv

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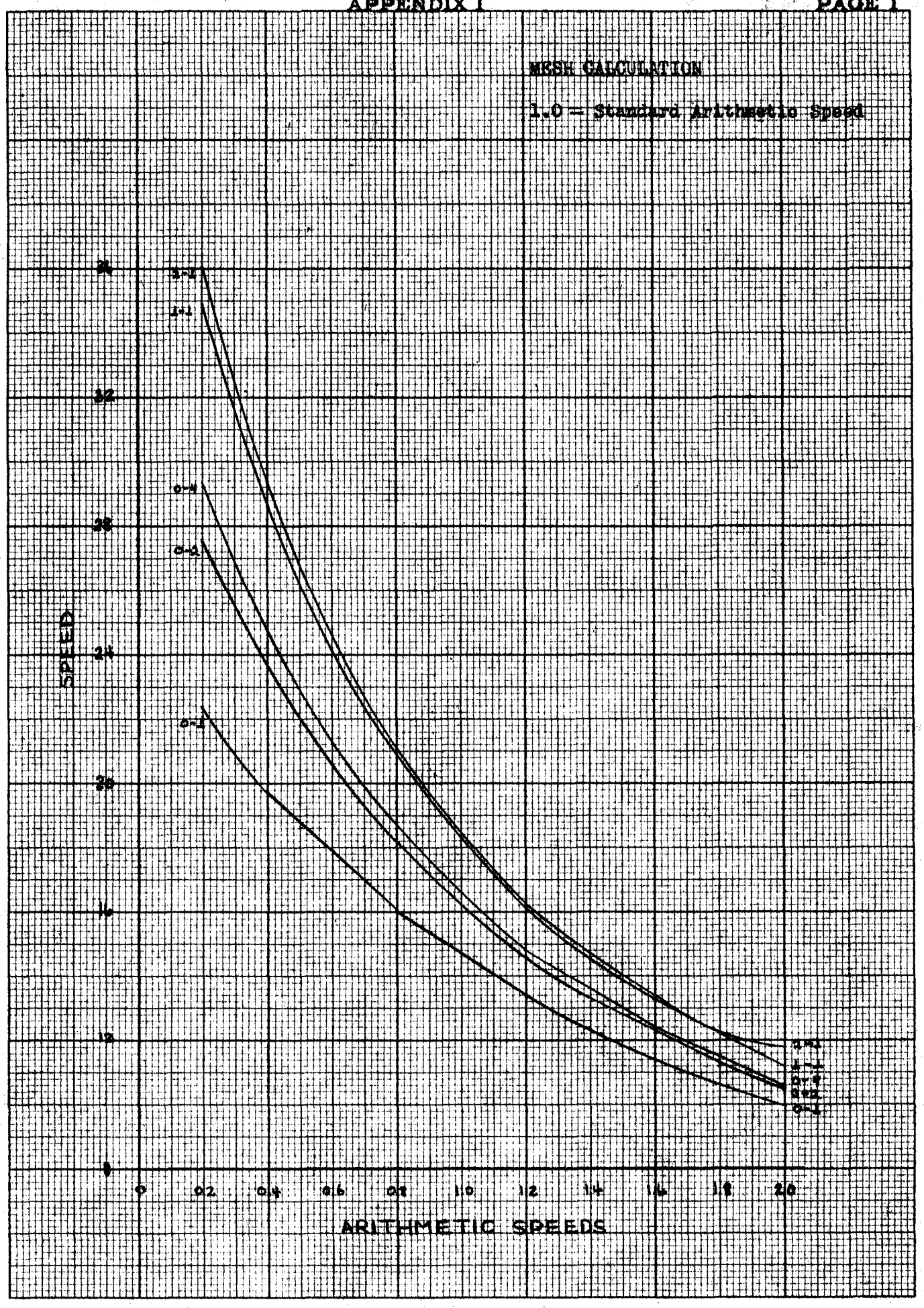
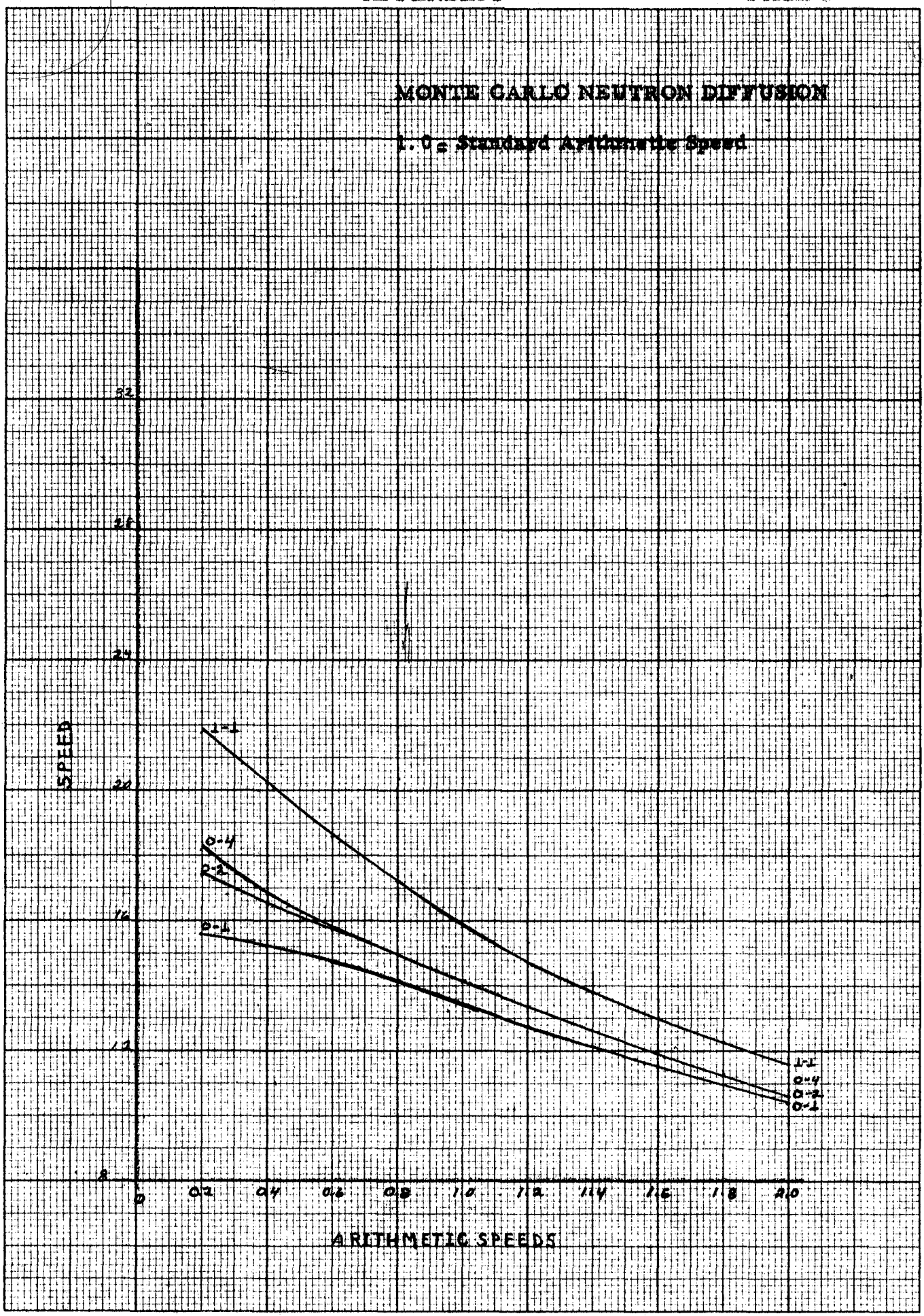
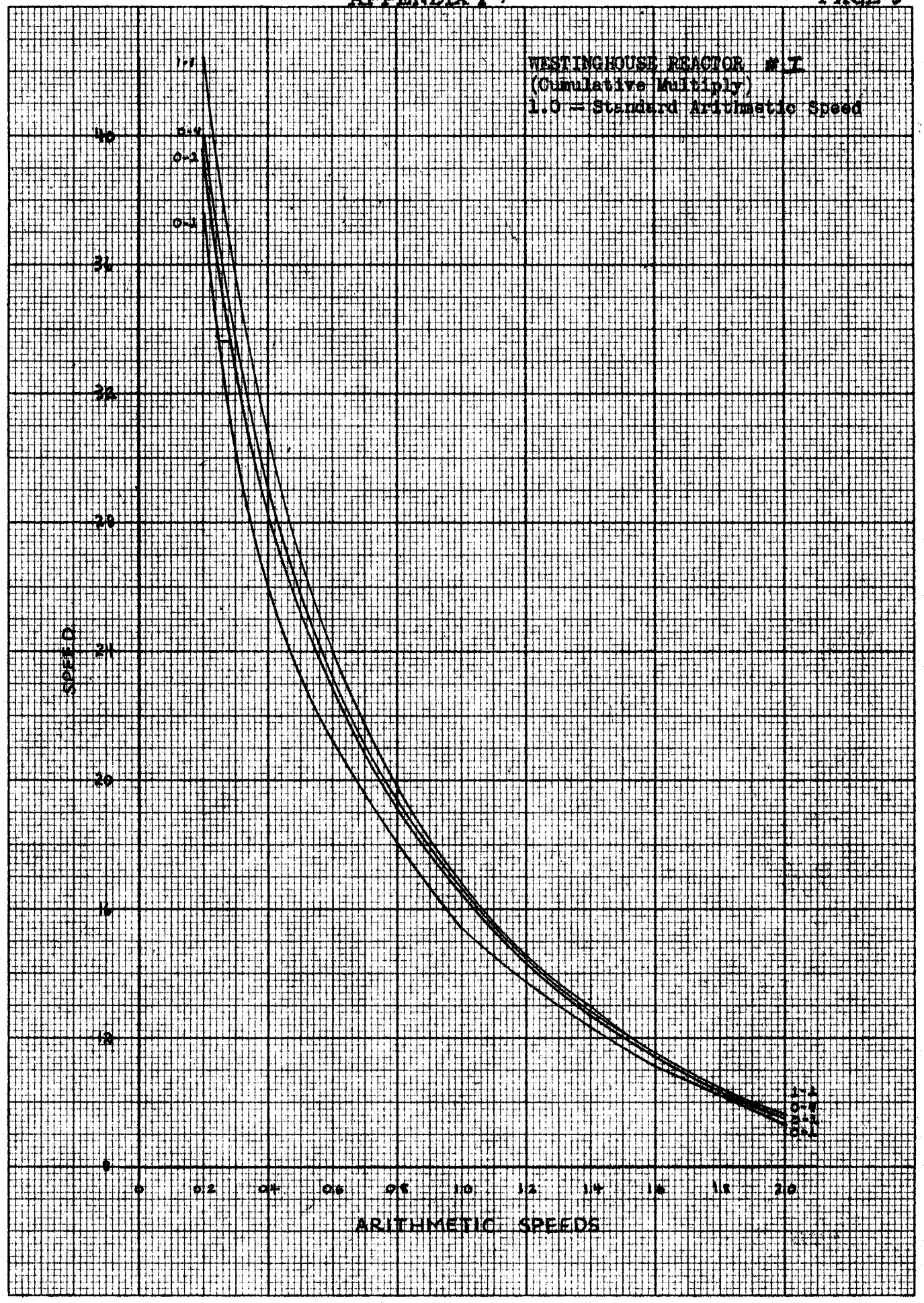
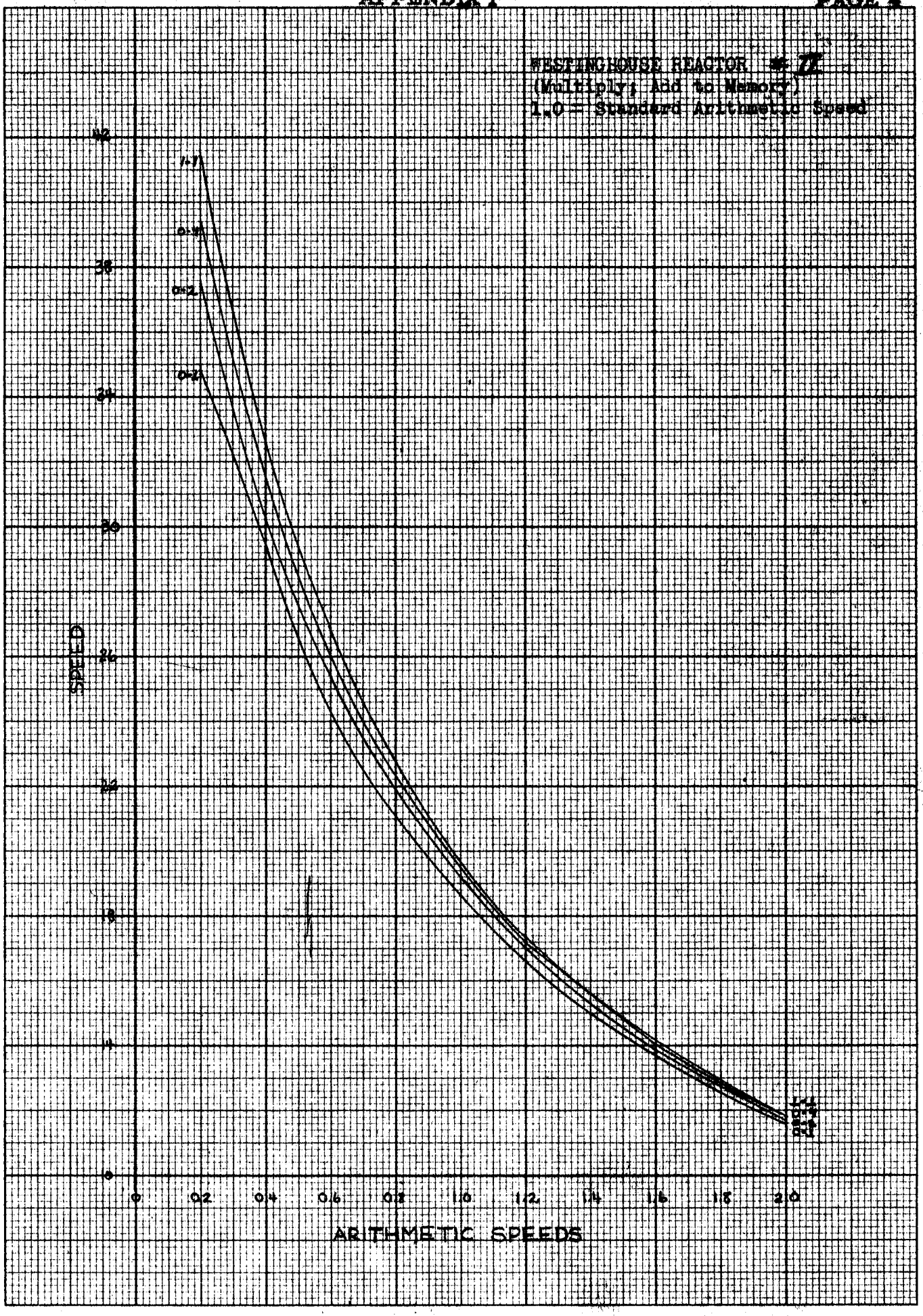
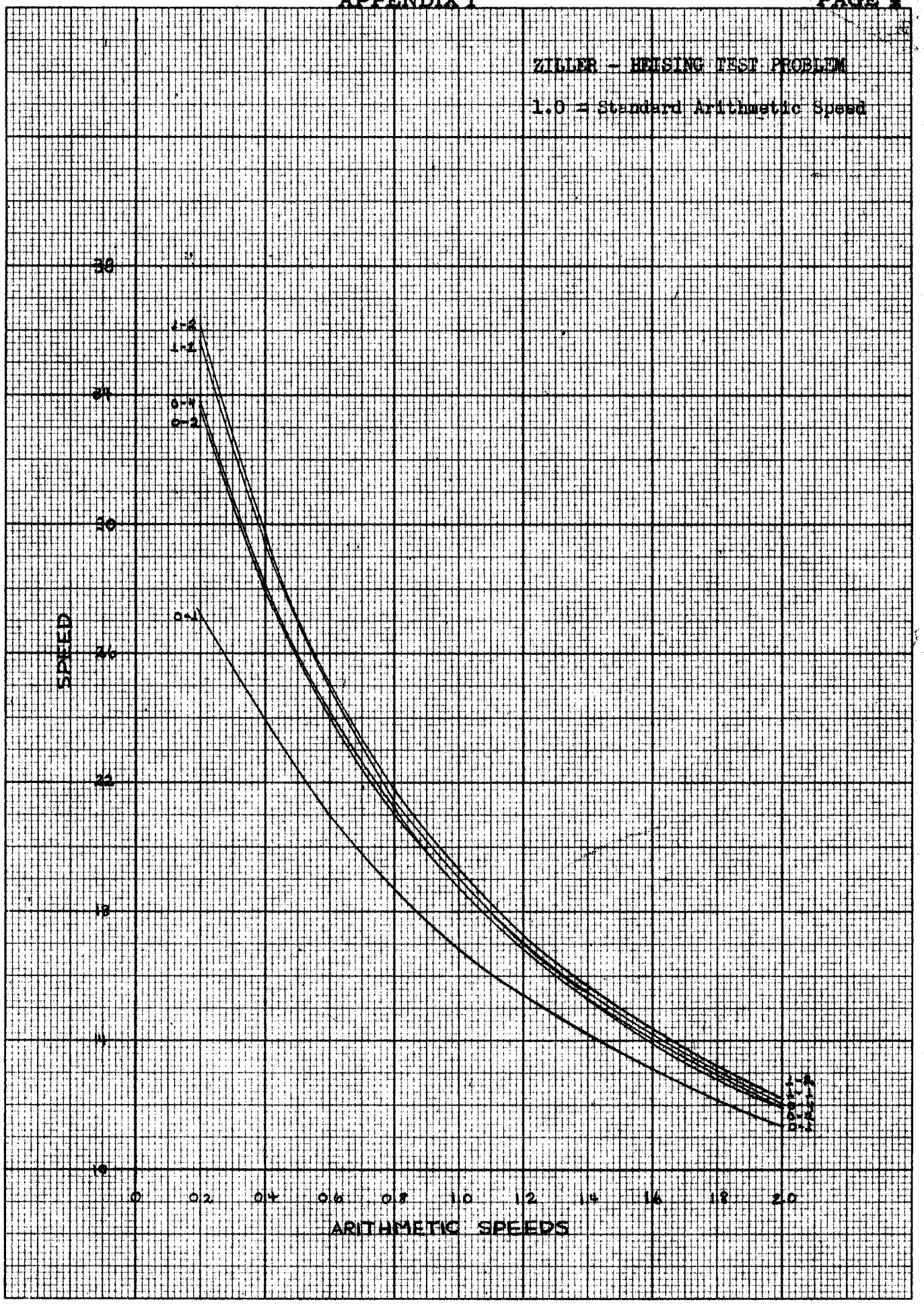


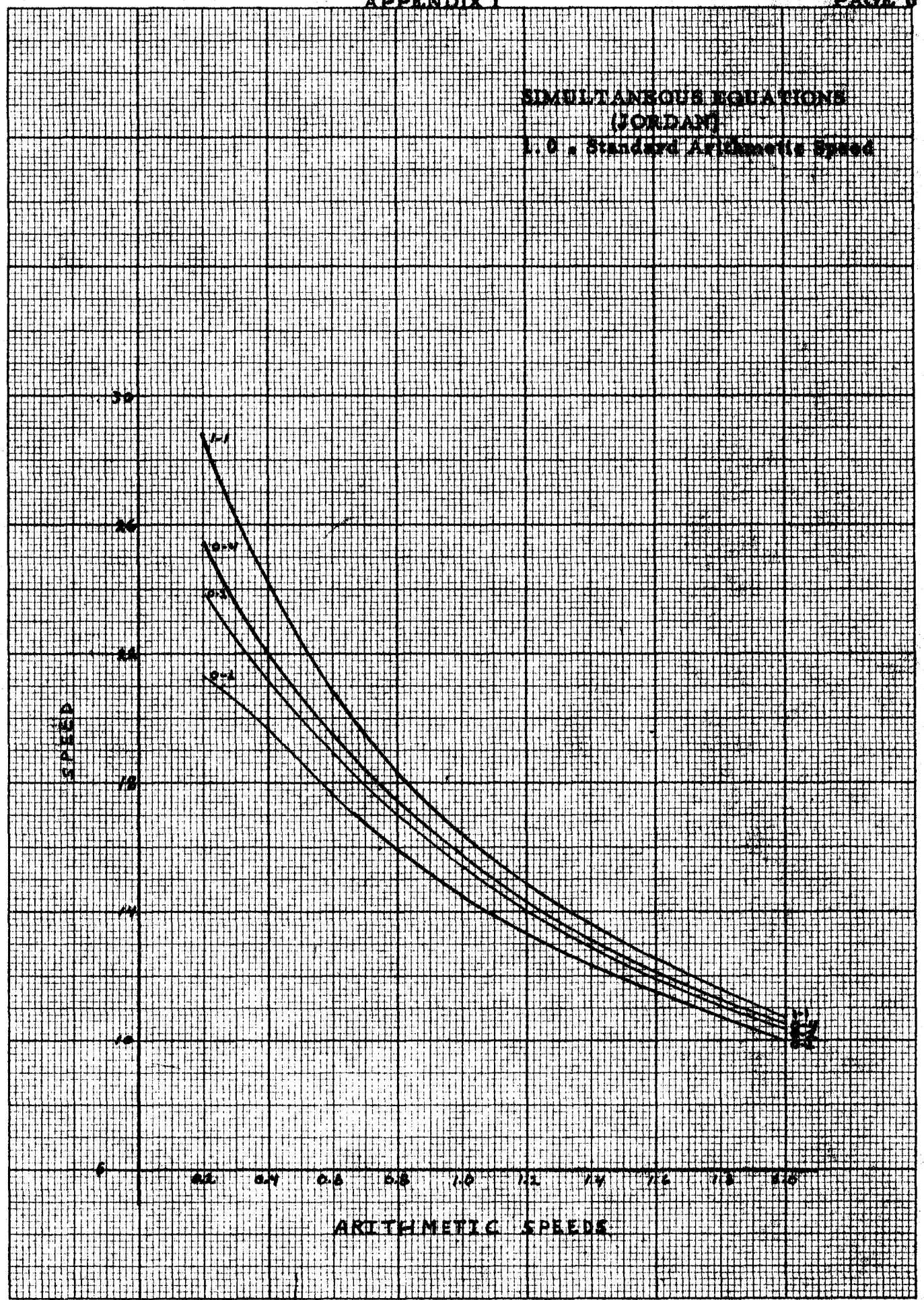


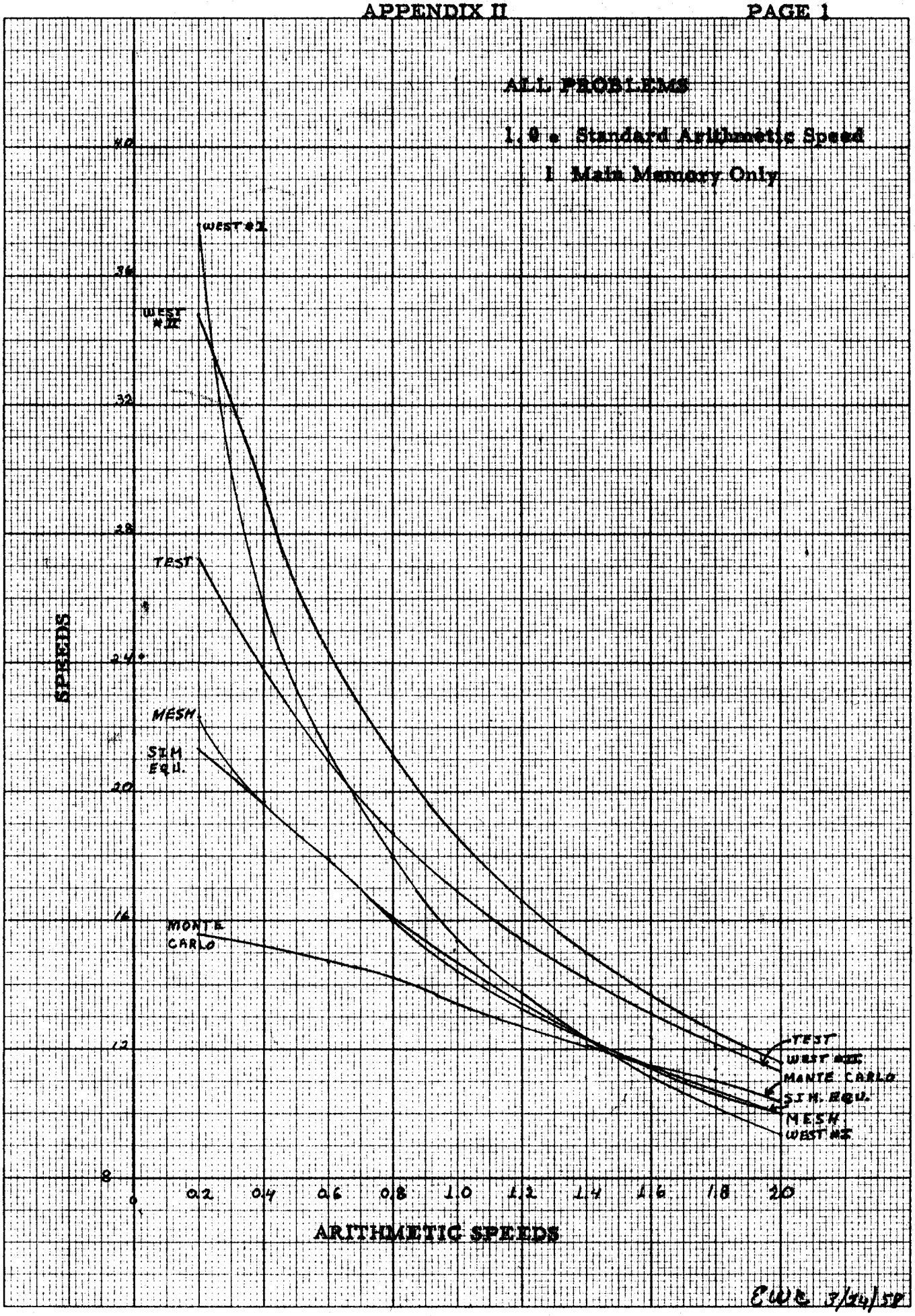


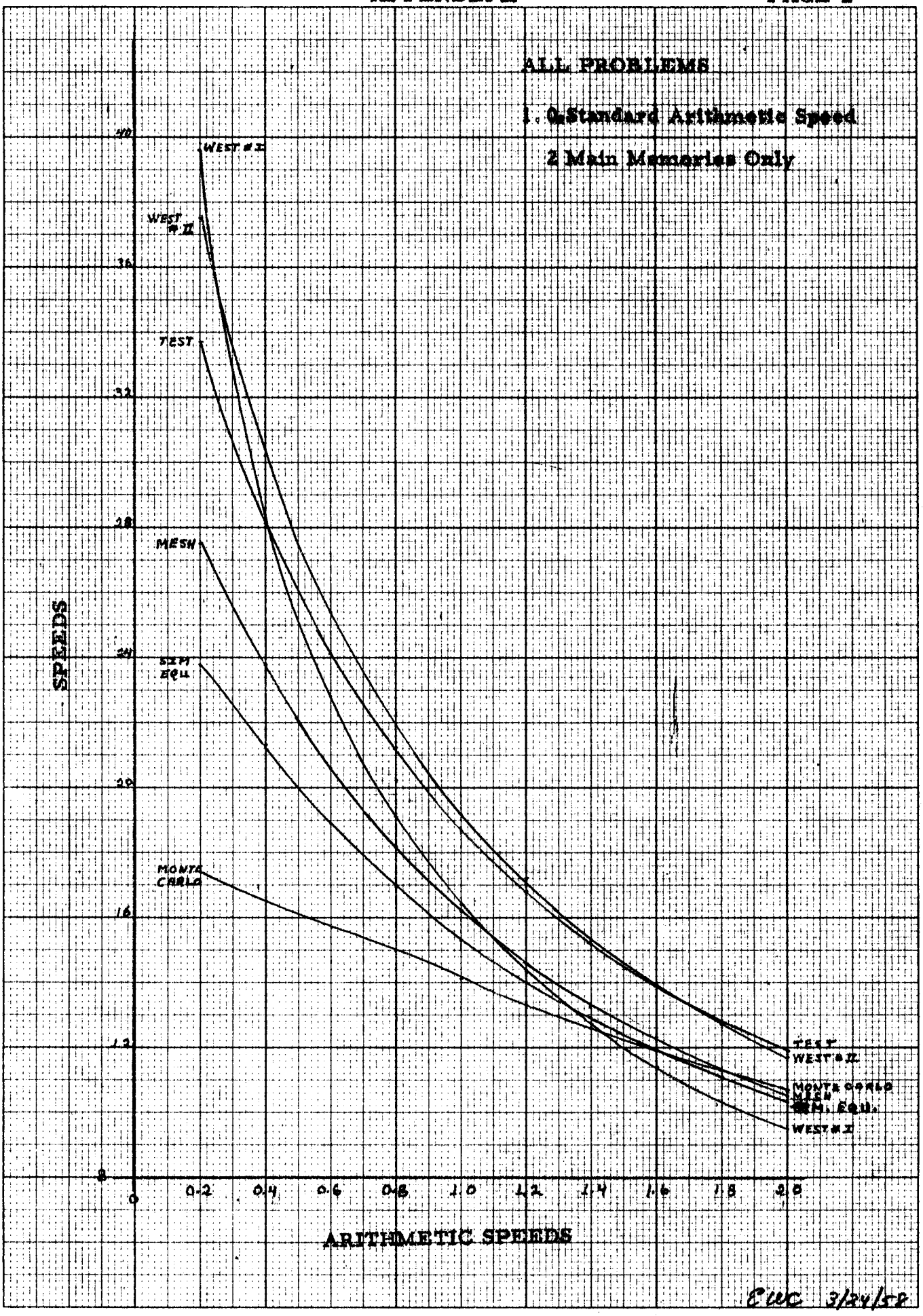


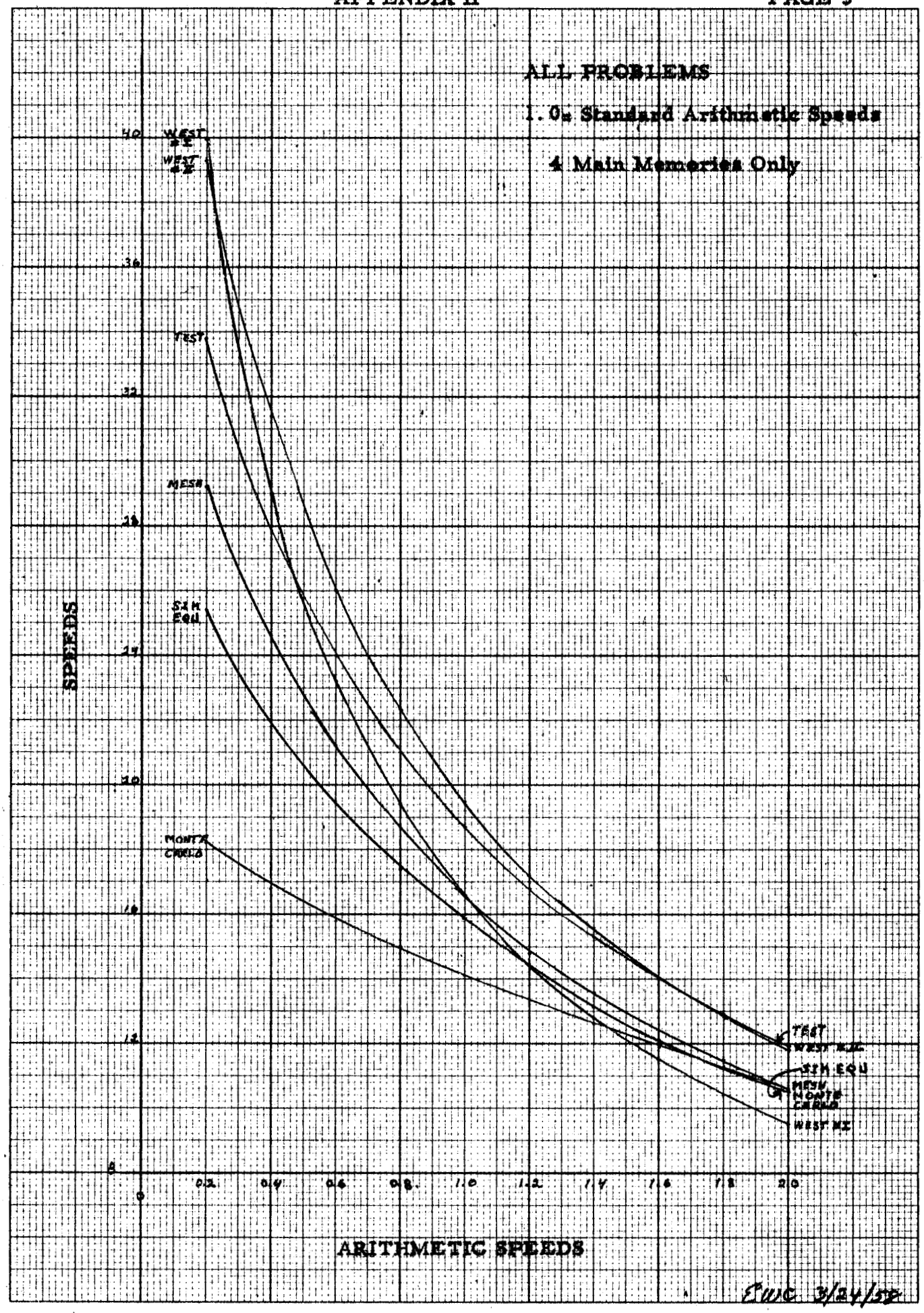


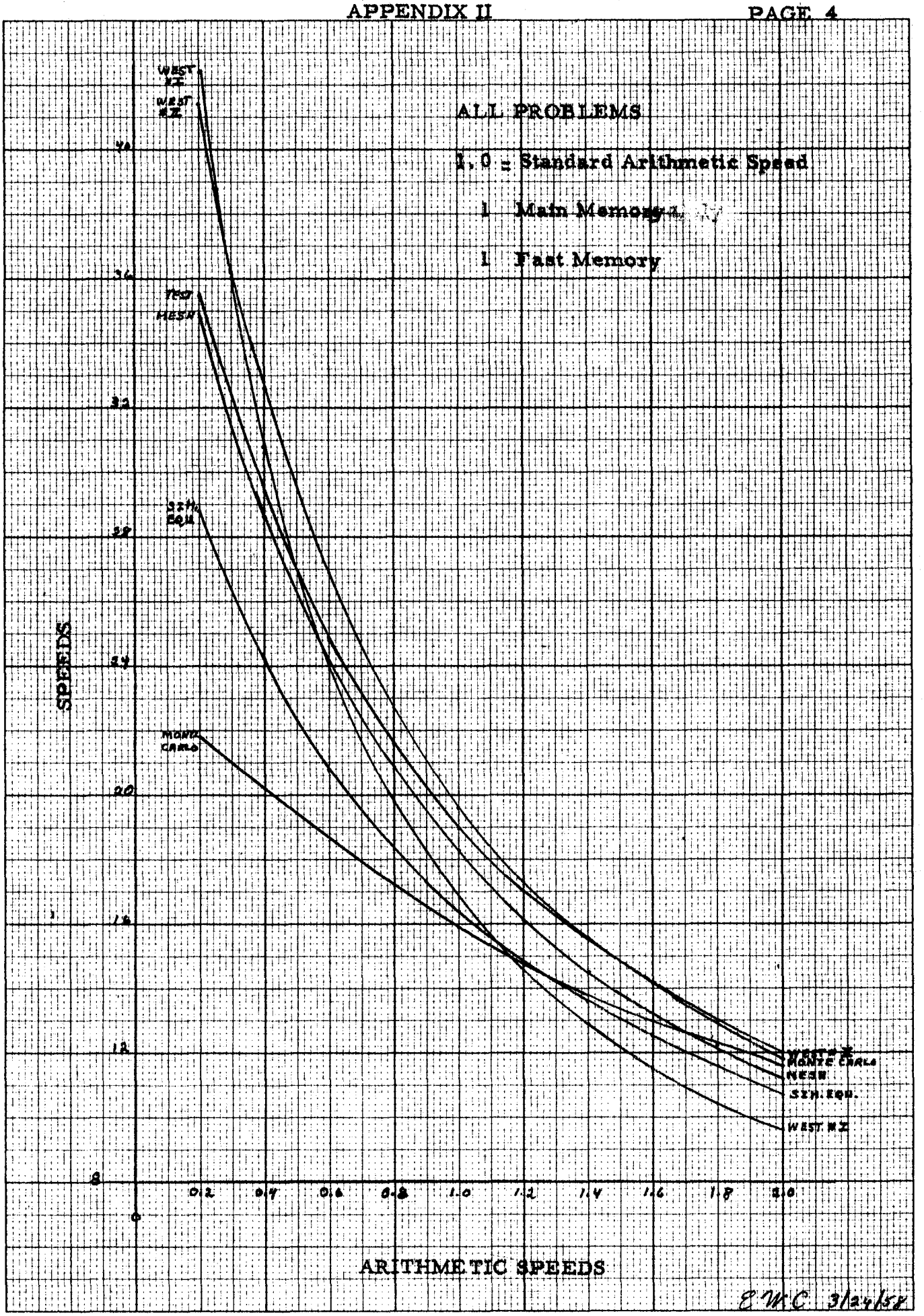
SIMULTANEOUS EQUATIONS
(JORDAN)
1.0 = Standard Arithmetic Speed



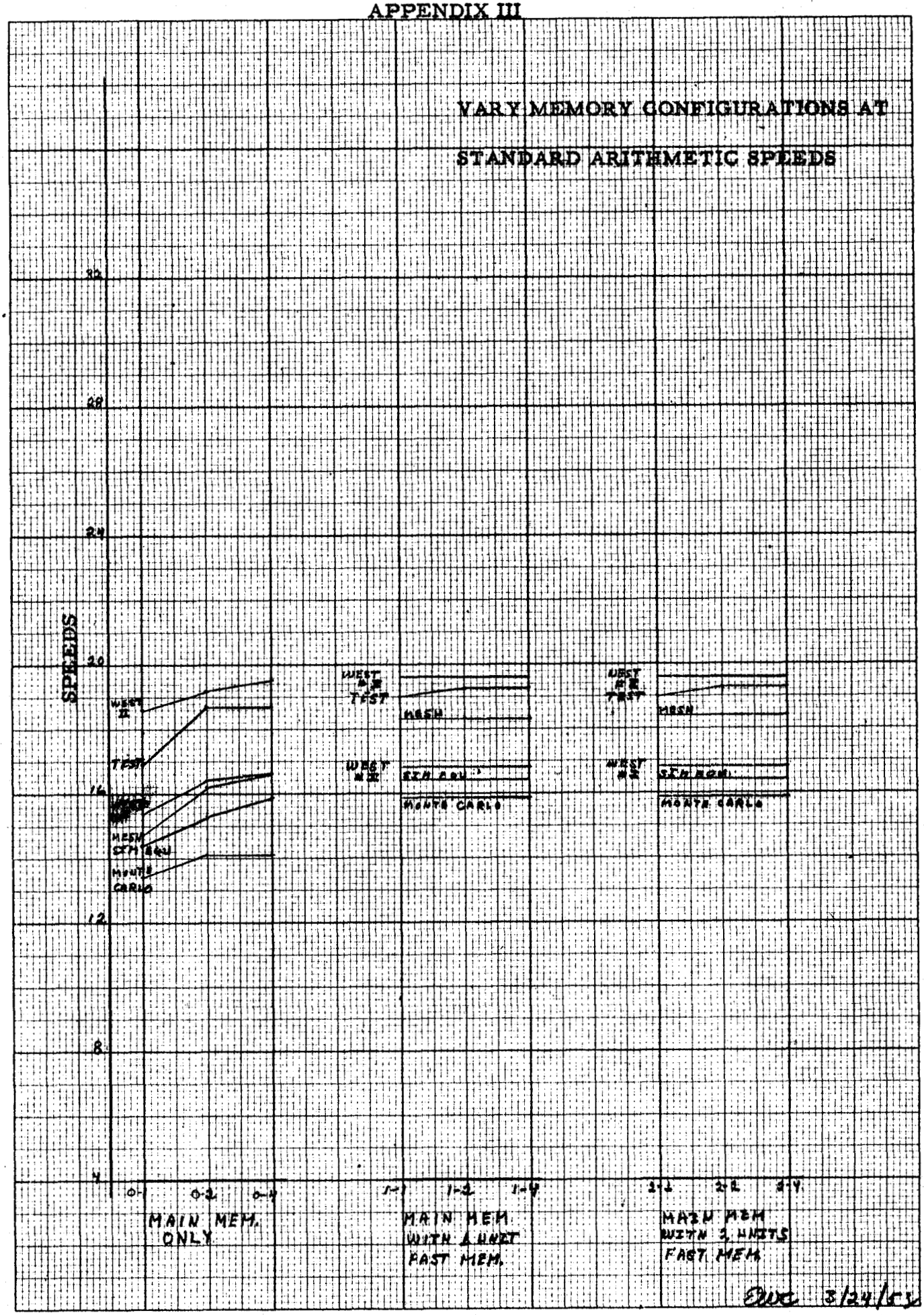




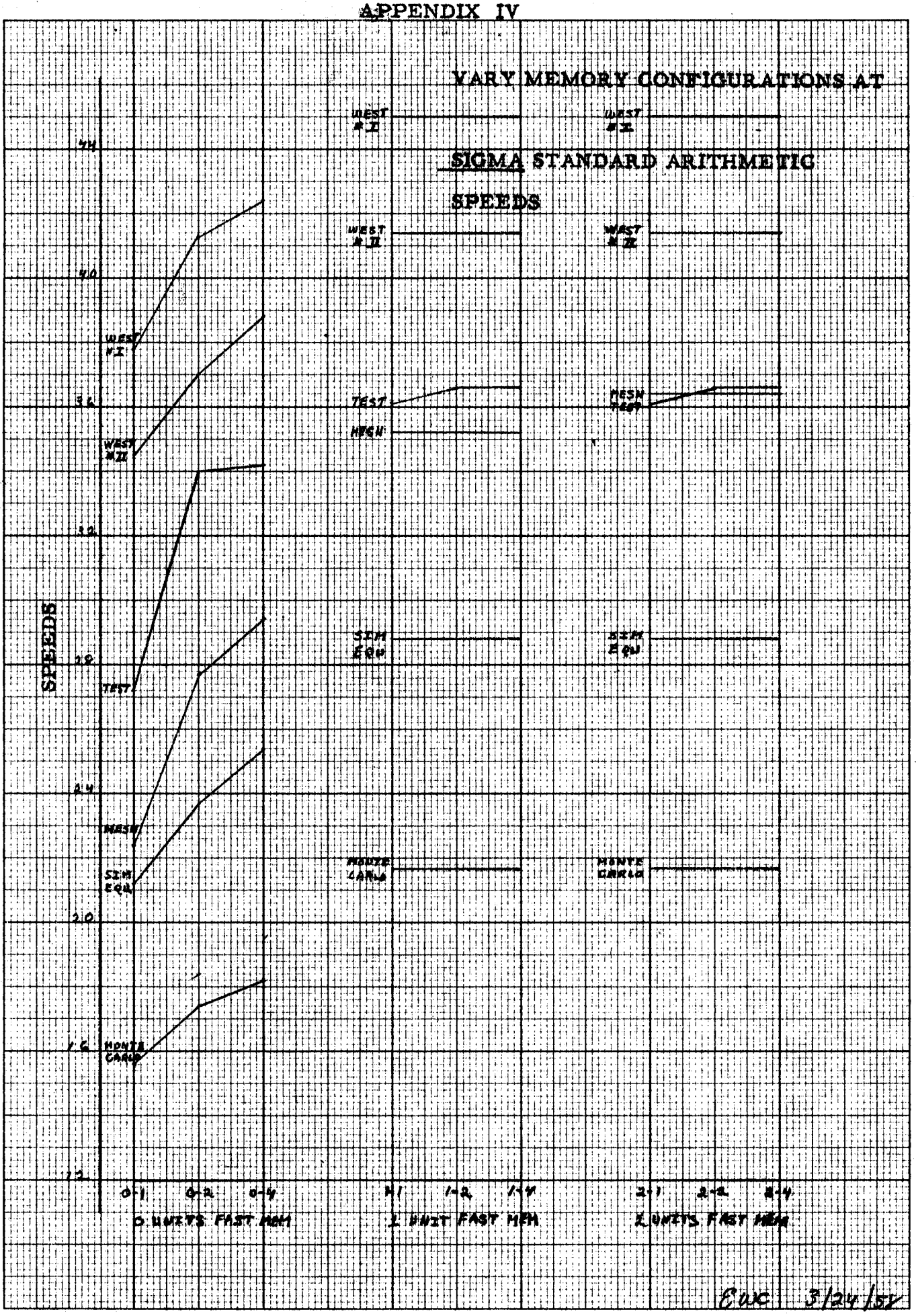




APPENDIX III



APPENDIX IV



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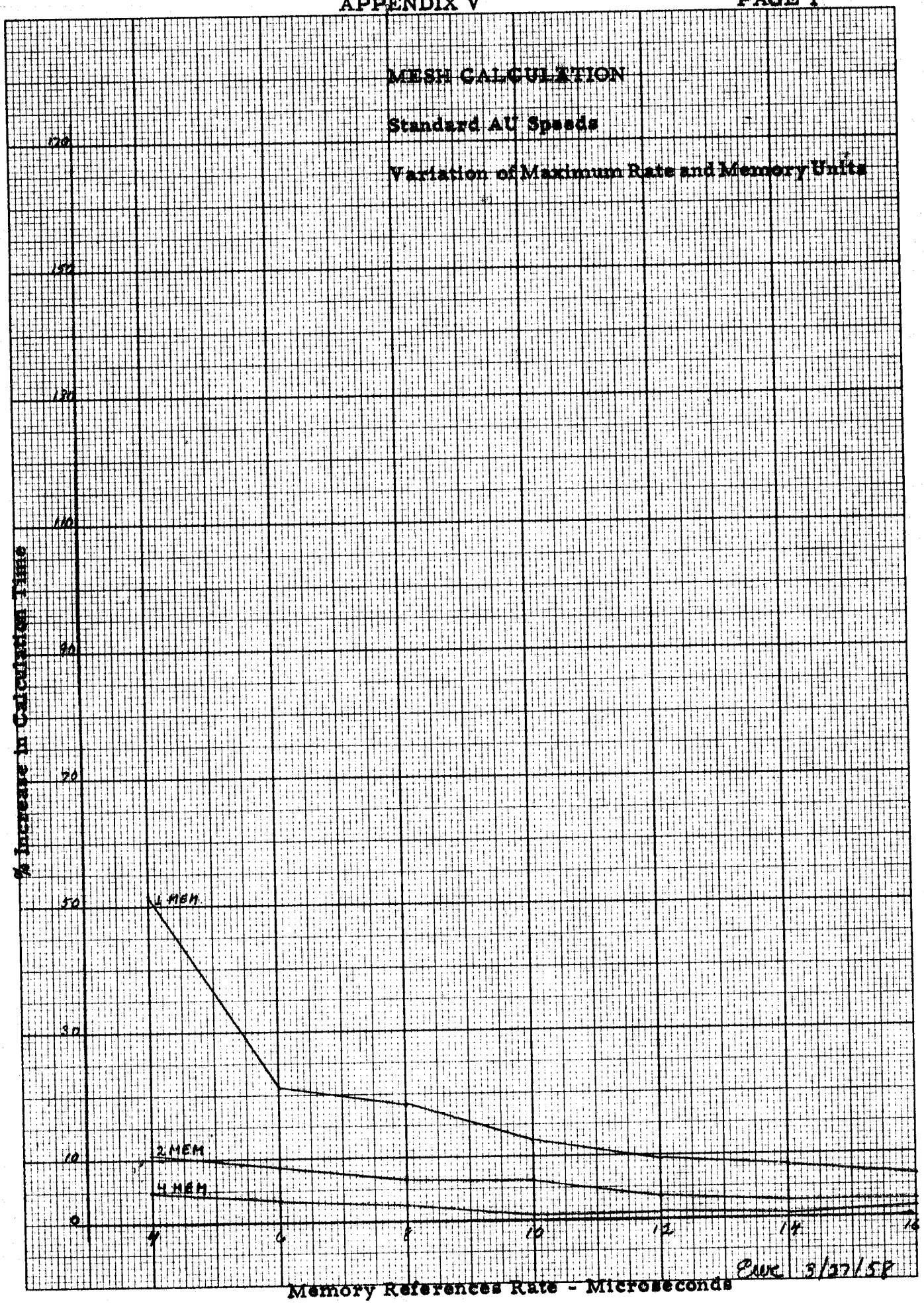
MESH CALCULATION

Standard AU Speeds

Variation of Maximum Rate and Memory Units



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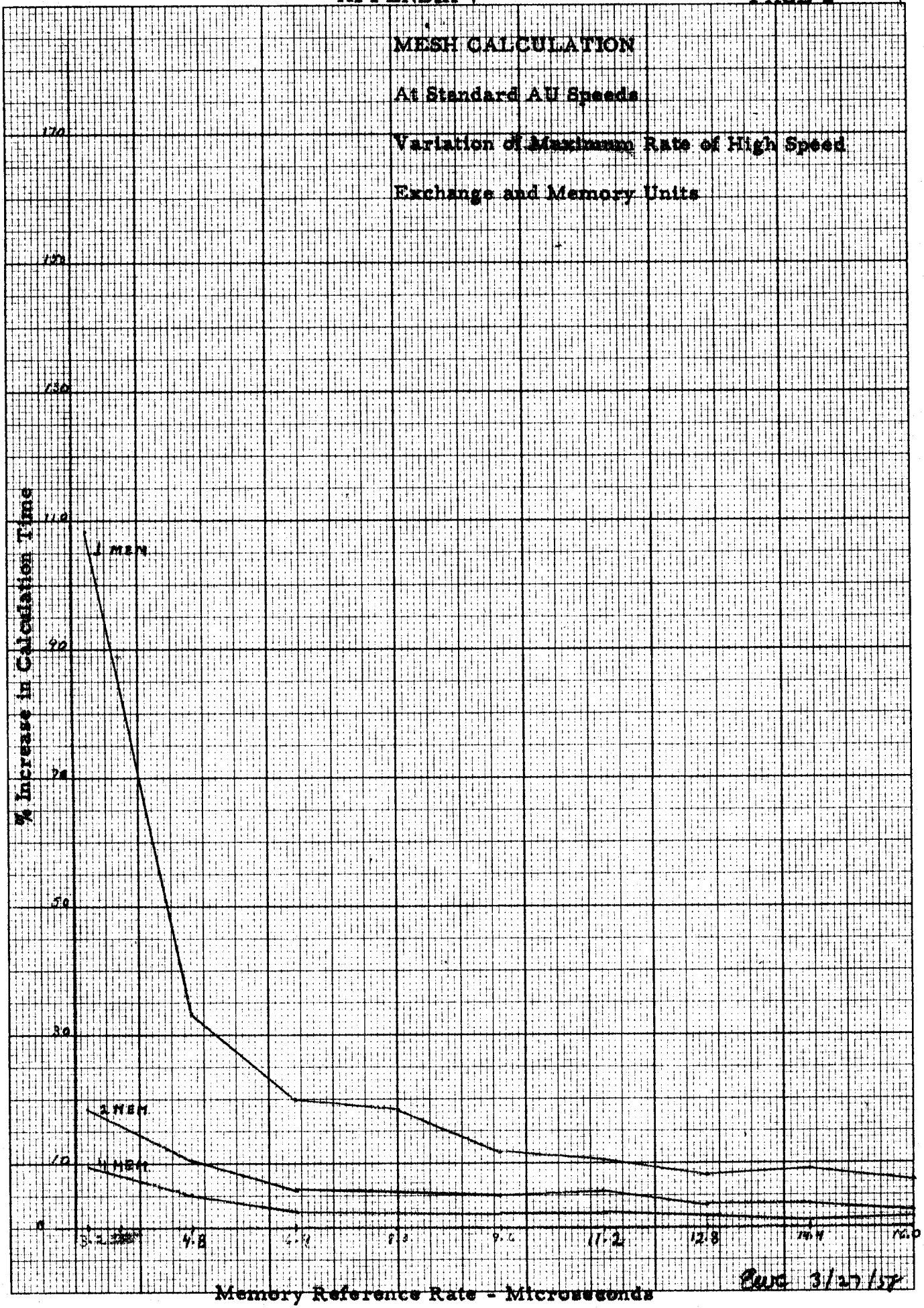
MESH CALCULATION

At Standard AU Speeds

Variation of Maximum Rate of High Speed Exchange and Memory Units



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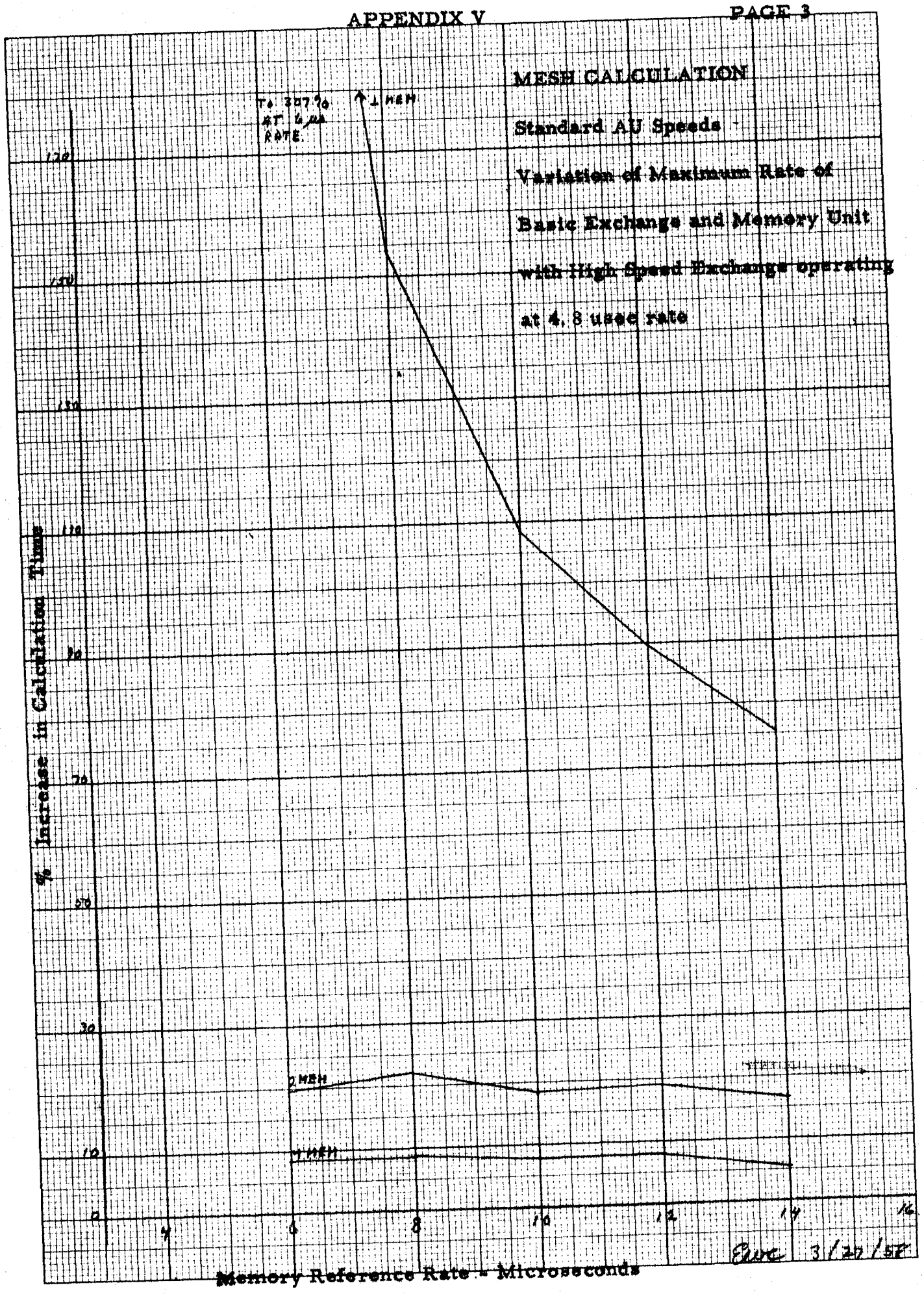
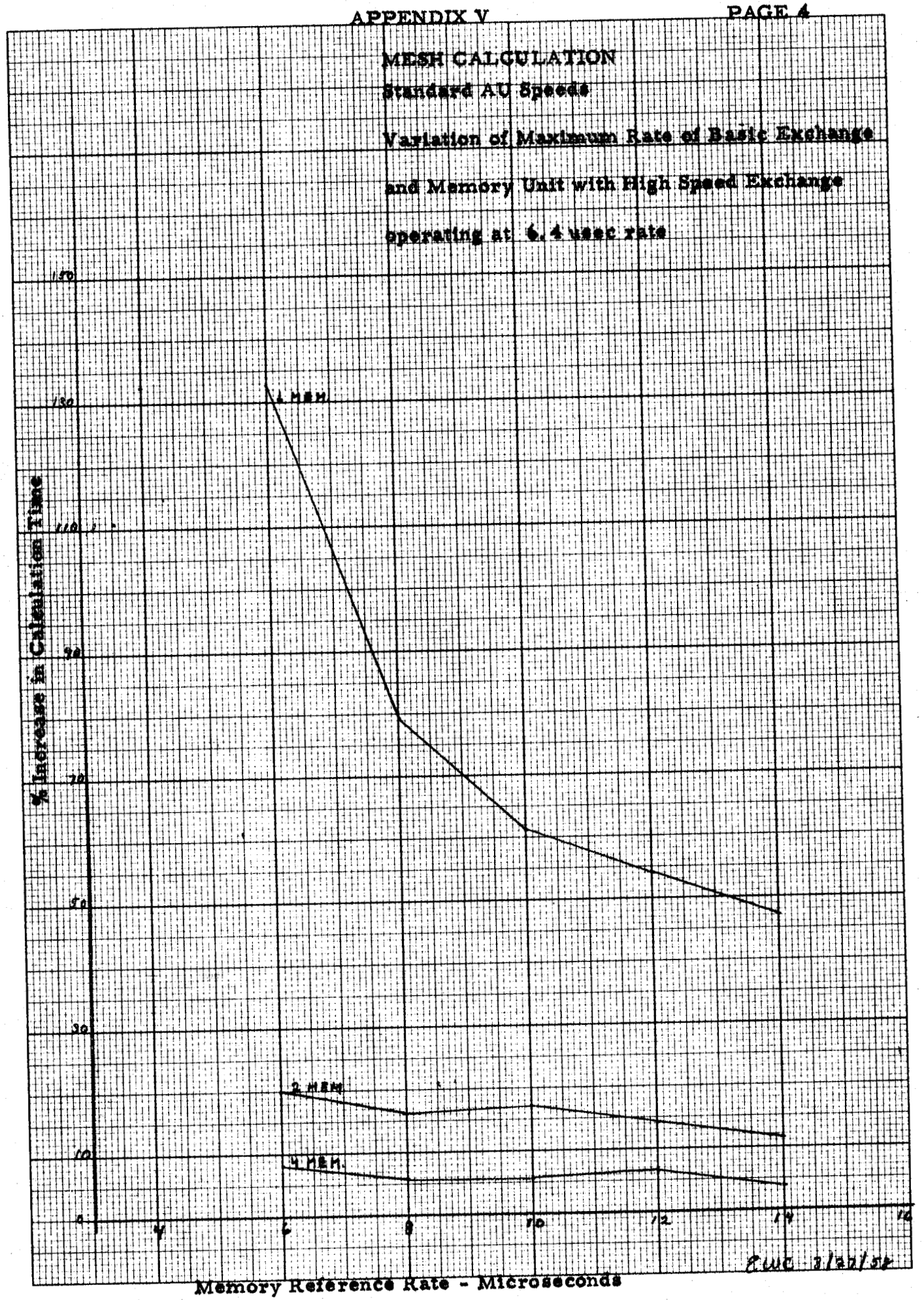
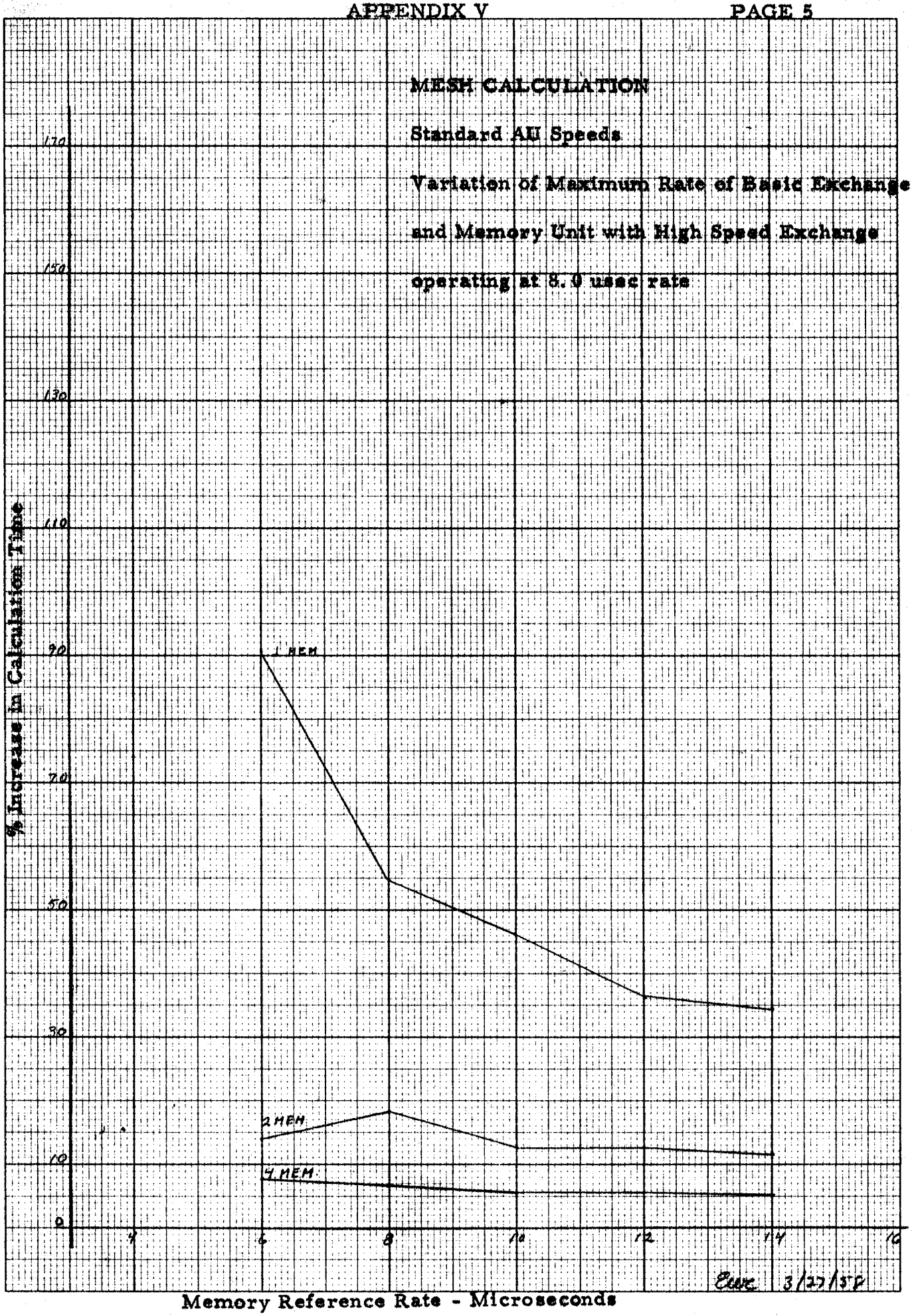
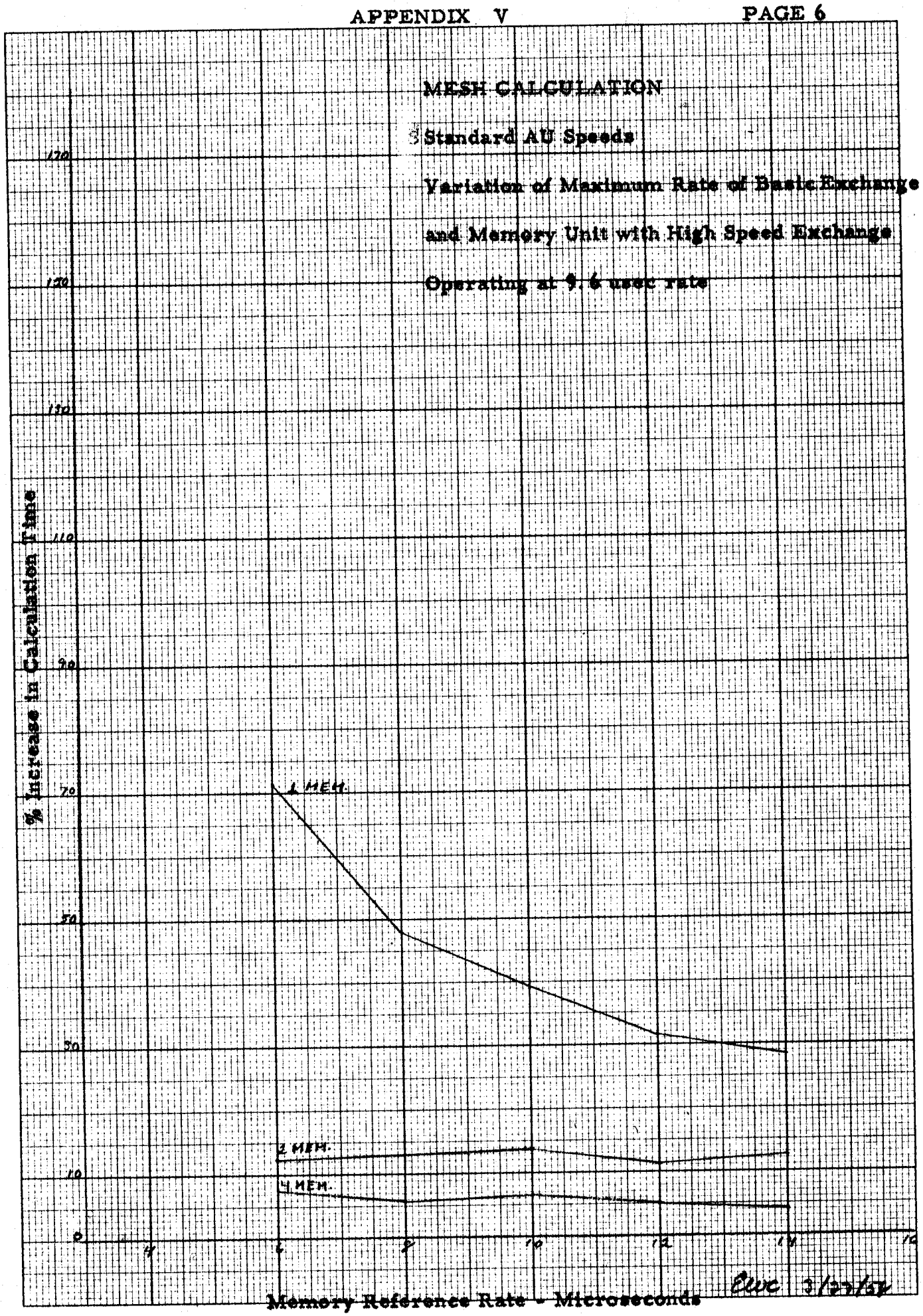


MESH CALCULATION
Standard AU Speeds
Variation of Maximum Rate of Basic Exchange
and Memory Unit with High Speed Exchange
operating at 6.4 usec rate



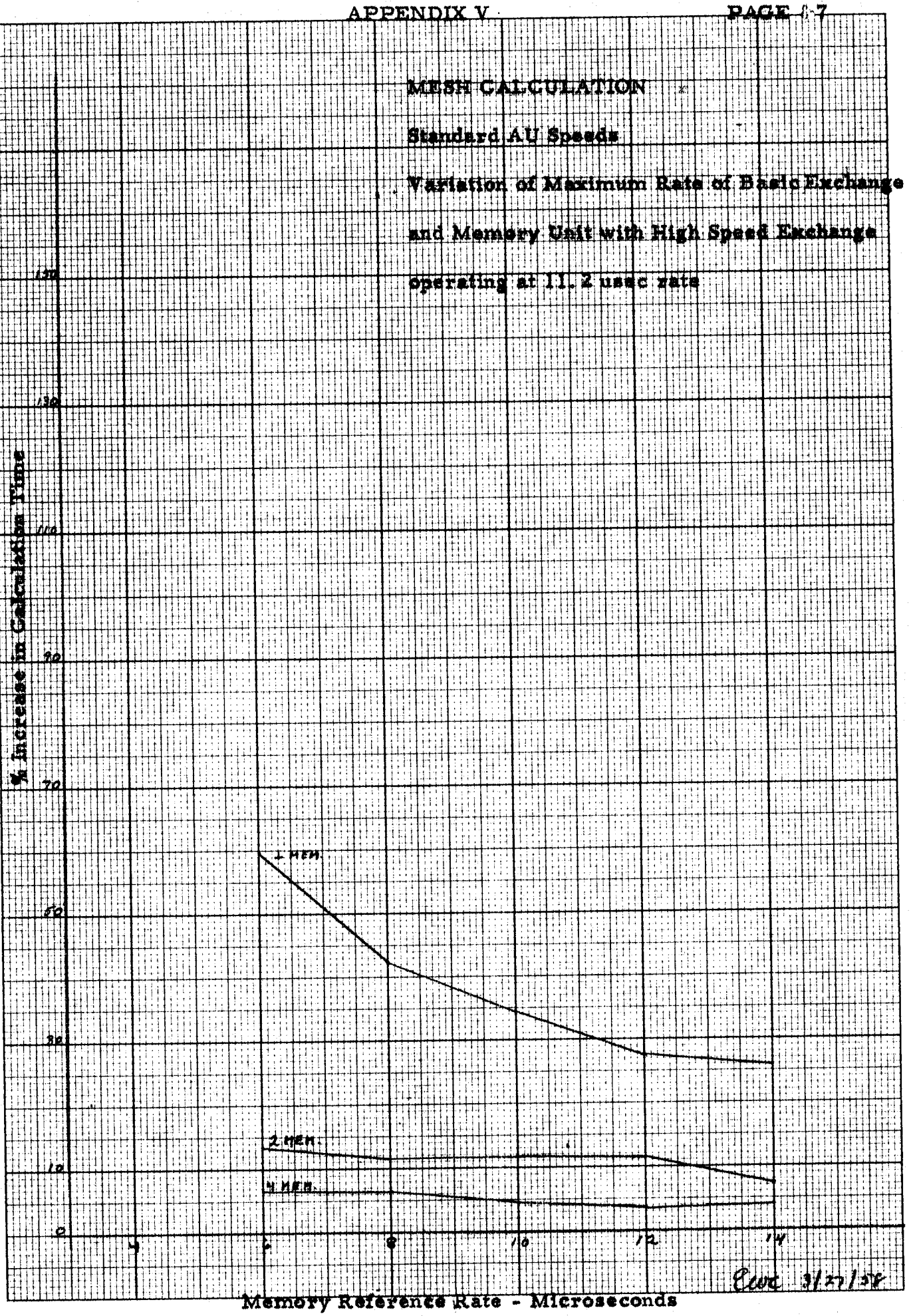




MESH CALCULATION

Standard AU Speeds

Variation of Maximum Rate of Basic Exchange and Memory Unit with High Speed Exchange operating at 11.2 usec rate



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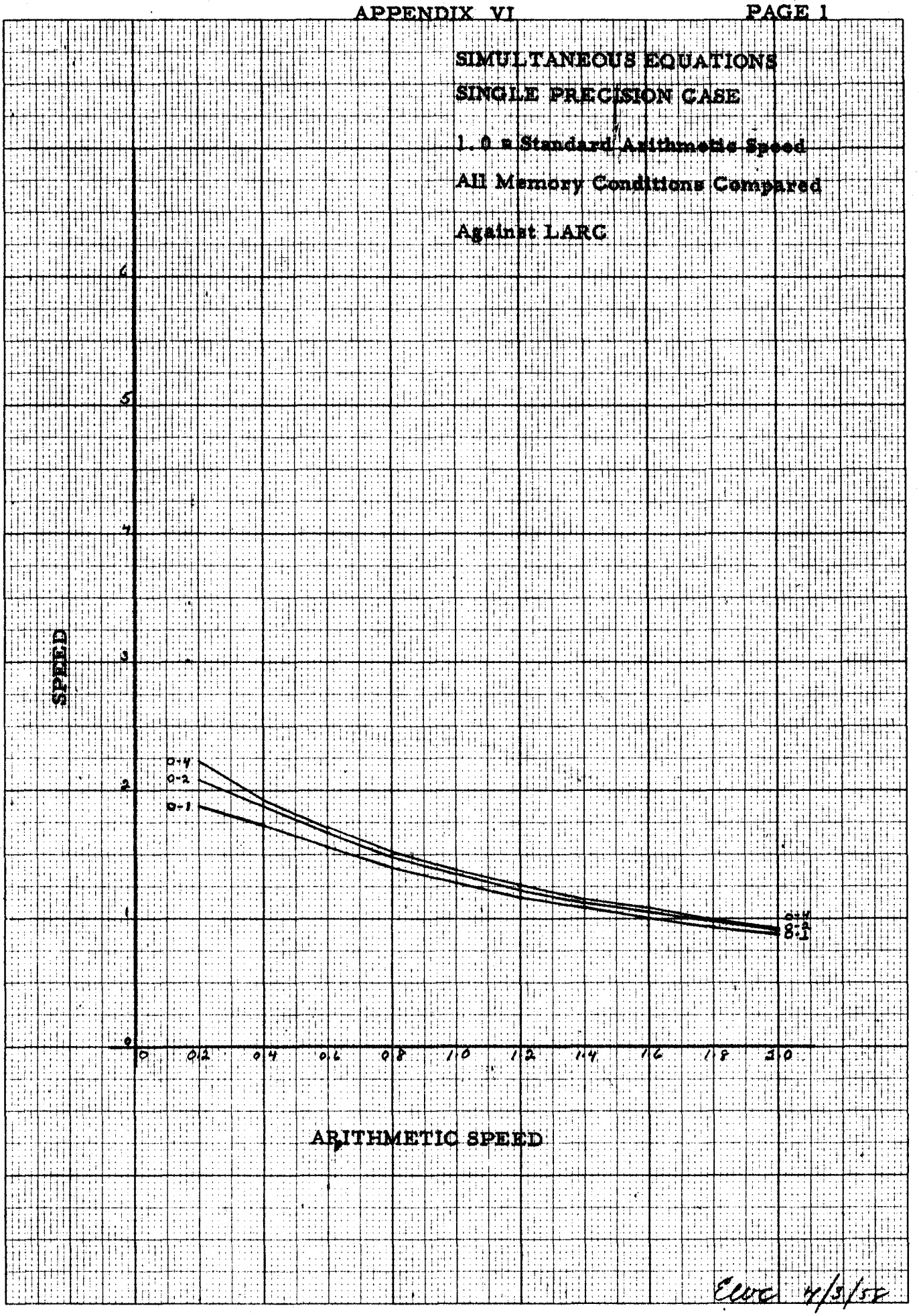
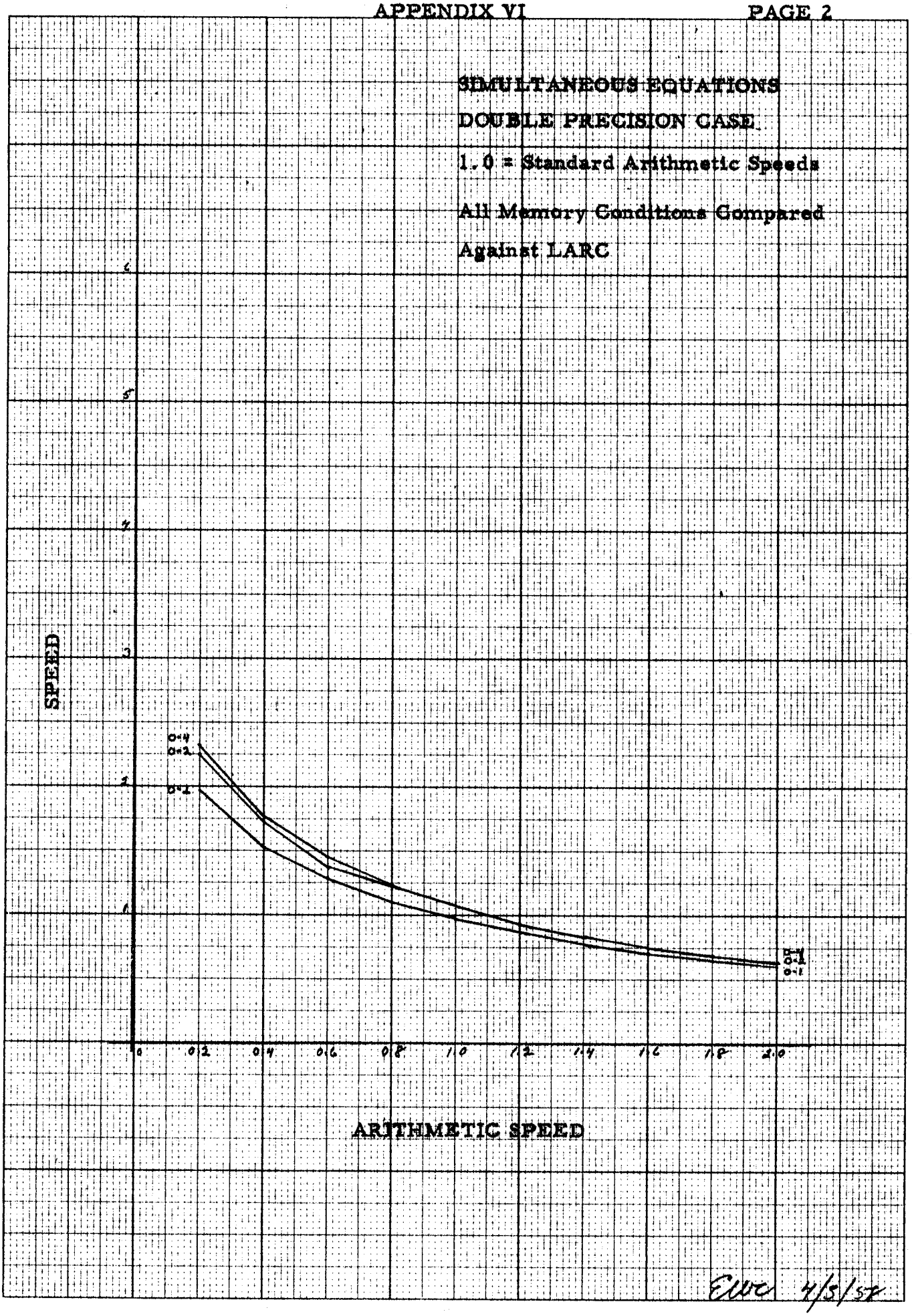
SIMULTANEOUS EQUATIONS
SINGLE PRECISION CASE
1.0 = Standard Arithmetic Speed
All Memory Conditions Compared
Against LARC



Eww 4/3/57



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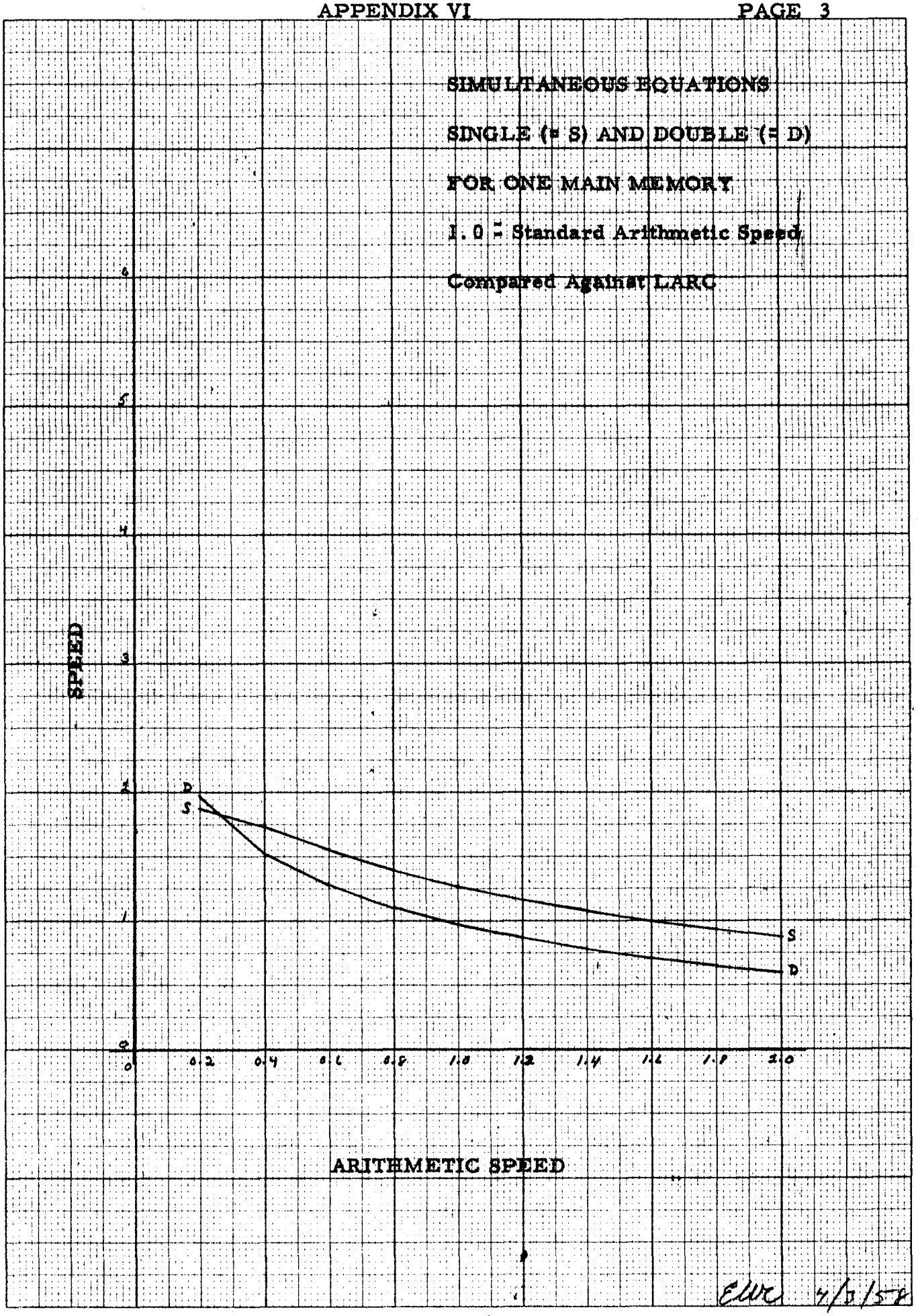

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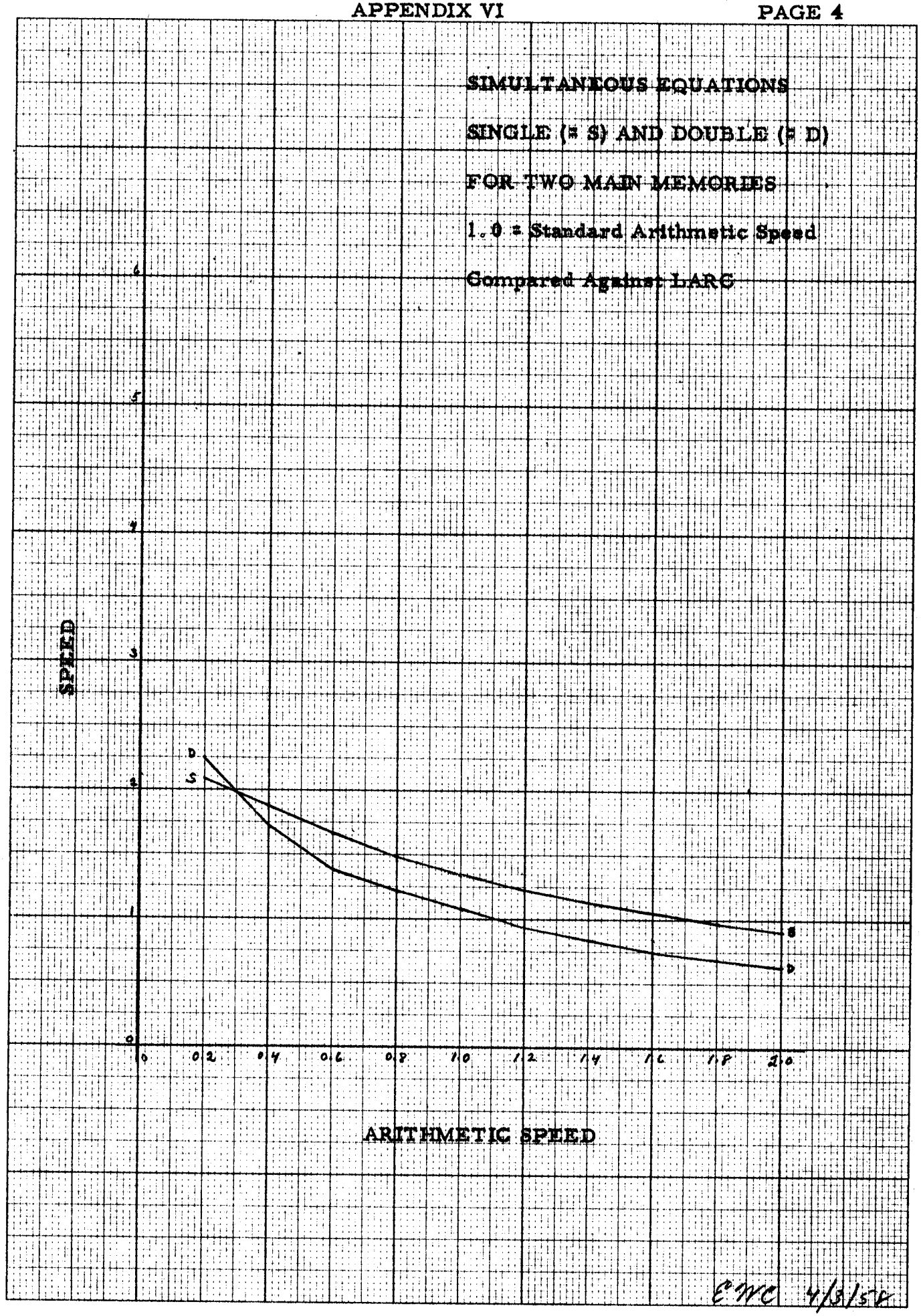

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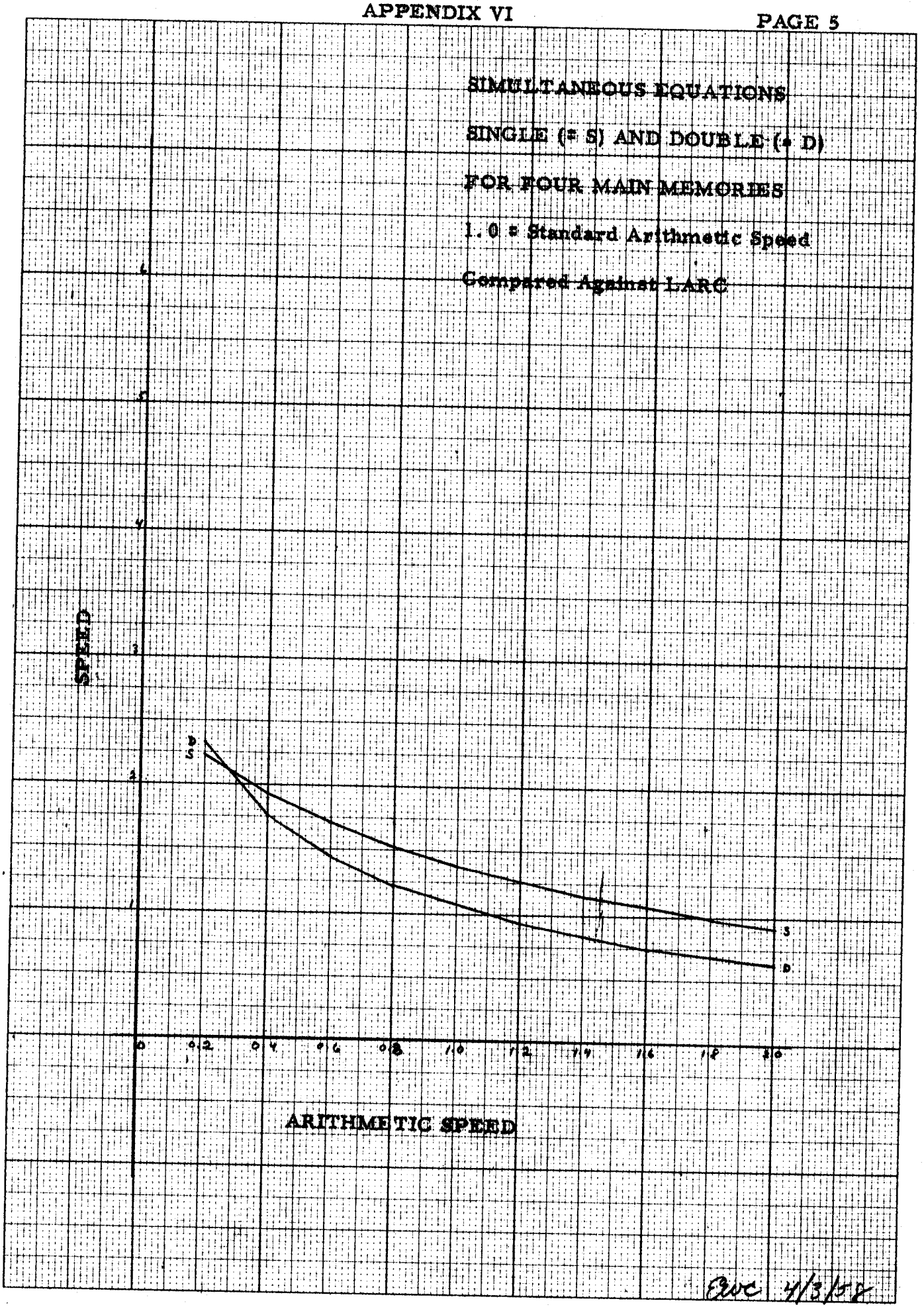

EWC 4/3/58