J. Cocke

BASIC COMPUTER MEMO # 10

SUBJECT: Hamming Checking/Correcting in the Basic System

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PURPOSE: To describe the proposed method for incorporating full word checking and correcting circuitry in the Basic Computer.

DESCRIPTION:

The attached drawing shows the proposed arrangement of a combination Hamming checker/corrector/ generator - Parity checker/generator box on the internal bus of the computer and its relation to the external memory busses and control unit.

Words coming from memory are gated directly into selected computer registers through a special "cascode gate" circuit. Selection is accomplished by decoding the return address in memory before gating the accessed word onto the memory out bus. The out bus contains as many select lines as there are registers to receive data. One of these select lines is energized as the word is placed on the bus.

As soon as the word is received into the computer register, it requests access to the internal bus and the common checking box. If the bus is available, the word is synchronized with the internal bus controls and gated out through the checker and back into the same register in one cycle. In the checker the word is checked, corrected if necessary, and the required parity bits are generated.

To store data in memory, the word has to be first gated onto the internal bus to the checker and back again. In this cycle the word is parity checked and Hamming E. C. C. is generated. It is then sent to the bus control unit where priority is established between Exchange, instruction box, and execution box requests.

For internal computer register to register transfers, the words are transmitted on the internal bus while being parity checked in the common checker.

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At the present time the sharing of one checker for the three operations does not appear to limit the basic system. The biggest problem associated with the system appears to be in controlling the internal bus. This problem and other details of the systems are currently being worked on..

ADVANTAGES:

This system evolved from a recent study of checking in the computer versus checking on the external memory bus. Members of the Harvest, Basic, Bus control and Exchange design groups participated in the study and generally agreed upon the proposed scheme. From the results of the study the following advantages were instrumental in deciding on this system:

1. Ability to share common Hamming Checker as a parity checker on internal bus.

2. Ability to use one Hamming Checker for checking incoming data and for generating ECC on outgoing data.

3. Memory bus capacity is unimpaired giving the computer the ability to send/receive words at a .2 us rate if needed and providing maximum system expandability.

4. Provides error correcting ability from the time a word leaves a register in the computer to be stored in memory until after it is actually received into a computer register after a fetch.

5. Is as economical as any other known system of checking.

6. Is most compatible with Exchange, Sigma and Harvest requirements.

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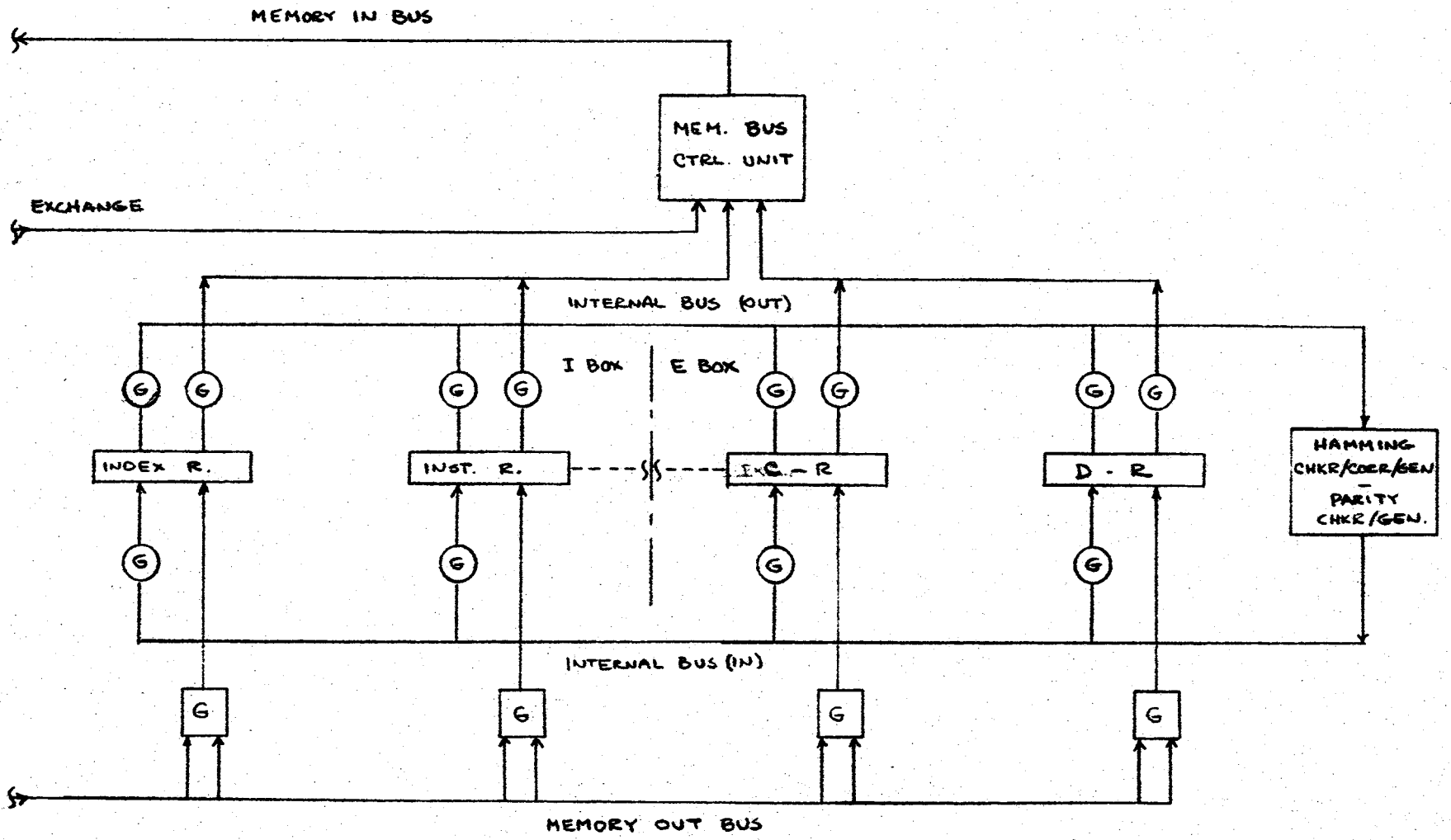
RTB:bjn

BASIC COMPUTER BUS SYSTEM



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RCB.