POUGHKEEPSIE

POUGHKEEPSIE
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Meeting on October 21. 1958 of the following persons:

Messrs.	G. A. Blaauw	H. G. Kolsky
	E. Bloch	O. L. MacSorley
	J. A. Hipp	C. A. Scalzi
	E. I. Jordan	D. W. Sweeney

SUBJECTS:

a) Specification of decimal multiply and divide.
b) Specification of single precision floating point add and divide.
c) Specification of offset for product in VFL binary multiply.
d) Definition of elapsed and real time clock.

RESULTS:

1. The specifications of single precision floating add shall be such that the full 48 bits of the shifted mantissa shall be added to the unshifted mantissa and 48 low order zeros. Truncation to a 48 bit resultant mantissa shall occur after post normalization. A zero result shall be determined from the full intermediate result (96 bits in length).

2. In a single precision floating point divide (DIV) and divide interchanged (DIVI), a 48 bit unrounded quotient mantissa is obtained with no remainder.

   Divide double (DIVD) is as presently defined except a 49th quotient bit is developed and placed in the accumulator at bit position 60. This additional quotient bit is not checked.

3. A 36 bit elapsed and real time clock employing a 17th index core storage register appears feasible. A real time clock will definitely be incorporated in the machine but its exact definition may be modified by the ability to use index core storage. It is not advisable to state tolerances on the clock which result in special maintenance problems.

4. Engineering Planning and Product Planning will investigate variable vs. fixed offset for the binary VFL multiply instruction.

5. Decimal multiply-divide instructions may be implemented in the following ways:

   a. Built-in instructions using a decimal adder.

   b. Built-in instructions using a decimal adder and in addition provide two memory to accumulator convert instructions (decimal to binary and binary to decimal.)

   c. Two memory to accumulator convert instructions (decimal to binary and binary to decimal). Decimal multiply-divide would be programmed.

   d. The conversion instructions stated in (b) and in addition pseudo instructions by which the computer automatically executes a program of four or five instructions to accomplish decimal multiply-divide.

All groups represented will study the above for acceptability.

E. I. Jordan

EIJ:am