POUGHKEEPSIE
Department 539
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FILE MEMO

SUBJECT: Actuation of Indicators and Consequent Effect on Machine Operations

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The indicators can be grouped into three classes according to the effect they have on the computer operation in progress at the time they are actuated.

Class C - Complete Operation
Actuation of the indicators in this class has no effect on the computer operation in progress.

Class T - Terminate Operation
Actuation of the indicators in this class causes the computer operation in progress to be terminated when the condition for actuating the indicator arises.

Class S - Suppress Operation
Actuation of the indicators in this class causes the computer operation in progress to be completely suppressed with the exception of the setting of certain specified indicators and changing the state of the interruption system if specified.

In order to discuss the effect of the indicators on machine operations, it is necessary to keep in mind the machine elements which are subject to change by these operations. These are:

1. Addressable Memory

   a. When specified by an actual memory address in the operation.

   b. When implied by the operation. These locations are the accumulator, R register, M register, the indicator register, and the left zeros and all ones counts.

   c. When specified by some designation other than their memory address. This applies to index registers specified in the I and J fields of an instruction.

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Note: When the elements listed in b and c, above, are mentioned specifically by name in this memo, the statement made about them is valid only when they are designated as described in b and c. When these elements are addressed by their actual memory address, the statements pertaining to all memory locations apply also to them.

2. Instruction Counter

   a. By stepping in the normal sequence of instructions.

   b. By replacement through the action of a successful branch operation.

3. State of the Interruption System, Enabled or Disabled.

The machine instructions can be placed into two general classes, single-level and multiple-level. The single-level instructions specify that one basic operation be performed; the multiple-level instructions can specify a succession of basic operations. A majority of the instructions are in the single-level class. Those in the multiple-level class are the transmission operations, TRANSMIT and SWAP; the execution operations, EXECUTE and EXECUTE INDIRECT; and the LOAD INDIRECT operation.

The effect of the indicators on the single-level operations will be discussed first.

Class C - Actuation of the indicators in this class has no effect on the operation being processed by the computer. The operation proceeds to completion in accordance with the defined rules for the operation. All machine elements normally affected by the operation are acted upon in the usual manner. The indicators in this class are:

3	Exchange Control Check indicator
5-6	The attention request indicators
10-14	The input-output status indicators.
23-24	The Lost Carry and Partial Field indicators
26-35	The floating point result exception indicators
36-38	The data flag indicators

39 The Index Flag indicator, except in the operations COUNT AND BRANCH and COUNT, BRANCH AND REFILL when the system is enabled and the XF mask bit is one.

48-63 The index result and arithmetic result indicators and the Noisy Mode indicator.

Class T - Actuation of the indicators in this class cause the computer operation in progress to be terminated. There is no requirement to restore to the original state any machine element or condition which has been changed in the normal sequence of the operation up to the point of termination. However, the contents of all addressable locations not normally affected by the operation up to the point of termination are guaranteed not changed, except in the case of machine malfunction. The instruction counter has been stepped.

The indicators in this class are:

0-2 Control Check, Arithmetic Unit Check and Memory Check indicators.

Since these indicators represent equipment checks, there can be no guarantee that any specific machine element is in its original state.

25 Zero Divisor

The operation is terminated before any arithmetic action has taken place. The accumulator and the R register remain as before the operation. When the operation is terminated, the data flag indicators have been set according to the data flag bits of the memory operand, if any. The To-Memory indicator has been turned off. If progressive indexing was specified, it has taken place and the associated indicators have been set. The instruction counter has been stepped.

Class S - Actuation of the indicators in this class cause the operation in progress to be suppressed. All machine elements are in their original state with the following exceptions:

1. The setting of indicators in this class.

2. The setting of the asynchronous indicators which may have been actuated by the exchange during the attempt to execute the suppressed computer operation.

3. The stepping of the instruction counter.

4. The changing of the state of the interruption mechanism if specified.

The indicators in this class are:

7-9 The input-output reject indicators

16 The Operation Code Invalid indicator

17 The Address Invalid indicator

20 The Data Store indicator

21 The Data Fetch indicator if the DF mask bit is one

22 The Instruction Fetch indicator if the IF mask bit is one

39 The Index Flag indicator in the operations COUNT AND BRANCH and COUNT, BRANCH AND REFILL if the XF mask bit is one and the system is enabled.

Note: If any of the above indicators is actuated at any stage of a single-level operation, the entire operation is suppressed. Take, for example, the operation STORE INSTRUCTION COUNTER IF COUNT, BRANCH AND REFILL, which specifies a branch if the count reaches zero. Assume that the count would normally reach zero as a result of the operation but that the refill address of the specified index register is invalid. Since a Class S indicator is actuated, the entire operation is suppressed. By this is meant that the counting does not take place, the index value field is not changed, and the instruction counter contents are neither stored nor replaced by the branch address. Suppression of the operation does not suppress the normal stepping of the instruction counter.

The operation receives the exact same treatment if the STORE INSTRUCTION COUNTER address or the branch address of the operation actuates a Class S indicator. However, it should be noted that neither of these addresses can actuate an indicator if the condition for branching is not met.

The instructions in the multiple-level class may be considered to consist of two or more single-level operations which for the purposes of this description are called sub-operations. The indicators which may be actuated by those sub-operations affect them in the same way that they affect the single-level operations. However, although actuation of a Class S indicator causes the sub-operation in progress and all succeeding sub-operations to be suppressed, the preceding sub-operations which have already been performed are in no way nullified.

The same indicators which cause suppression of single-level operations also cause suppression of the sub-operations of multiple-level instructions. Two other indicators, which are actuated only in the multiple-level operations, also suppress the sub-operations. These indicators are:

18 Indirect Addressing Incomplete

19 Execute Exception

The effect of the actuation of Class S indicators on the multiple-level operations is discussed below. Each operation is treated individually.

LOAD INDIRECT

If a LOAD INDIRECT operation is suppressed at any level by the actuation of a Class S indicator, the effect on the machine elements is the same as the effect when a single-level operation is suppressed.

TRANSMIT and SWAP

If either of these operations is suppressed at any level by the actuation of a Class S indicator, the sub-operations at that level and all succeeding levels are suppressed. However, all preceding sub-operations have been fully performed and are in no way nullified. This includes any transmission in memory which may have occurred at preceding levels.

EXECUTE and EXECUTE INDIRECT

The execute-type operations consist of the functions of the execute-type operation itself plus the execution of a subject instruction. The execution of the subject instruction is the second level of these operations and is not attempted unless all the functions of the first level have been completed.

The EXECUTE operation specifies that the interruption system be enabled before the subject operation is performed. If the subject operation actuates a Class T or Class S indicator, it is terminated or suppressed. Such action has no effect on the enabling of the interruption system which occurred on the first level.

The effective address of EXECUTE INDIRECT specifies the location of a pseudo instruction counter which in turn specifies the location of the subject instruction. If either the location or the effective address of an EXECUTE INDIRECT instruction actuates a Class S indicator, the entire operation is suppressed. Otherwise, the system is enabled, the subject instruction is obtained, and the pseudo instruction counter is stepped accordingly. If the location of the subject instruction or any condition arising during its execution actuates a Class T or Class S indicator, the subject operation is terminated or suppressed. This has no effect on the enabling of the interruption system and the updating of the pseudo instruction counter which have already occurred as functions of the first level of the operation.

It is possible for the execute-type operations to refer to other instructions of the same type to many levels. If a many-level operation is suppressed or terminated at any level after the first, the pseudo instruction counters of all EXECUTE INDIRECT operations on preceding levels have been stepped in memory and the system has been enabled.

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