SERIES 7000 CIRCUIT MEMO #28

SUBJECT: PROPOSED SYSTEM DESIGN FOR THE MEDIUM-SPEED MEMORY

BY: Robert J. Flaherty

Richard C. Lamy

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ABSTRACT: This report gives a general description of the memory array and details the logical functions of the memory unit.

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I. General Description of Memory Array

A. Memory Element:

1. 30-50-12 mil toroid
2. 0.585/1.170 amp nominal drive
3. Element wiring - Figure 1

B. Memory Size:

1. 16, 384 words
2. 72 bits/word
3. No X-Y drive segmenting
4. Sense segment - (4 per plane) 64 x 64 cores
5. Inhibit segment - (4 per plane) 64 x 64 cores

C. Plane Size:

1. 4 segments of 64 x 64 cores
2. Each segment 6" x 6" (includes frame)
3. Packing density - 16 cores/inch in each segment

D. Drive Currents:

1. X-Y current furnished from matrix switch

   a) 585 ma (nominal)
   b) Rise time, 100 mμsec, 10% to 90% + 5%, -20 to-50%;
      Pulse duration & tolerance, 90% to 90%, 400 mμsec ± 10%;
      Fall time, 100 mμsec, 10% -90%
   c) Array X-Y drive delay - 115 mμsec

2. Inhibit currents furnished from direct drive transistor drivers

   a) 585 ma (nominal)
   b) 0.1 μsec rise time; 0.75 μsec flat top; 0.1 μsec fall time (nominal)
   c) The inhibit currents will be staggered in turning on. That is, the Z driver for the first plane will turn on before the one for the 72nd plane.
   d) Since there are 4 Z segments per plane, the memory is designed so that only 1/4

of the Z drivers need be turned on during a memory cycle.

e) Post Write Disturb:

1. 585 ma (nominal)
2. 0.1 usec rise time; 0.1 usec flat top; 0.1 usec fall time (all nominal)
3. The post-write disturb pulse is furnished by the inhibit drivers which were not turned on during the write portion of the cycle. The time at which these drivers are turned on is staggered.

f) Array delay - 50 musec

E. Sense:

1. One sense amplifier per plane

   a) 4 sense segments per plane with 64 x 64 cores each

2. The sense amplifiers require a strobe pulse during the "read" portion of a "Read from Memory" cycle.
3. The strobe pulse is time delayed down the memory planes to take into account the drive line delay.
4. Array Sense Delay - 70 musec

F. Array Delay:

1. X-Y delay - 115 musec (128 x 72 cores)
2. Inhibit delay 50 musec (64 x 64 cores)
3. Sense delay 70 musec (64 x 64 cores)

G. Array Timing Cycle:

1. Figure 2

II. Description of Memory Logic

A. Recognition of Memory and Start Memory Cycle:

1. The Central Control Unit (CCU) in the Bus provides memory recognition and triggers the memory timing ring. The memory sends back a busy signal to the CCU. This busy signal is reset when the memory can accept a new address, allowing for transmission time of the signal to the CCU and for data back to the memory.

B. Memory Address Register:

The Memory Address Register (MAR) gates are controlled by the bus. These 14 gates open and allow the MAR to set up to the configuration supplied by the bus. The MAR is reset during the "write" portion of the cycle. At this time the memory is free to accept new information.

C. Memory Address Decoder:

Figure 3 shows the winding pattern of the 32 input, 16 output matrix switch. The 32 inputs are grouped in pairs of drivers so that there are a total of 16 pairs of drivers for each matrix switch. During the "read" portion of the memory cycle one driver out of each pair turns on. During the "write" portion the other half of each driver pair turns on. The 16 drivers which turn on during read time add power to switch the selected matrix switch core. All other cores receive no effective current due to cancellation. During the "write" portion the other 16 drivers turn on to reset the matrix switch core. Refer to Silo Technical Memo #14.

Figure 4 shows the logical functions which were derived from the winding pattern of the matrix switch. These logical functions select which output of the matrix switch is energized. Figure 5 shows the basic decoder which is used to provide the necessary logical functions for either X or Y dimensions.

The MAR contains the address of the word in memory. Four bits of this address are used for X decoding and 4 bits for Y decoding. Bits A, B, C, D, and their complements, Figure 6, are sent to the "Exclusive Or's" in the manner shown and the logical functions are generated. These func-

tions along with the information bits A, B, C, D, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$ are then brought to the "Switching Exclusive Or's" where they are "exclusive ored" with the output from the, Read/Write, flip-flop. The Read/Write (R/W) flip-flop is true for read time and false for write time. This flip-flop causes the outputs of the "Exclusive Or's" to switch when it changes state. The outputs of the "Switching Exclusive Or's" are tied to driver gates, where they are "anded" with the matrix switch selection outputs. The proper gates are opened to turn on sixteen drivers during the read portion of the cycle. After "read" time the R/W, flip-flop changes its state, thereby changing the output of the "Switching Exclusive Or's". At "write" time the outputs are sampled at the driver gates by the matrix switch selection line and the other 16 drivers of the 16 pairs are turned on.

D. Matrix Switch Selection:

1. In Figure 7, the 6 high order bits (J, K, L and M, N, Q) of the memory address are used to select which matrix switch is to be energized. This does not necessarily have to be so, in that by using the low order bits for this purpose, the word locations within a memory unit may be staggered. For instance bits A, C, E could be used to select one group of matrix switches and bits B, D, E could be used for the others. This would stagger sequential addresses throughout the memory unit.

2. Selection Logic:

   All of the eight possible combinations of bits J, K, and L are "anded" with a timing pulse in eight "And" circuits. Since only one of these combinations can be true at one time only one set of 32 gates receive the selection pulse. The same holds true for the bits M, N, and Q. The length of time the drivers are on for "read" and "write" portions of the memory cycle is also set by the timing pulse with which the matrix switch selection bits are gated.

E. Regenerate and Store Logic:

1. Regenerate:

   In a "Read" cycle the memory user is requesting data from the memory. This also means that the memory has to retain the data for any future references. The

"read" portion of a memory cycle destructively reads the data out of the cores which, in conjunction with what was stated above, implies that the same data taken from memory must be written back into the memory location as well as being sent to the memory user. This is done by a regeneration loop.

The memory user sends an address to memory where it is decoded and the proper X and Y drivers are turned on. These switch selected matrix switch cores sending half-select currents down the selected X and Y drive lines. The cores which receive a full select switch (if they are in a "one" state) and induce voltages in the sense wires. The voltages are amplified by the sense amplifiers (S. A.) and the data register is set up to the configuration of the word which was just "read". The true sides of the data register flip-flops are gated to the output bus. The complement sides are gated with the inhibit segment select line and staggered timing pulses. The outputs of the gates are sent through "Or" circuits to the inhibit drivers. The inhibit drivers connected to the planes in which "zeros" were stored are turned on. This provides half-select pulses which are of opposite polarity to the "write" current, thereby cancelling out one of the "write" half-selects and preventing the writing of a "one" into the core. Also necessary, in the memory, are post-write-disturb (P. W. D.) pulses to offset the adverse effects of the half-selects on the cores. The P. W. D. pulses are formed by turning on the inhibit drivers which were not turned on during the write portion of the cycle. The logic for doing this is shown in Figure 8. The true sides of the data register flip-flops are sent to P. W. D. gates as well as the output gates. The P. W. D. gates have three inputs which are:

a) The inhibit segment selection line.
b) Staggered timing pulses. This allows staggering of the turn on time of the drivers to prevent large power drains and noise. These staggered timing pulses occur at a later time than those used during the "write" portion of the cycle.
c) The information in the data register.

The logic for the selection of the inhibit segments is also shown in Figure 8. Bits L & Q are used to determine which segment should be turned on. The 4 possible combinations are "anded" together as is shown and provide

signals to the inhibit gates and the P.W.D. gates.

2. Store:

In a "Write" cycle the memory has to store new data into a memory location. The CCU sends the memory the recognition pulse, the memory address, the data to be stored, and a store pulse. These are gated into the memory by the bus. The memory decodes the address and turns on the X and Y drivers. The data is sent to the data register. The store pulse sets the store flip-flop to its false state and prevents the strobe pulse from turning on the sense amplifiers. It also prevents the data from being gated to the output bus. During the "write" portion of the cycle, the proper inhibit drivers are turned on, in the manner described above, thereby writing the new data in the memory location. The P.W.D. pulses are also generated by the method mentioned above.

F. Special Features:

1. Parity Checking:

The memory address is parity checked. The bus supplies the parity bit as well as the 14 address bits to the memory. The memory address and the parity bit are sent to the parity checking logic (Figure 7) for comparison. If there is an error the signal is gated to the alarm circuit.

2. Address Checking:

There is a need for address checking in a magnetic core memory to determine if the input address was decoded properly and that the correct current drivers were selected.

A scheme for address checking in a magnetic core memory unit has been developed. The method proposed allows address checking to be done during a memory cycle. The method compares the decoded address with the input address.

On each output drive line of a matrix switch a core is placed. Through each core are wound sense lines, a bias line, and the drive line. (Figure 9). The sense

lines numbered 1, 2, and 3 show which of the eight matrix switches were selected. (Figure 10). The other four sense lines show which of the sixteen possible outputs of the matrix switch were selected.

The operation of the encoding matrix is as follows:

When a drive line is pulsed the sense lines which pass through the core on that drive line have an output. The sense lines are connected to sense amplifiers which detect the signals and send them to the comparison logic. (Figure 11). The input address is also sent to the comparison logic. If the address bits compare, no output is delivered to the alarm circuit from the last logic stage.

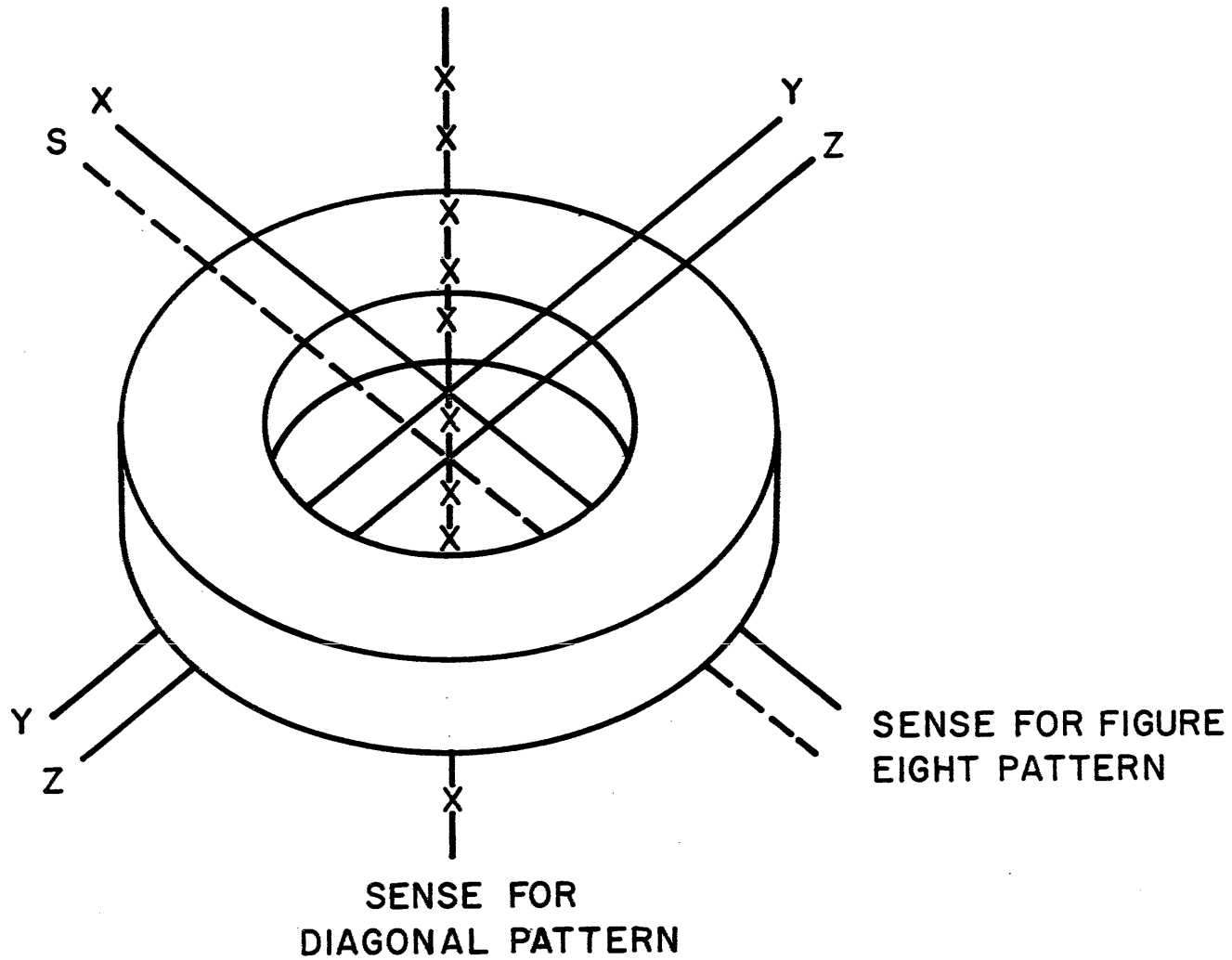
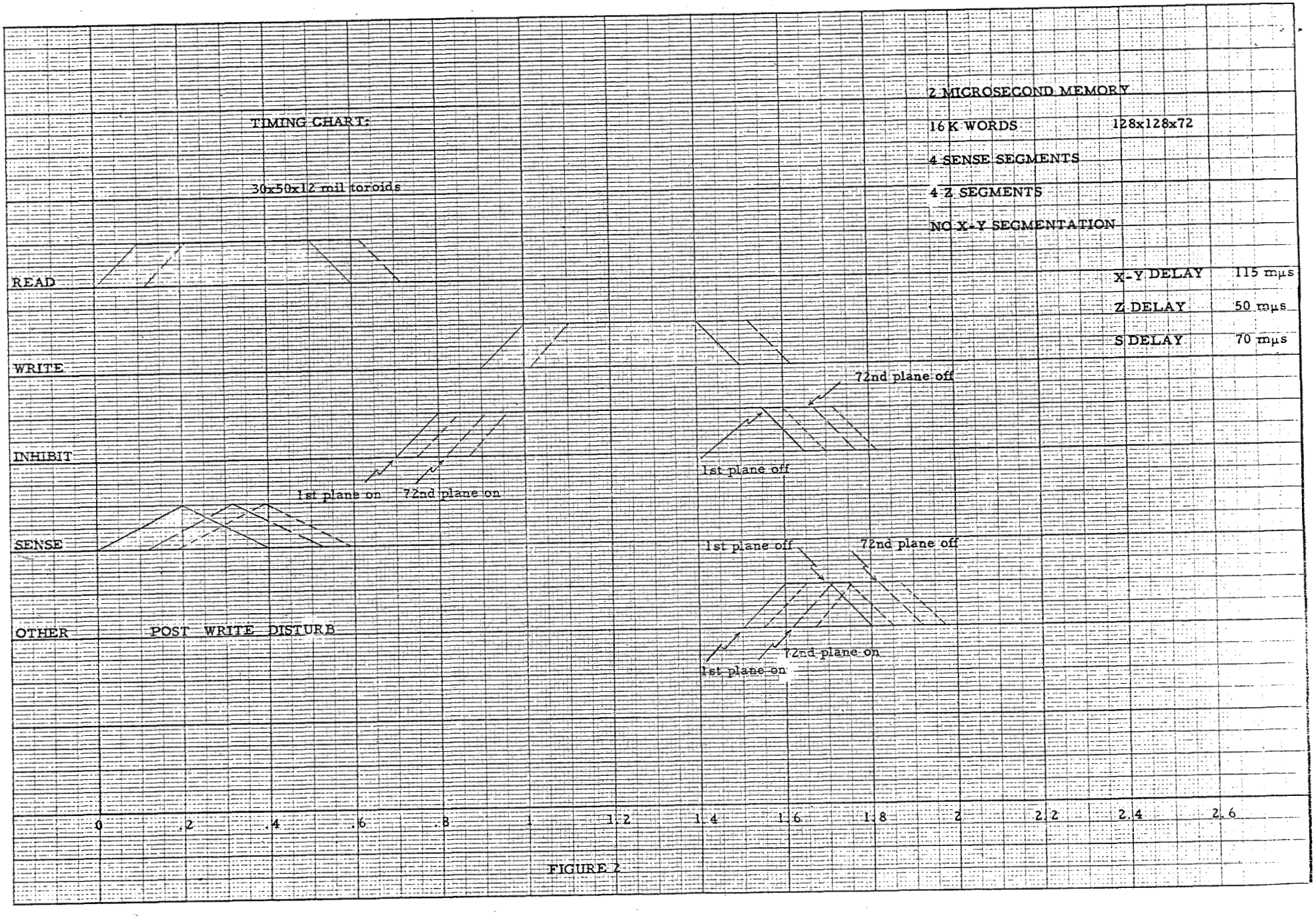


FIGURE I ELEMENT WIRING

TIMING CHART:

30x50x12 mil toroids



2 MICROSECOND MEMORY

16 K WORDS 128x128x72

4 SENSE SEGMENTS

4 Z SEGMENTS

NO X-Y SEGMENTATION

X-Y DELAY	115 mμs
Z DELAY	50 mμs
S DELAY	70 mμs

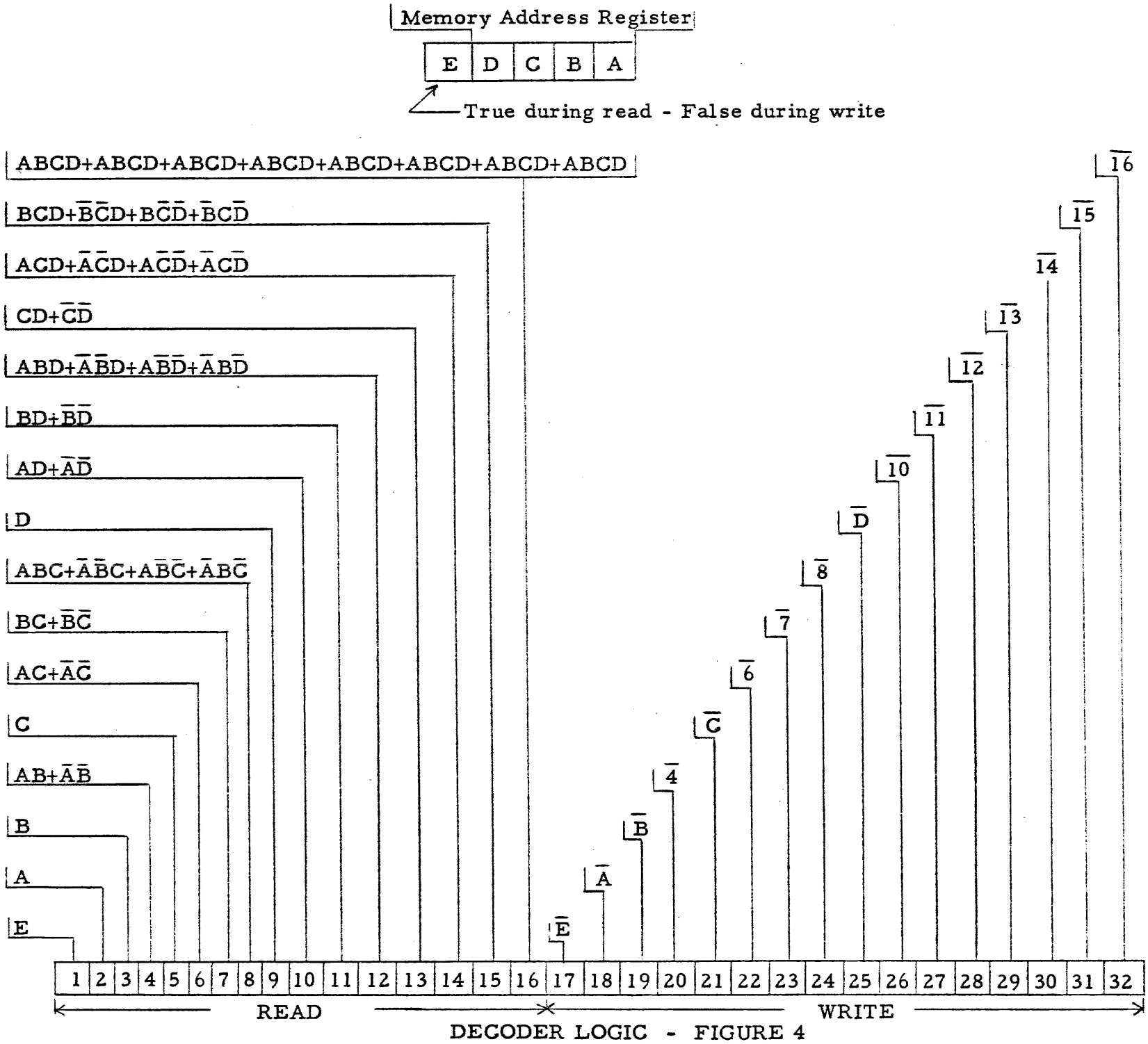
FIGURE 2

INPUTS

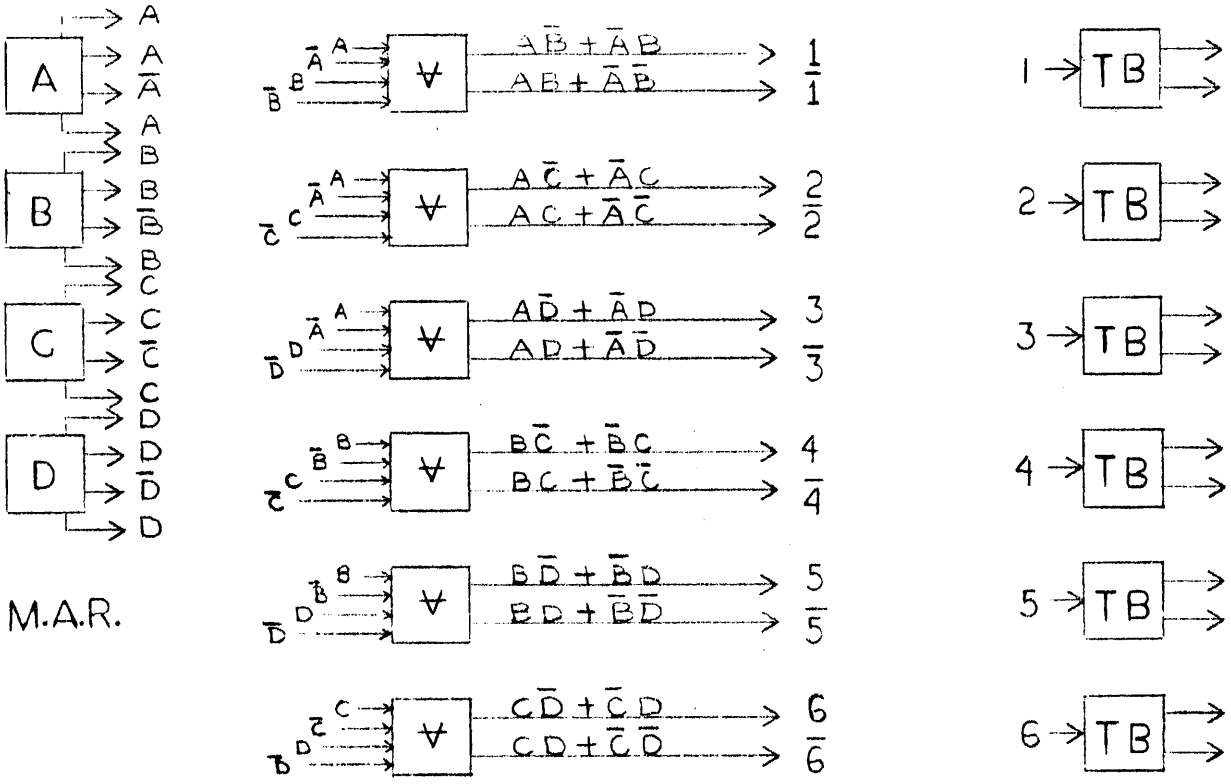
OUTPUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
I	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
II	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
III	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
IV	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
V	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
VI	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1
VII	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
VIII	1	0	0	1	0	1	1	0	1	0	0	1	0	1	1	0
IX	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
X	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1
XI	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1	1
XII	1	0	0	1	1	0	0	1	0	1	1	0	0	1	1	0
XIII	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
XIV	1	0	1	0	0	1	0	1	0	1	0	1	1	0	1	0
XV	1	1	0	0	0	0	1	1	0	0	1	1	1	1	0	0
XVI	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

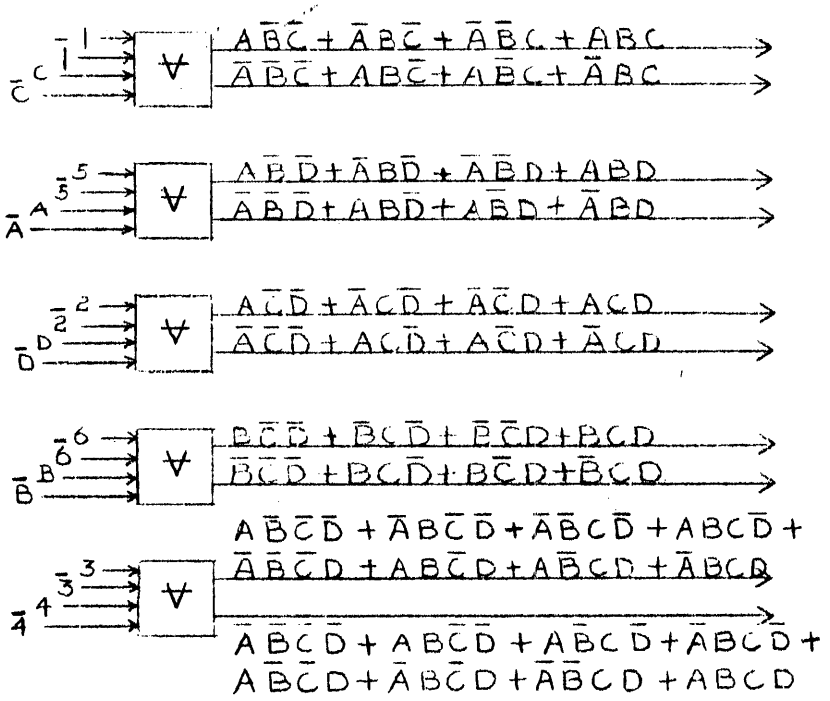
MATRIX SWITCH WINDING PATTERN

Figure 3



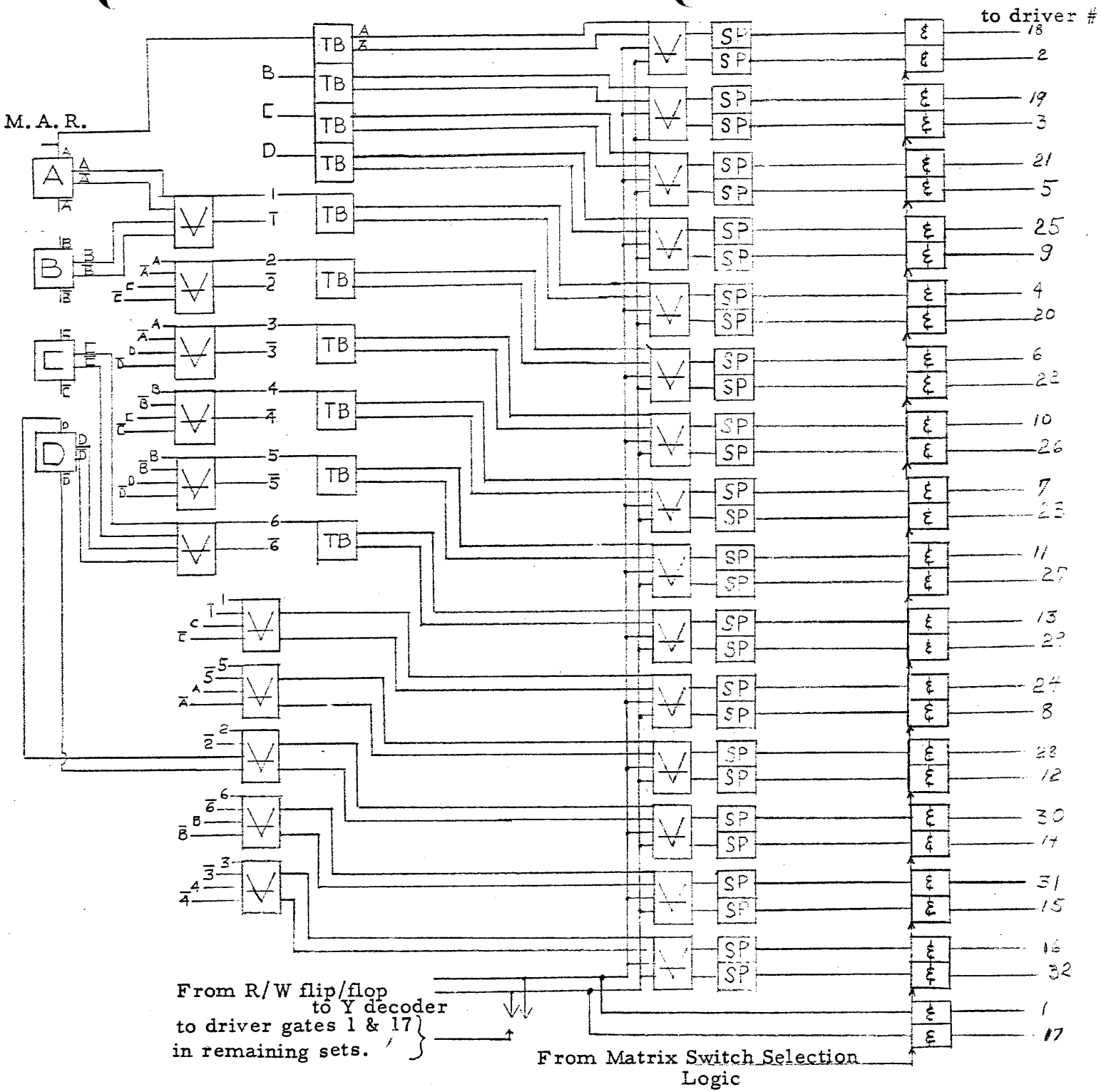
DECODER LOGIC - FIGURE 4





DECODER FOR A 16 OUTPUT MATRIX SWITCH

FIGURE 5

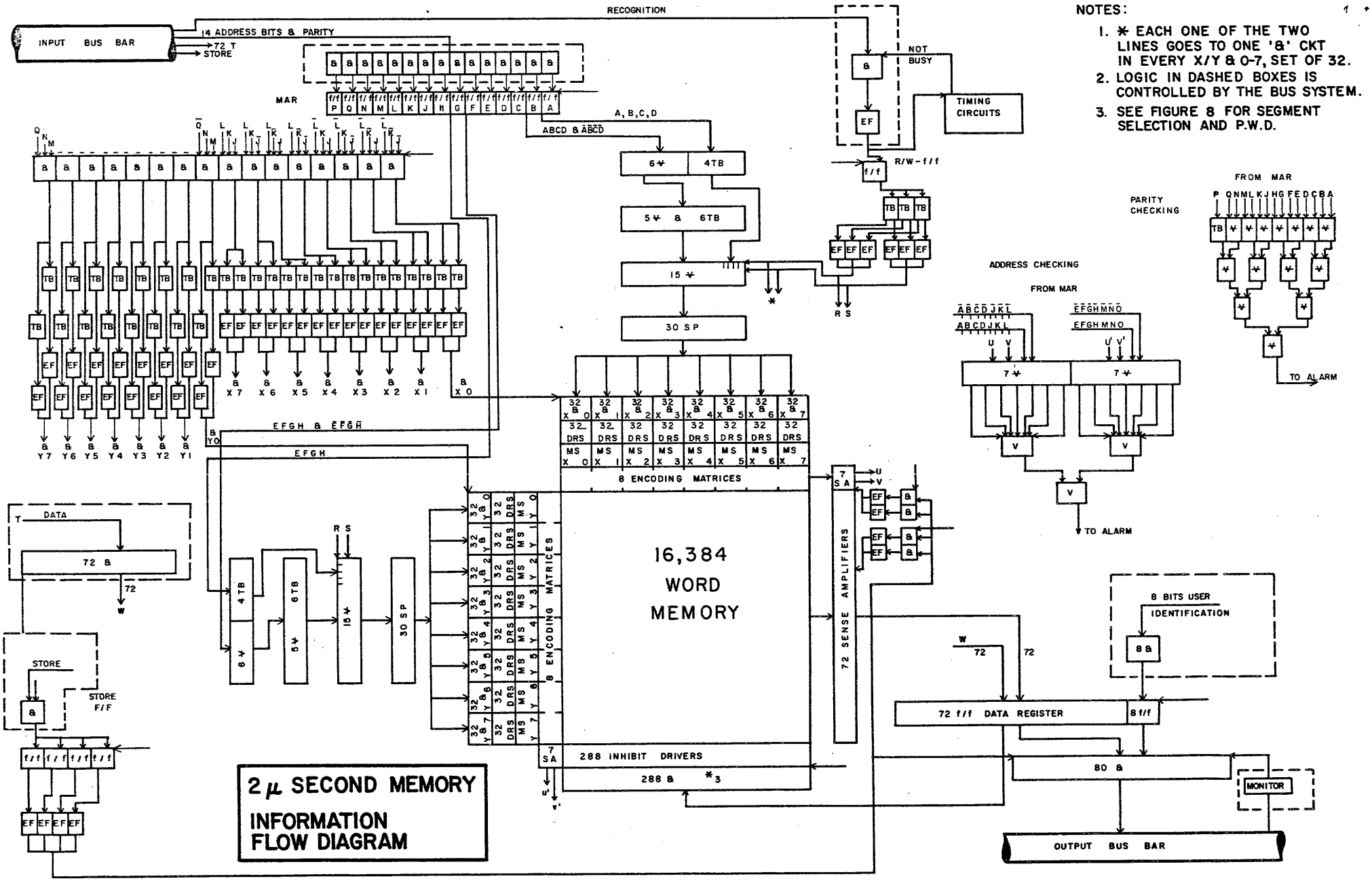


The outputs from SP's also go to the appropriate driver gates in the remaining sets of drivers.

X DECODER LOGIC AND SWITCHING CIRCUITS

FIGURE 6

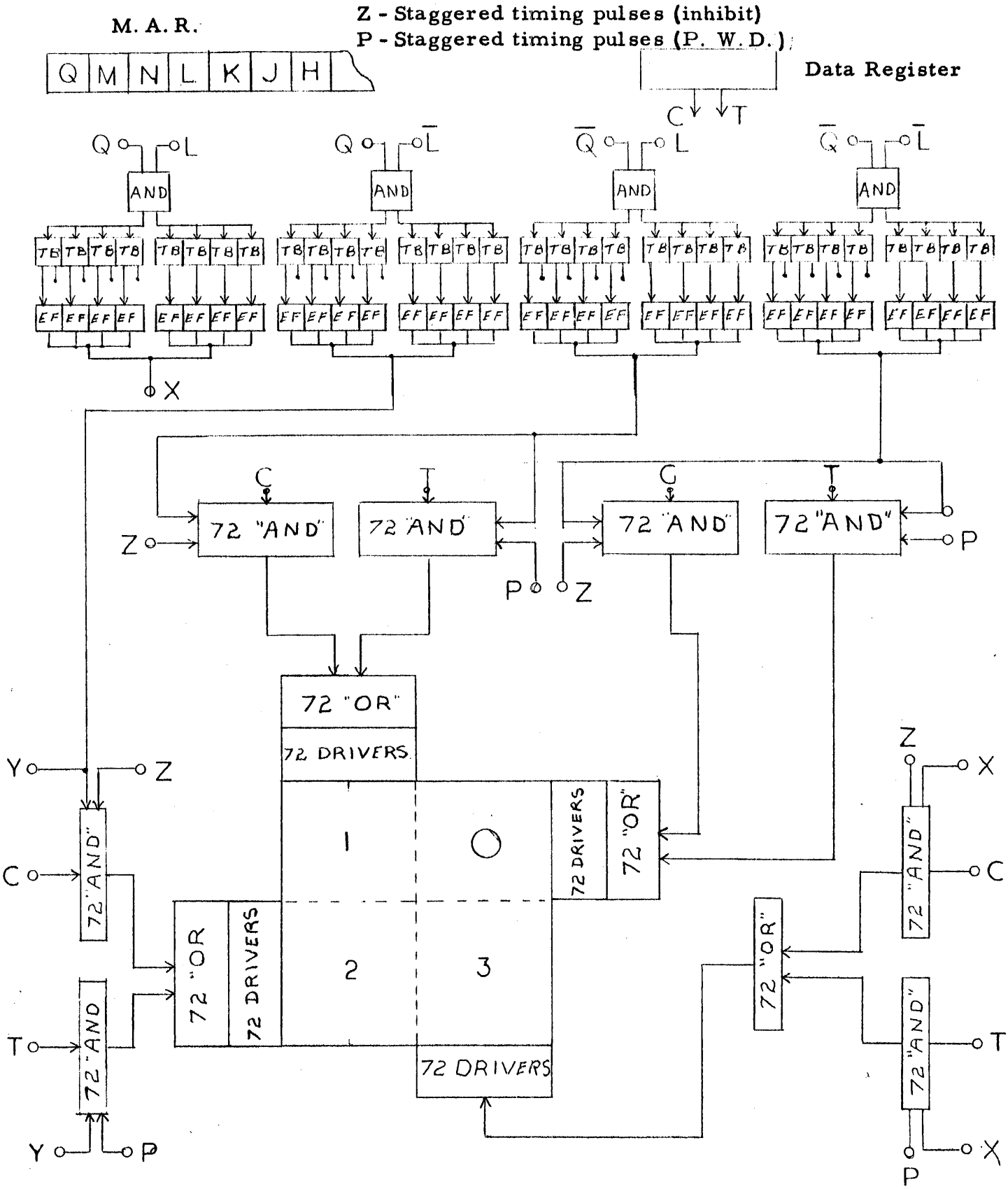
7



NOTES:

1. * EACH ONE OF THE TWO LINES GOES TO ONE '8' CKT IN EVERY X/Y & 0-7, SET OF 32.
2. LOGIC IN DASHED BOXES IS CONTROLLED BY THE BUS SYSTEM.
3. SEE FIGURE 8 FOR SEGMENT SELECTION AND P.W.D.

FIGURE 7



POST-WRITE-DISTURB AND Z SEGMENT SELECTION

FIGURE 8

SENSE LINES: 1, 2, 3 SHOW WHICH OF 8 POSSIBLE MATRIX SWITCHES WAS SELECTED

SENSE LINES: 4,5,6,7 SHOW WHICH OF 16 POSSIBLE OUTPUTS OF THE MATRIX SWITCH, WAS SELECTED

THE OUTPUTS OF THE SENSE AMPLIFIERS, [SA], GO TO ADDRESS COMPARISON LOGIC

EXAMPLE: MS-7, LINE-10 } WAS SELECTED. THE CONTENTS OF THE S.A.'S ARE AS SHOWN

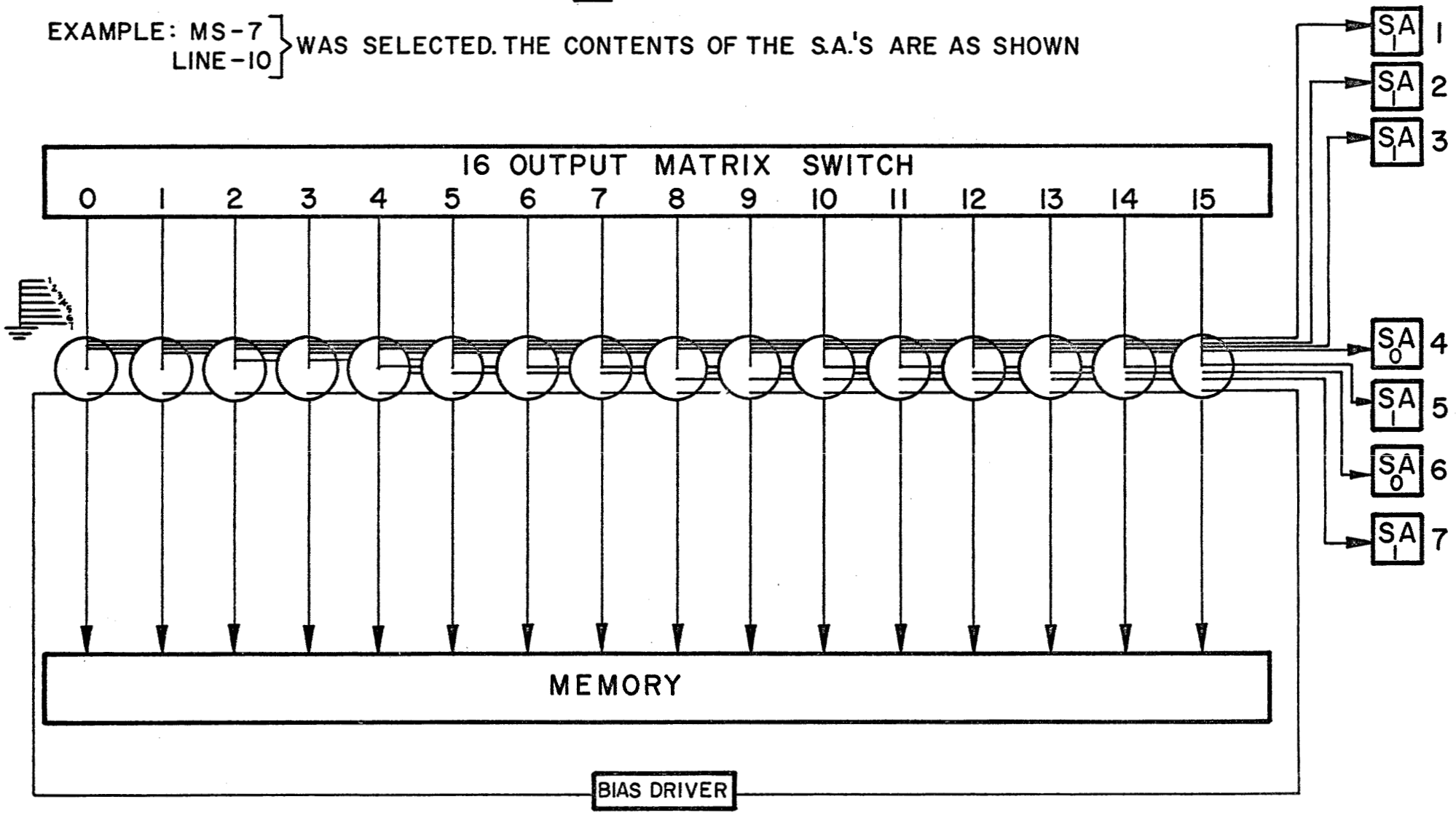
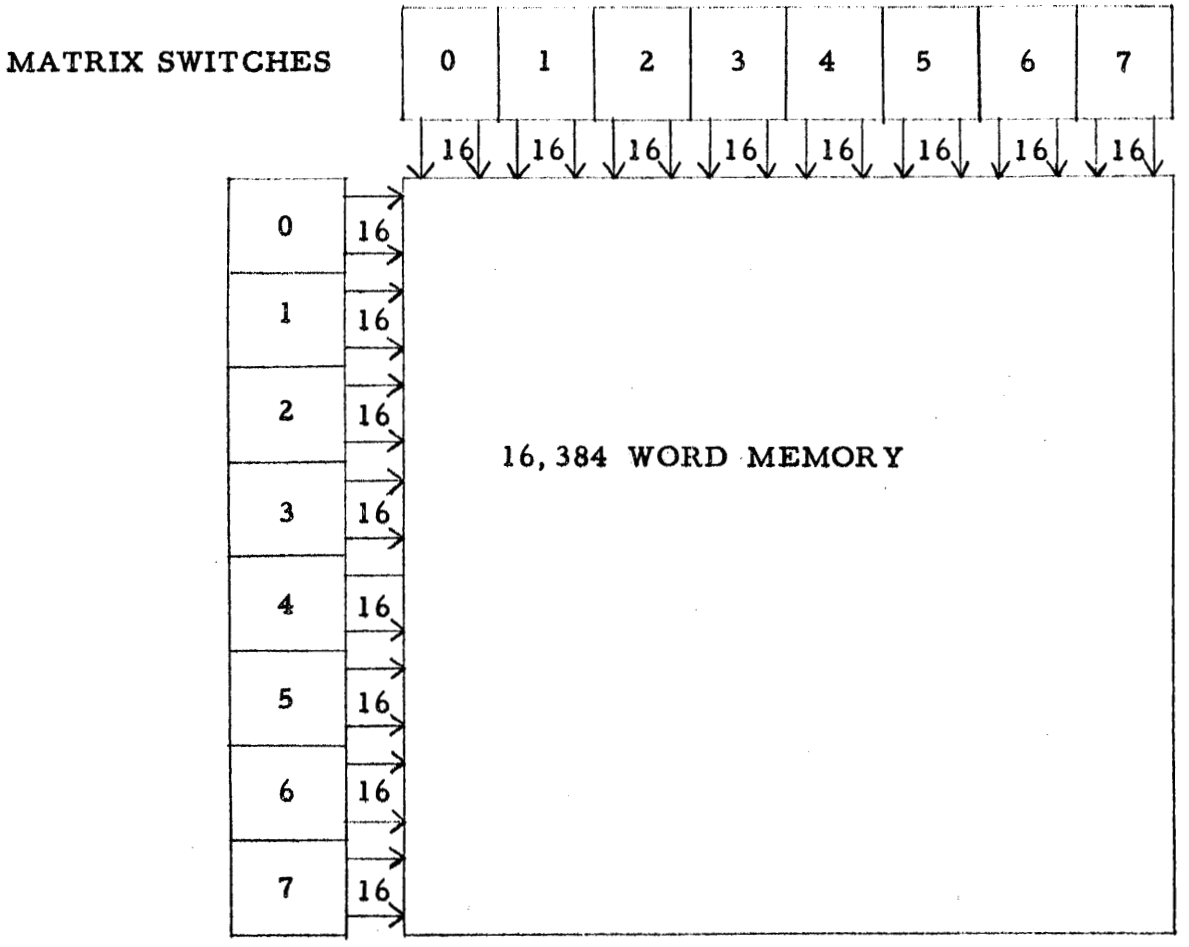


FIGURE 9 ENCODING SCHEME FOR ADDRESS CHECKING



ARRANGEMENT OF MATRIX SWITCHES AROUND A MEMORY ARRAY

FIGURE 10

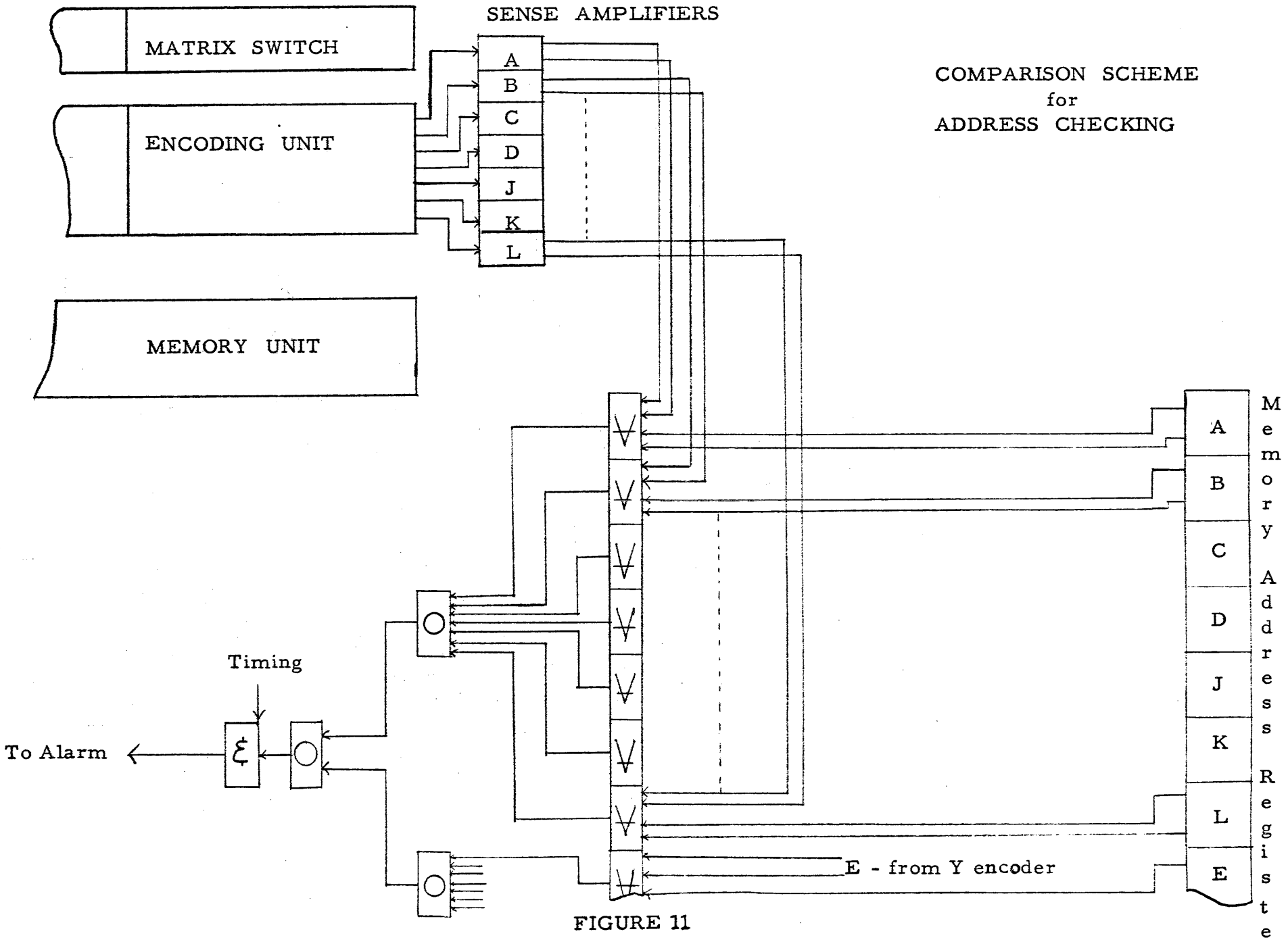

MATRIX SWITCH
ENCODING UNIT
MEMORY UNIT
SENSE AMPLIFIERS
A
B
C
D
J
K
L
COMPARISON SCHEME
for
ADDRESS CHECKING
Timing
To Alarm
E - from Y encoder
Memory Address Register

FIGURE 11