SERIES 7000 CIRCUIT MEMO #27

SUBJECT:

MEMORY CROSS-SECTION

BY:

Edwin D. Councill

Joseph H. Widmar

DATE:

August 30, 1957

ABSTRACT:

Values of characteristic impedance and time delay for the drive lines in the memory must be known in order to design the proper driving circuits. Two model cross-sections, which simulate actual memory conditions, were built so that these measurements could be taken. The results of these measurements are given.

COMPANY CONFIDENTIAL:

This document contains information of a proprietary nature. ALL INFORMATION CON-TAINED HEREIN SHALL BE KEPT IN CONFI-DENCE... No information shall be divulged to persons other than IBM employees authorized in writing by the Department of Engineering or its appointee to receive such information.

MEMORY CROSS-SECTION

Page 1.

CORE PLANE WINDING TECHNIQUES

High-Speed Memory

One proposed system of wiring the high-speed planes is the buttonsewing technique. In this system the cores are placed in counterbored holes in a square piece of phenolic. The wires are hand wired through the cores with the X and Y lines being perpendicular to each other. The Z-wire and bias wires are placed parallel to the X wires. The sense wire is wound in the form of a figure eight, thus ensuring the most effective noise cancellation possible.

Another proposed system is an open-wire technique somewhat resembling that presently employed in the IBM 704 and 705 memories. A picture of a plane wound in this manner is shown in Figure 1. Sketches illustrating the winding pattern are shown in Figure 2.

A third system is a combination of printed wiring and open wiring. The X, Z, and S lines are printed wires while the Y wire and bias wires are of the open wiring technique. Although this printed system was designed for core operation utilizing one wire per hole, the hand wiring of the Y lines and bias windings has made it possible to consider it as a means of wiring the high-speed memory planes.

These three techniques of wiring are explained in greater detail in STM-30.

Medium-Speed Memory

The medium-speed planes are currently being wound in the same manner as the planes found in the IBM 704 and 705 memories. This technique, known as the open wire scheme, has the X and Y lines perpendicular to each other with the Z line wound parallel to the X lines. The sense line is wound diagonally in such a way as to provide for noise cancellation on the sense output. A plane wound in such a manner is shown in Figure 3.

Another method of winding the sense wire is currently under investigation. This method utilizes the figure eight technique of attaining noise cancellation. A more detailed description of this scheme can be found in STM-21. Adaptation of the figure eight sense winding is very likely because of better noise cancellation and ease of winding.

DESCRIPTION

High-Speed Cross-Section

The cross-section of the 512-word high-speed memory is actually a cross-section of a 16x16x24 segment. It contains three completely wired bit plane segments utilizing the button sewing technique of wiring. Three planes were chosen as the minimum number required for determination of cross-talk between adjacent planes. With the exception of a few selected addresses, the cores are untested 3-hole multipath cores of X-8b material. The approximate size of one of these cores is 70x100x15 mils with 20 mil diameter holes.

In order to simulate an actual drive line, 336 additional cores were strung on an X-line, as shown in Figure 5. These cores also have the three bias wires necessary for biased multipath operation. To enable switching of all cores in a word segment (24), one of the Y lines was run through 21 additional cores appropriately spaced on the long X-line.

Medium-Speed Cross-Section

The cross-section for the 16,384-word medium-speed memory contains four completely wired 64x64 bit plane sections wound by the open wire technique. They are located as shown in Figure 4. Three of the four planes are adjacent to permit observation of cross-talk between planes, while the fourth plane is located so as to permit enlargment of a Z segment from 4096 cores to 8192 cores.

With the exception of selected lines, the cores in the cross-section are untested 30x50 mil toroids of high coercive force material. The selected lines in the wired planes contain cores which were tested to meet the specifications necessary for the medium-speed memory.

As shown in Figure 4, 8960 additional cores were strung on parallel lines, 128 to a line, above the wired plane sections in order to simulate an actual drive line in the memory. These cores were tested in order to ensure having cores of high coercive force on the drive line to preclude half-select switching. A Y-line was run through 69 of these additional cores appropriately spaced on the X-line in order to enable switching of all 72 cores in a word.

Two other wires were also placed through these additional cores in order to provide a ground plane.

RESULTS

High-Speed Cross-Section

Since the high-speed transistor drivers were not yet available, the X and Y lines were driven by the vacuum tube current drivers utilizing switch cores. Data were taken on core performance and sense winding signals.

The same address was selected on each of the three planes. The "one" signals obtained varied from 0.26 volts to 0.28 volts, while the "zero" signals varied from 0.08 volts to 0.10 volts. These outputs were measured at the sense wire terminals by use of a differential amplifier. The common-mode noise was measured with the Z-wire driven and not driven. With the Z-wire driven the peak-topeak voltage was 7 volts, while with the Z-wire not driven it was 4 volts.

Values of time delay and characteristic impedance of the drive line and inhibit line were obtained. The characteristic impedance of the X-line was measured as 240 ohms while that of the Z-line was found to be 160 ohms. The time delay was found to be 22 mµs for the Xwire and 20 mµs for the Z-wire. Measurement of characteristic impedance was done by applying pulses of the shape and rise time planned for the memory into one end of a drive line and terminating the other end in a resistance. Matching was obtained by changing this resistance until the input and output waveforms were of the same shape (i.e., minimum reflections occurred on the line). Delay measurements were obtained by noting the transit time of this pulse from input to output.

The values of time delay and characteristic impedance mentioned above are approximate values and are expected to change somewhat when an entire cross-section of 24 completely wired planes is assembled.

Medium-Speed Cross-Section

Characteristic impedance and time delay measurements were taken for this cross-section in much the same way as was done on the high-speed cross-section. The characteristic impedance of the Xline was measured as 200 ohms while that of the Z-line was found to be 150 ohms. The time delay was found to be 110 mµs for the X-wire and 64 mµs for the Z-wire.

Again, as in the high-speed cross-section, these values are approximate and may change when an entire cross-section of 72 completely wired planes is assembled.

CONCLUSIONS

Of the three methods being considered for the high-speed plane winding, the open wiring scheme appears to be most efficient. However, further investigation is currently being carried on in order to get a more detailed picture of the advantages and disadvantages associated with each method.

The medium-speed plane winding will be of the open wire technique with a possible adaptation of the figure eight sense winding.

The figures obtained for delay time and characteristic impedance in both cross-sections indicate that the arrays should be able to be driven and

MEMORY CROSS-SECTION

Page 5.

sensed. As was noted before, these values are approximate and may change when the complete array is assembled. Work is being continued on these cross-sections in order to get more accurate data.



FIGURE 1 - OPEN WIRED HIGH-SPEED PLANE

Page 7.



WIRING PATTERNS FOR OPEN WIRED HIGH-SPEED PLANE

FIGURE 2



FIGURE 3 - OPEN WIRED MEDIUM-SPEED PLANE



FIGURE 4 - MEDIUM-SPEED CROSS SECTION



FIGURE 5 - HIGH-SPEED CROSS SECTION