SERIES 7000 CIRCUIT MEMO #17

SUBJECT: CLEAR MEMORY AND COUNT IN MEMORY

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ABSTRACT: This memo shows how clearing memory may be simulated and how one bit addition is done in a memory system.

I. "CLEAR MEMORY"

At the completion of a statistical problem, it is necessary simultaneously to clear all blocks of memory which were used for counting.

A method for simulating the clearing of memory has been proposed. This method does not actually place "zeroes" in each bit position of the words to be cleared. An extra bit plane per memory unit is required (Figure 1).

The cores in the extra bit plane would be wound as is shown in Figure 2. The difference between the physical winding of a core in the extra bit plane and that of a core in the regular memory array is that one more winding is added (C_x). The electrical difference is that the currents in the C_x and C_y lines pass through the core in the direction opposite to that of a normal inhibit winding.

The normal state of the cores in the clear-memory plane is "one". When the computer sends a signal to clear memory, the clear drivers associated with the clear-memory plane, hereafter referred to as the C-M plane, are selected by the logic shown in Figure 3.

The computer sends the address of the section to be cleared along with a clear memory pulse. The address is set in the address register. The address bits and their complements are sent to AND circuits in the configurations shown. The high order bits (F, E, D) select which of the 8 x 8 sections is to be cleared. The low order bits (A, B, C) select which 8 x 1 section is to be cleared. The outputs of the low order AND's are OR'ed with a clear large section pulse, if an

8 x 8 section is to be cleared, and all the flip-flops are set. The output of the high order AND which is true sets up a flip-flop. The outputs of the flip-flops are gated with a timing pulse through AND circuits and the proper clear drivers are selected. These drivers are turned on and the section of cores which receives full select current from the clear drivers is set to the "zero" state.

When a word location is "read" during a statistical operation, the memory will sense the contents of the C-M core associated with that location. If the content of the core is a "zero", the word will be prevented from being written back into the memory and prevented from being sent to the counter. This is done by the circuitry shown in Figure 4. The core is then put in its "one" state by the write pulse thereby allowing the new data in the word location to be usable information. The time necessary to clear the cores is less than the two complete memory cycles allowed.

II. "COUNT IN MEMORY"

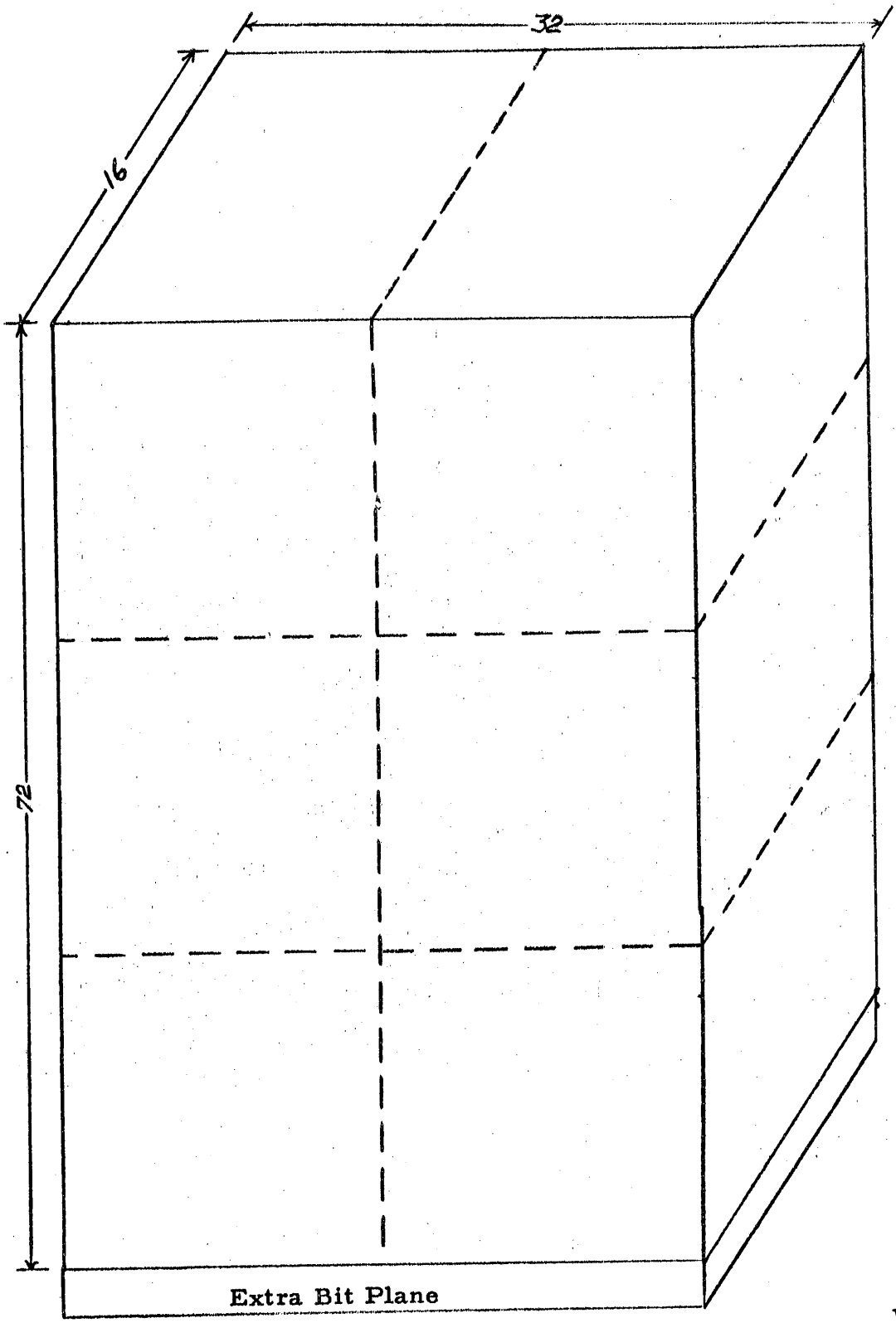
The count in memory has the following specifications:

1. Be able to add 1 into any bit position of 64 bits.
2. Have a variable carry size.
3. Trigger the timing circuits to start the "write" pulse when the carry is complete.
4. Indicate overflow, if the carry goes beyond its specified positions.

Figure 4 shows the logic necessary to send the data to the counter and prevent the storing of information before the counting is done in a counting cycle. If the cycle is not a counting one, the memory performs as a regular memory. That is, it either regenerates, or stores new data, depending upon the type of cycle the memory is in.

A block diagram of the counter is shown in Figure 5. The "dashed" sections shown in Figure 5 are the ones added for count in memory. The circled number above each section is the transistor count for that particular section. The total transistor count, for clearing and counting in memory is 5550. This includes controls to establish counter size.

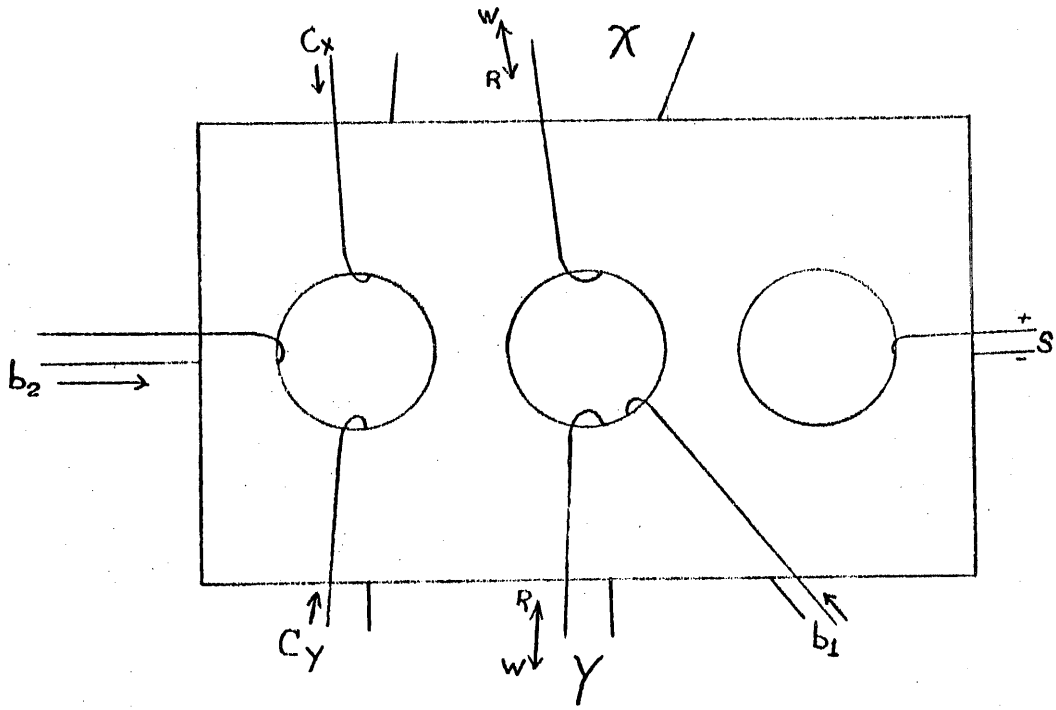
The augend is supplied from register A and the addend from register B. The contents of A and B are summed and the carry is generated in the adder. The carry circuit is monitored to determine when the carry is completed.



512 Word Memory With the Extra Bit Plane for Clearing Memory

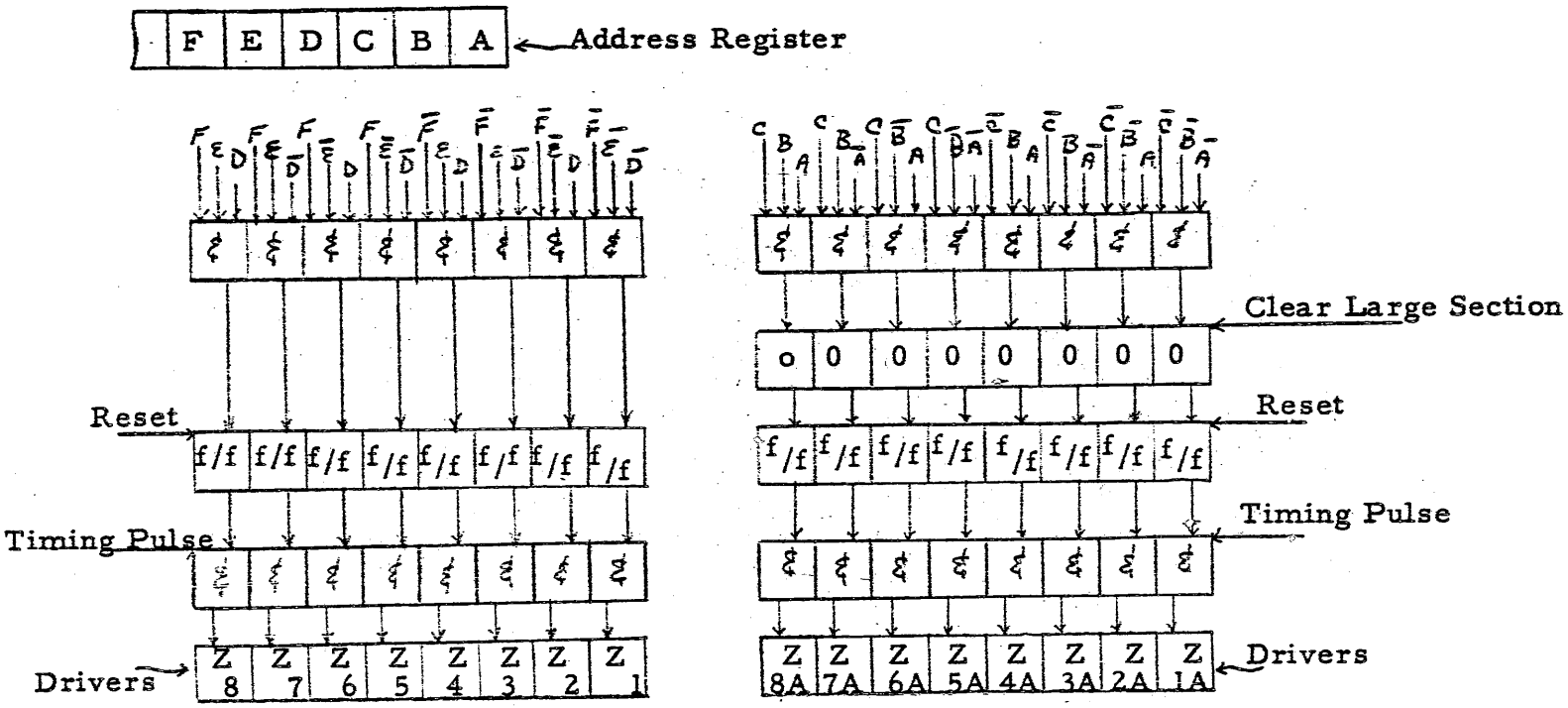
Figure 1

A Possible Element For The "Clear Memory" Plane



All currents 1 amp except b_2 which is 2 amps.

Figure 2



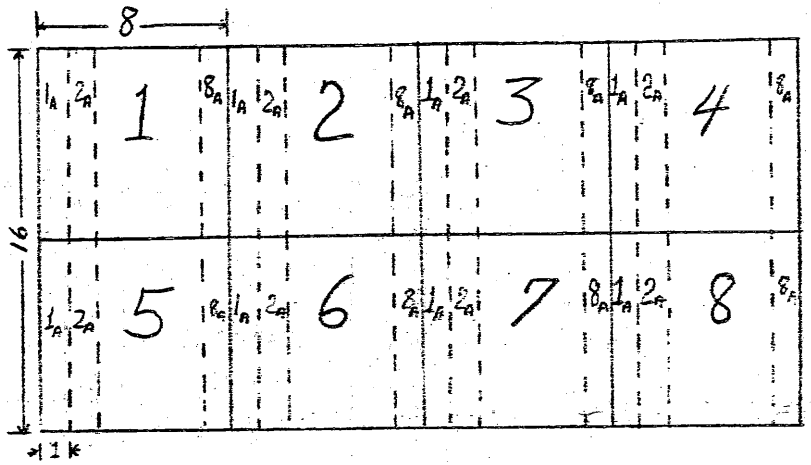
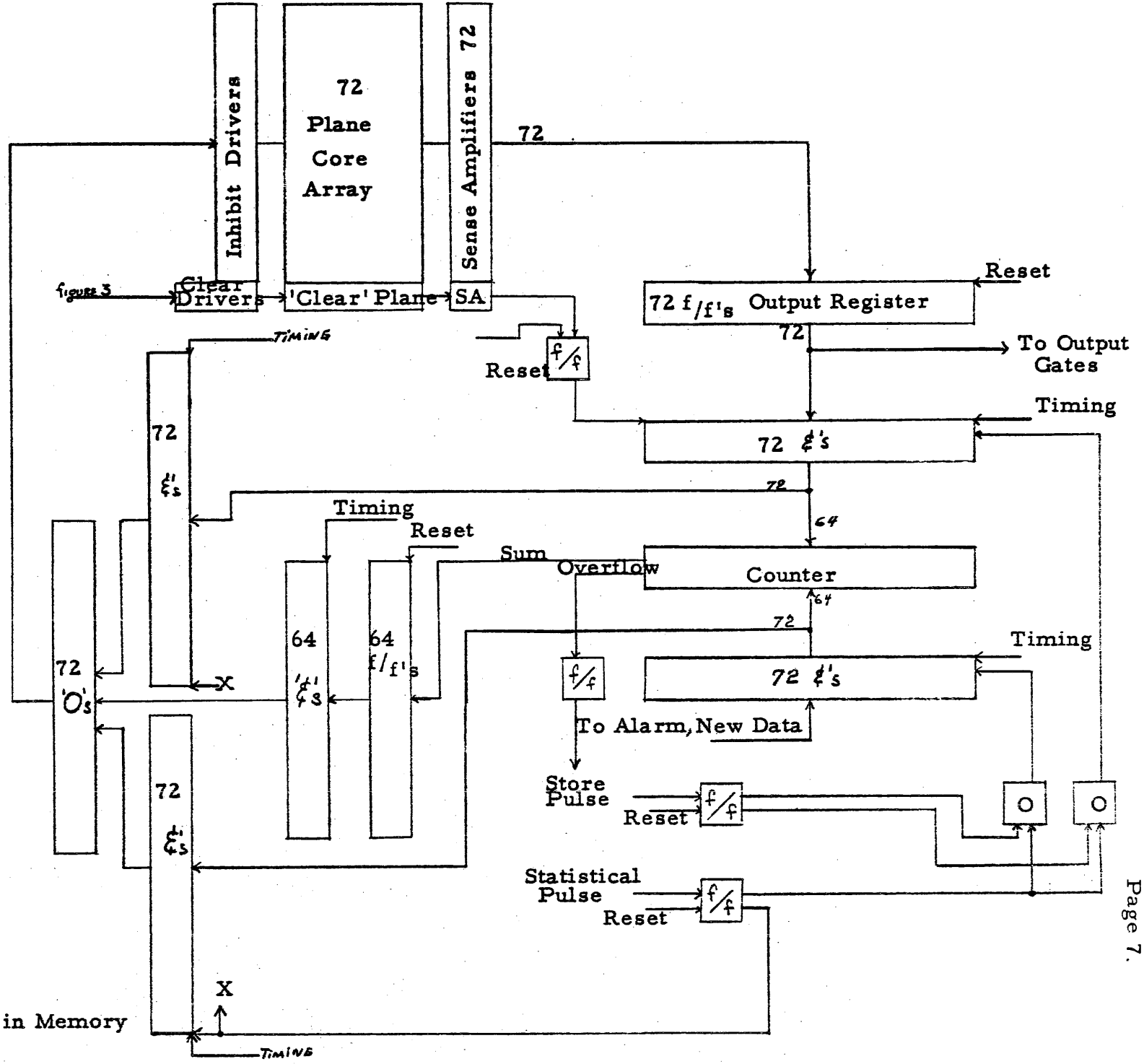


Figure 3

Clear Memory Logic
For 0.5 μsec Memory



Logic for Counting in Memory

Figure 4

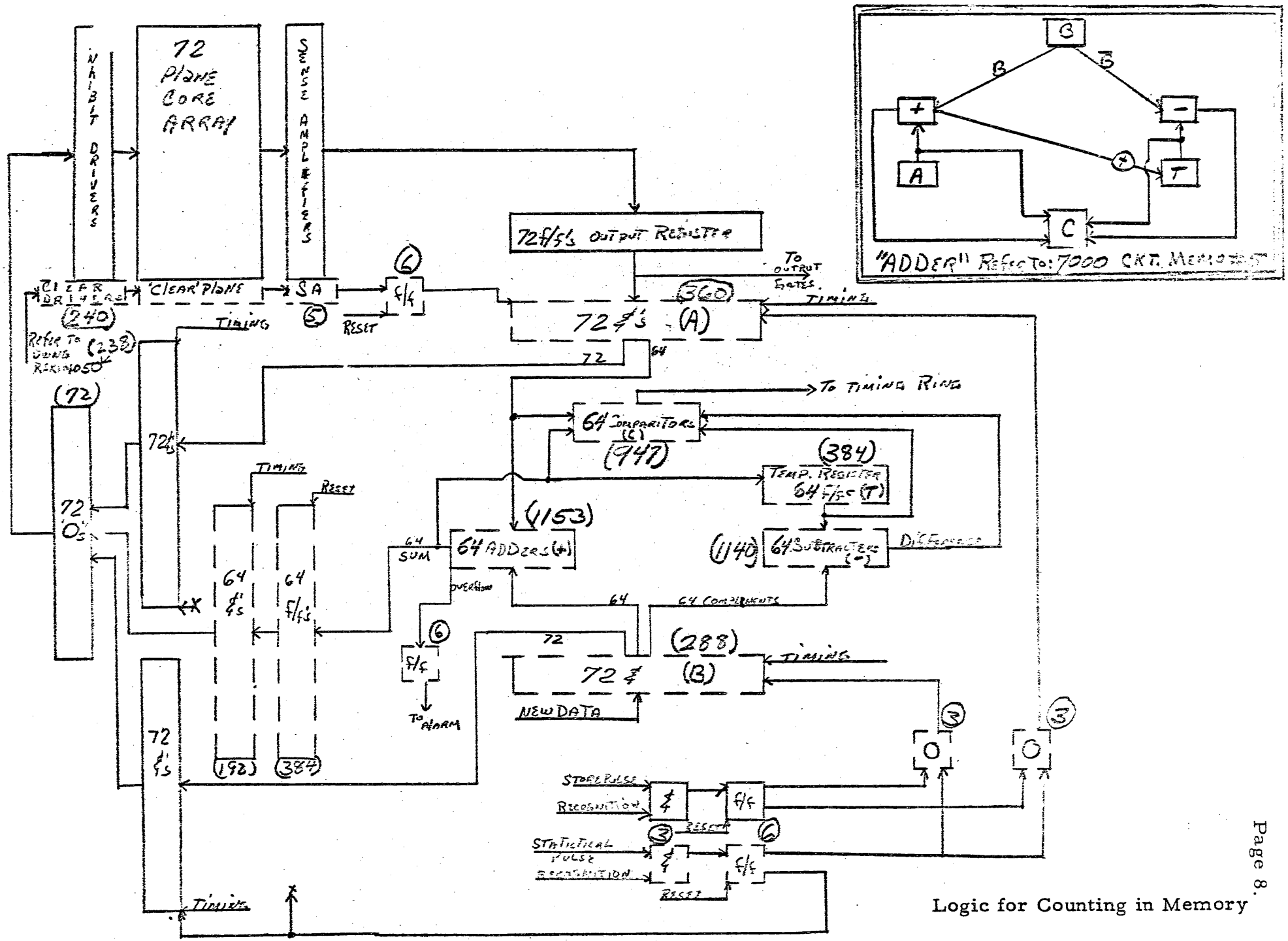


Figure 5

Logic for Counting in Memory