SERIES 7000 CIRCUIT MEMO #16

SUBJECT: ADDRESS CHECKING IN THE 512-WORD CORE MEMORY

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DATE: June 27, 1957

ABSTRACT: This report shows the encoding unit which will be used to produce the decoded address for comparison with the input address and the logic used for comparison.

This memo shows how an encoding matrix of magnetic cores, through which the memory drive lines pass, supplies the address of the selected drive line for a comparison with the input memory address.

Figure 1 shows a segmented 512-word memory. On the outputs of each of the twelve matrix switches is connected an encoding matrix (Figure 2). Sense line A indicates which of the two matrix switches (0 or 1, or L or R) were selected. Sense lines B, C, D, and E are used to supply the address of the output of the matrix switch which was selected. An example of this is:

> Suppose matrix switch "0" output "13" was selected. The configuration in the memory address register for this section would be

E	D	C	B	A
1	1	0	1	0

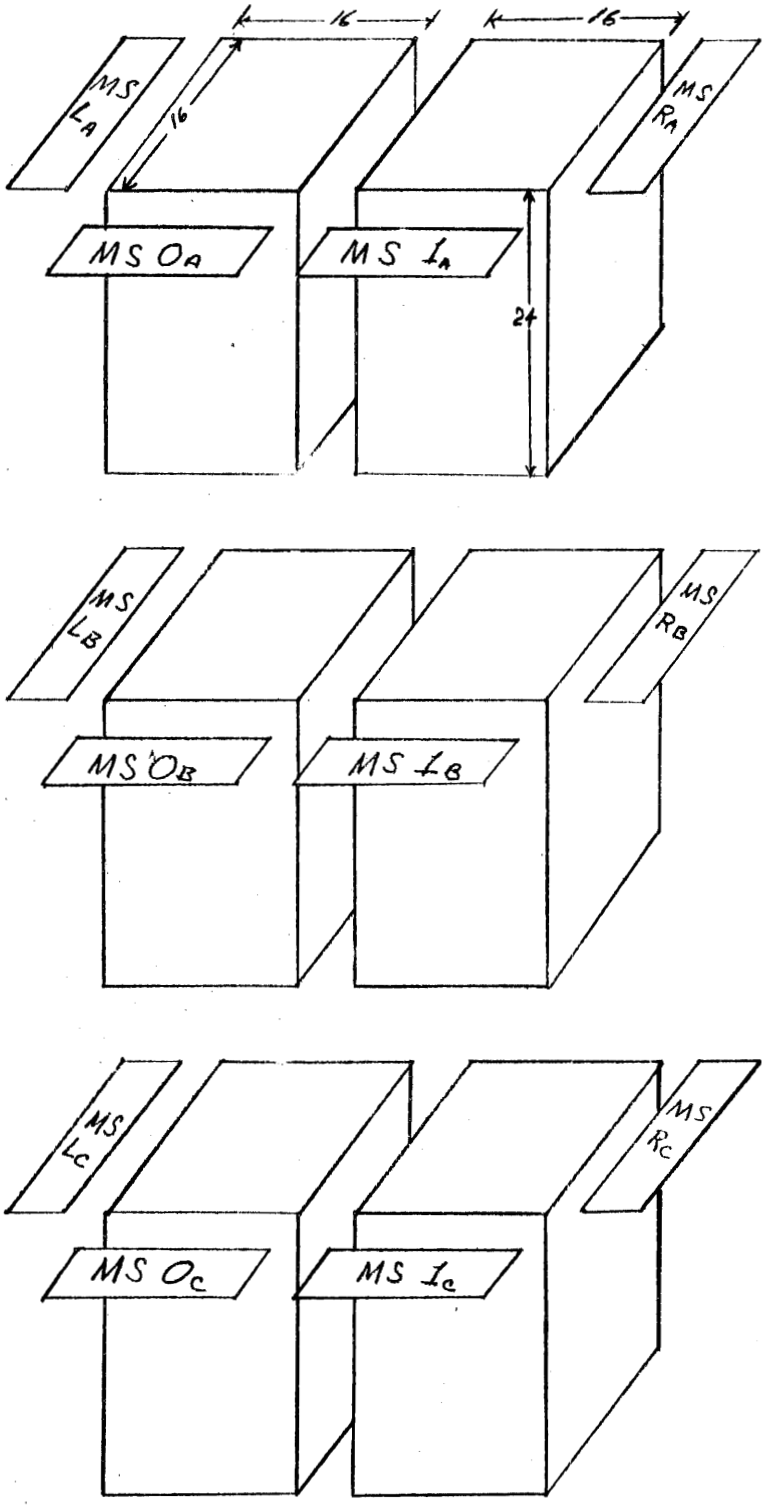
> and the output of the sense lines in the encoding unit would be

E	D	C	B	A
1	1	0	1	0

The outputs from the sense amplifiers connected to the sense lines of the encoding unit are sent tc the comparison logic (Figure 3) to be compared with the input address.

Line X passes through two encoding units but in opposite directions. For instance this line would pass through the encoding units attached to MS-L_A and MS-O_A so that if both of these matrix switches are selected there will be no output on line X due to signal cancellation. If only one matrix is selected, there would be an output on line X and a signal would be sent to the alarm circuit.

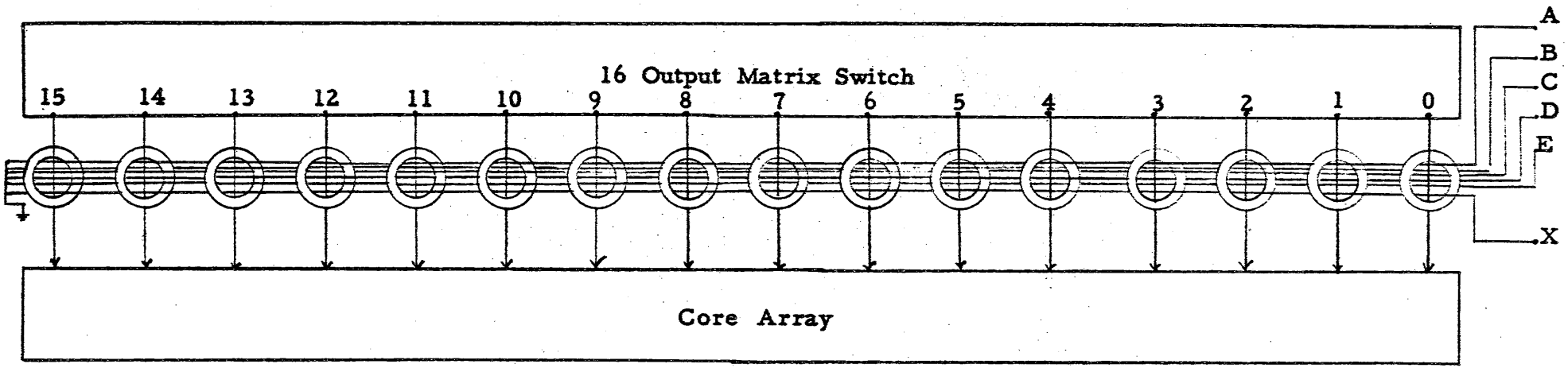
The outputs of each set of three encoding units (for example) the encoding units attached to matrix switches L_A, L_B, and L_C) are compared for similarity. Figure 4 shows one of the groups of matrix switches with its associated encoding units and the logic necessary to determine if the outputs of the three matrix switches were the same. The logic shown is for one sense line. The logic for the other sense lines would be the same. If the outputs from all the matrix switches compare, the alarm circuit receives no signal. The number of transistors needed to do complete address checking is 574.



MS = 16 Output Matrix Switch

Figure 1
Segmented 512-Word Memory

Encoding Unit For Address Checking



Line A shows which of two possible matrix switches were selected.
Lines B, C, D, and E show which of 16 possible outputs were selected.
Line X is used to detect if more than two or less than two matrix switches were selected.

A bias line is also run through the encoding matrix. This is not shown.

Figure 2

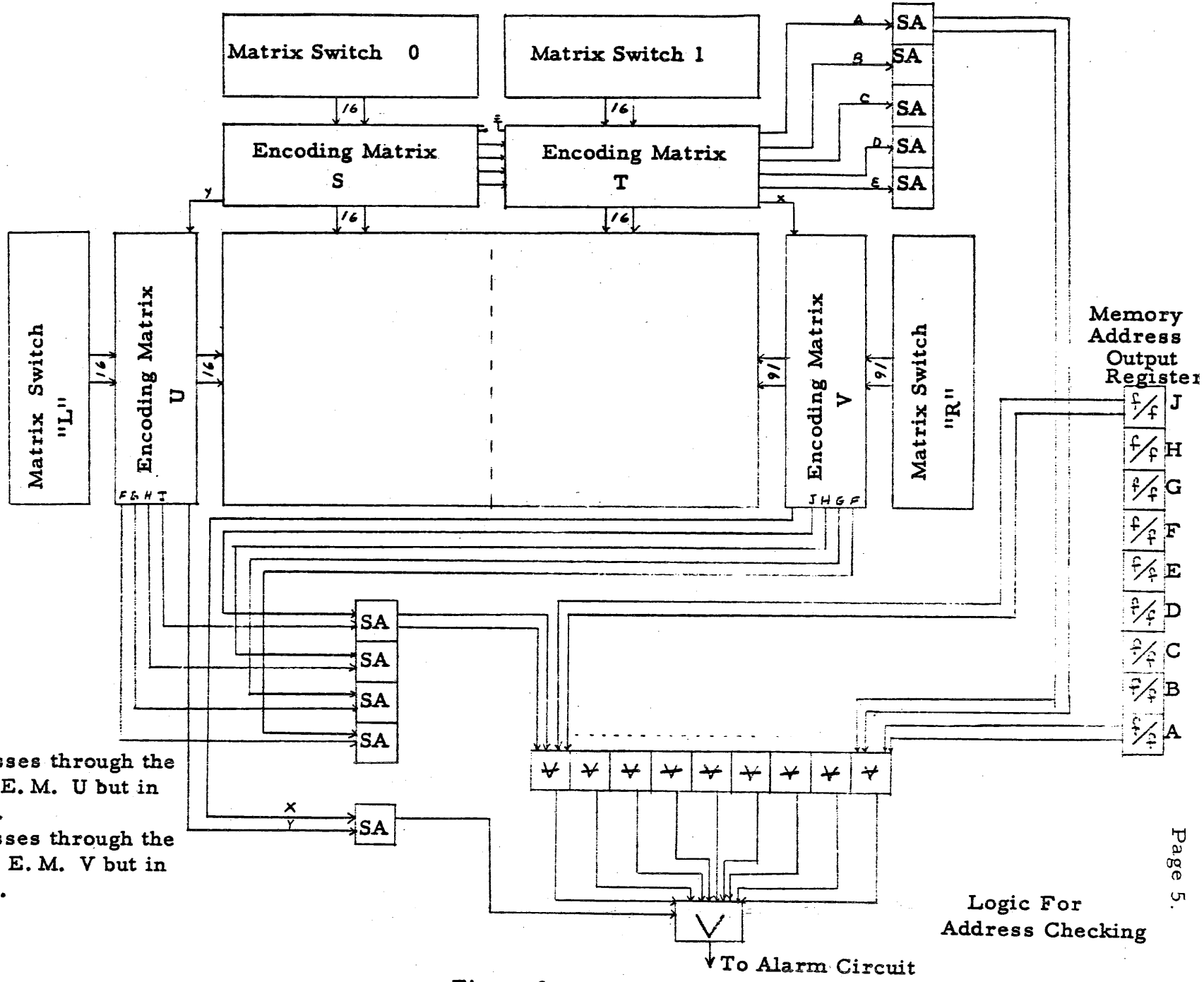

Matrix Switch 0
Matrix Switch 1
Encoding Matrix S
Encoding Matrix T
Encoding Matrix U
Encoding Matrix V
Matrix Switch "L"
Matrix Switch "R"
SA
Memory Address Output Register
Logic For Address Checking
To Alarm Circuit
Sense Line "Y" passes through the cores in E. M. S & E. M. U but in opposite directions.
Sense Line "X" passes through the cores in E. M. T & E. M. V but in opposite directions.

Figure 3

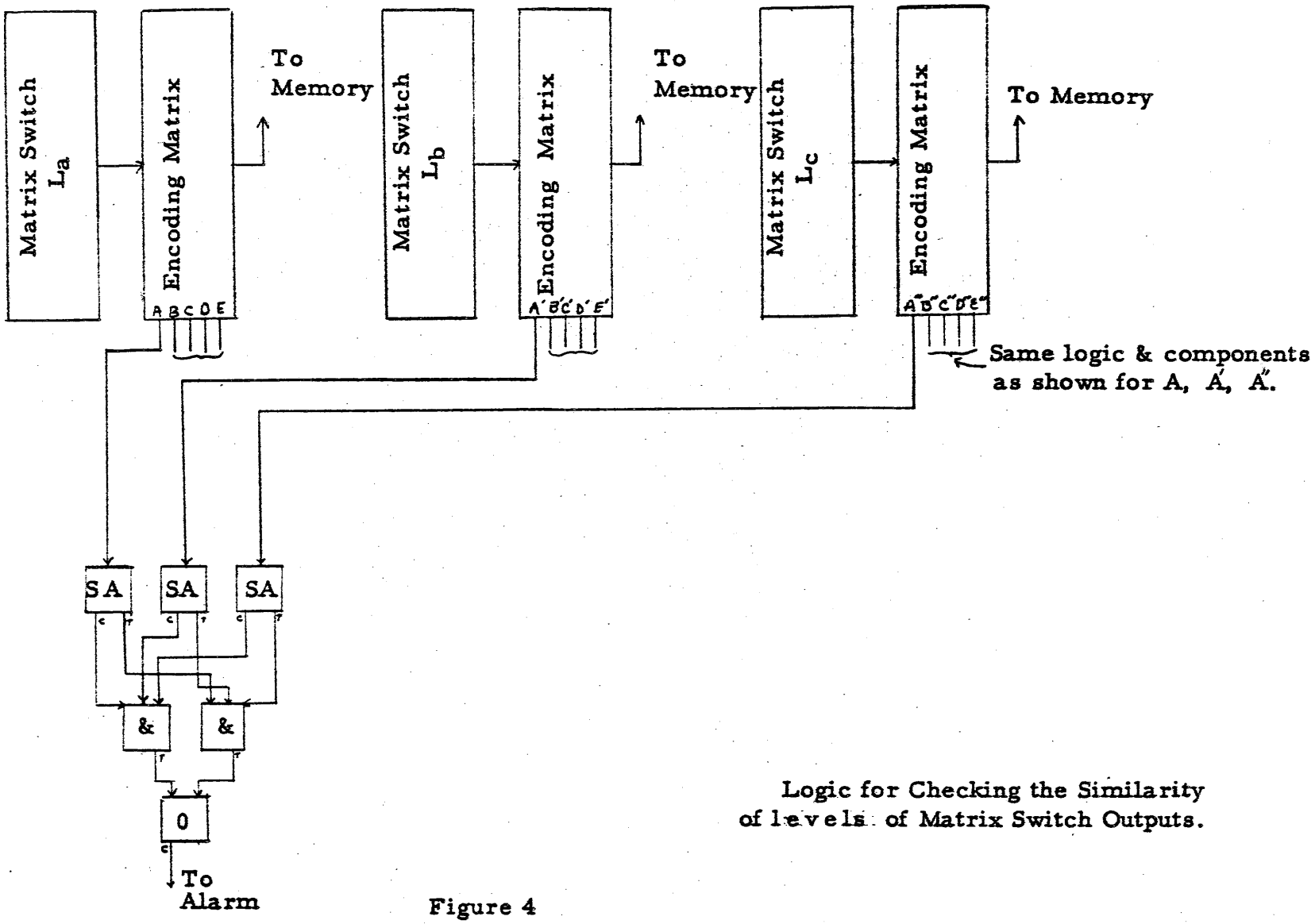


Figure 4

Logic for Checking the Similarity of levels of Matrix Switch Outputs.