SERIES 7000 CIRCUIT MEMO #15

SUBJECT: A Method For Clearing Blocks In Memory

BY: J. J. Mackson

DATE: July 1, 1957

REFERENCE:

Series 7000 Circuit Memo #17
June 27, 1957 by R. J. Flaherty and R. C. Lamy

ABSTRACT: By the addition of a clear memory plane to a memory array, it is possible to simulate the clearing of certain sections in memory for a counting operation. Putting a zero or a one in a core of the clear memory plane, indicates whether a word is cleared or has information stored in it.

Product Development Laboratory

International Business Machines Corporation

Poughkeepsie, New York

Because there is a need to clear certain blocks in memory, the following scheme of logically clearing memory was investigated. Other schemes had been proposed before, but they showed requirements that increased both driving and wiring problems.

This scheme for clearing was proposed in the referenced memo. The 3-hole cores which are to be used to clear blocks in memory will be wired in what will be known as the clear memory plane. Therefore, the clear memory plane will be the 73rd plane; the other 72 planes will comprise the 72 bits for the different words in memory.

To see if such a system was possible, one 3-hole core of X-8 material was wired as shown in Figure I.

Putting on the two bias drivers and the X and Y drivers gave the customary read one, write one cycle. The functions of the C_y and C_x are to clear the core, that is switch it to the zero state. Then when the next read-write cycle comes along, there will be a zero read and a one written instead of a one read and a one written. Both C_x and C_y must be turned on at the same time to clear the core. To see if the core had actually cleared, a program was set up. Five timing points were used. These timing points were spaced 10 μsec apart. (See Figure II).

When the X and Y drivers were turned on, the core operated in the conventional manner, reading and writing a one. In addition to putting on the X and Y drivers, the C_x and C_y drivers were turned on. The output from the core was similar to that shown in Figure II namely read one, write one, clear, read zero, and write one. It is important to have the bias drivers on in order to clear the core.

Having cleared one core, a 4 x 4 plane was assembled. This 4 x 4 plane was built to show that a block in memory can be cleared. Then once cleared, one or more words of the clear block or column can be used for counting. Only one word will be used at one time in a counting operation. The program used in determing if a block of 4, 8, or 16 words is cleared

is the same as that used to clear the one 3-hole core.

The bias was wound in such a way that one bias driver was used to supply 2 amp turns through one leg of the core and 1 amp turn through the other leg. (See Figure III)

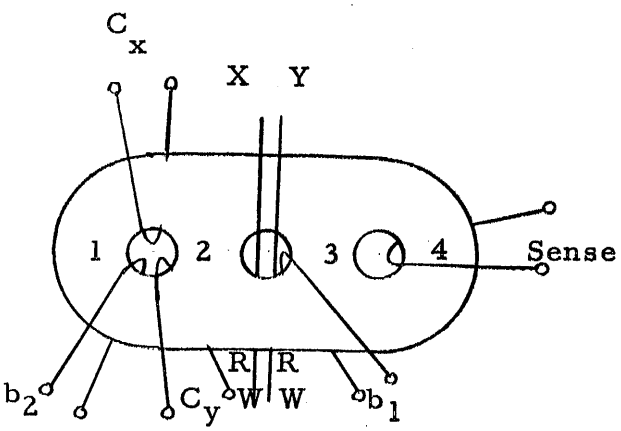
Having cleared a block in memory, all drivers are turned off, leaving the cores in the cleared memory section of the clear memory plane in the zero state.

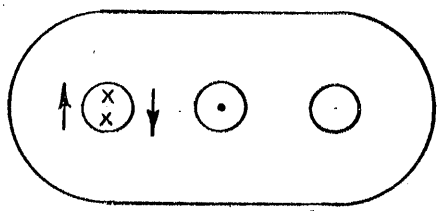
The cores of the 73rd plane in the cleared memory section can be selected for a counting operation by turning on their respective X and Y drivers. No matter what core is selected, initially a zero is read and a one is written in a core of the clear memory plane. The clear memory plane only indicates if a word in memory is cleared. A core in the one state in the clear memory plane indicates information is stored in the word it represents. A zero stored in a core of the clear memory plane, indicates that nothing is stored in that particular 72 bit word. Figures 4a, b, c, show 4, 8, and 16 cores being cleared, respectively. Figure 4d shows the one to zero ratio of a clear pulse for one core after 16 cores have been cleared.

That an individual core can be cleared substantiates that the wiring and drive currents proposed for the clear memory core are feasible. Also, by clearing one, four, eight, or sixteen cores of the 16 core clear memory plane, further substantiates that such a system could be used to clear columns or blocks in memory.

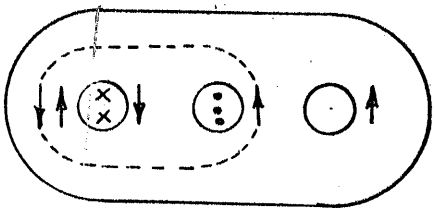
The wiring scheme used in this 16 core clear memory plane is included at the end of this report as Figures 5, 6, 7, 8, & 9.

If it is desired to go ahead and build a 16 x 16-core clear memory plane, the principles of operation described here may be followed.

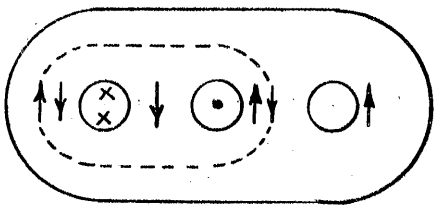




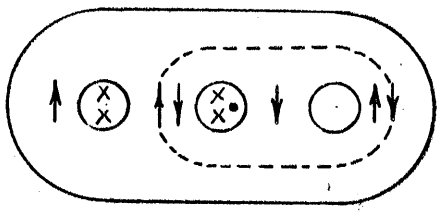
Bias Applied



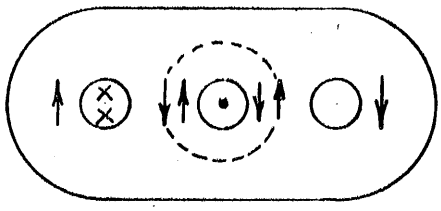
Read One



Bias Switch Back



Write One



Bias Switch Back

Figure 1

Symbolism: X = current into hole
• = current out of hole

This is how a 3-hole clear-memory-plane core will be wired. Its operation is very similiar to the operation of the cores in the other 72 planes.

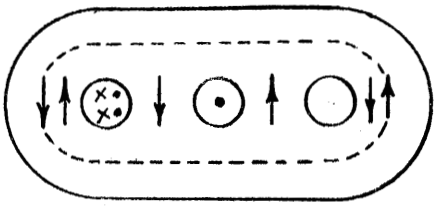
The Theory behind its operation is as follows: Assuming a demagnetized core is used. Applying 2 amp-turns of D. C. bias into the 1st hole of the core and 1 amp-turns D. C. bias out of the middle hole of the core, will saturate legs 1 and 2.

Applying 2 amp-turns of read drive out of the middle hole, the core will switch flux in the manner shown. Leg 1 will flip over, legs 3 and 4 which were initially demagnetized will be saturated inorder to offset the change in leg 1.

Upon removal of read drive, there is no flux change in leg 4 due to bias switch back.

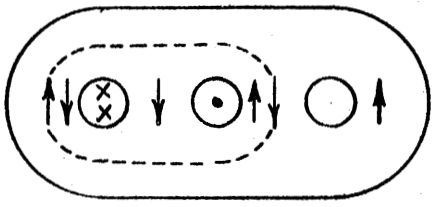
Applying 2 amp-turns of write drive into the middle hole, leg 4 will flip over, due to the change in flux as shown.

Upon removal of write drive, there is no flux change in leg 4, due to bias switch back.



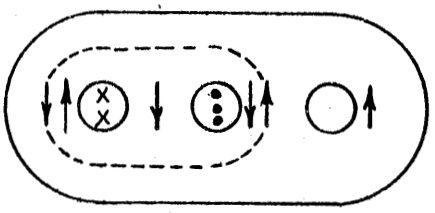
Clear

Applying 2 amp-turns from C_x and C_y drivers out of the first hole, leg 4 will flip over showing the core is cleared.



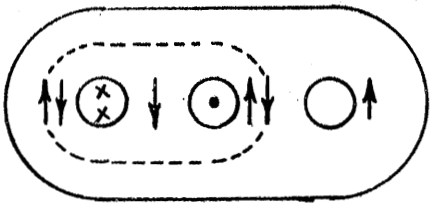
Bias Switch Back

Upon removal of C_x and C_y drivers, there is no flux change in leg 4 due to bias switch back.



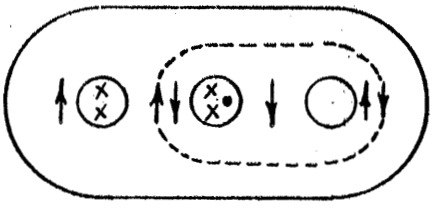
Read Zero

Applying 2 amp-turns read drive out of the middle hole, leg 4 will not flip over, showing a zero is read.



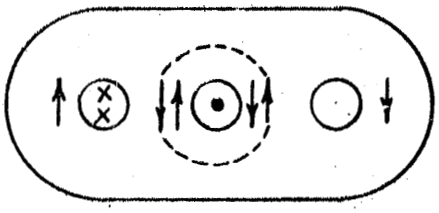
Bias Switch Back

Upon removal of read drive, there is no flux change in leg 4 due to bias switch back.



Write One

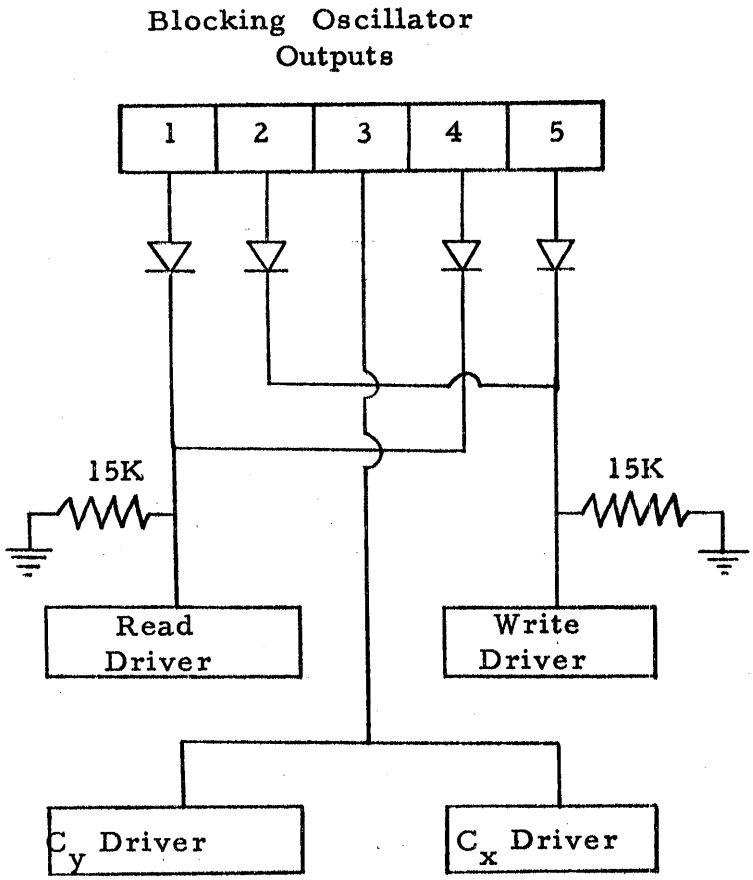
Apply 2 amp-turns write drive into the middle hole, leg 4 will flip over, showing a one is written for the next count operation.



Bias Switch Back

Upon removal of write drive, there is no flux change in leg 4 due to bias switch back.

This operation is repetitive.



Read Driver = 2d
Write Driver = 2d
C_y Driver = d
C_x Driver = d
b_2 = 2d D.C.
b_1 = d D.C.

where d is the net half-select drive current
For this case, d = 1 amp-turn

Program:

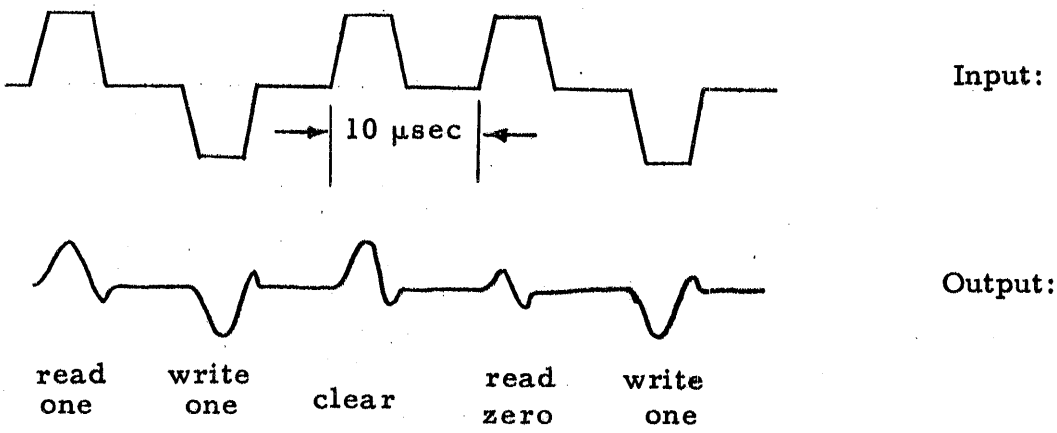


Figure 2

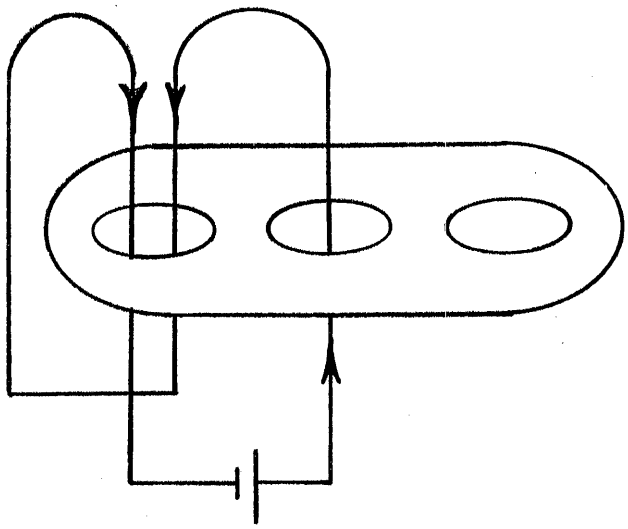
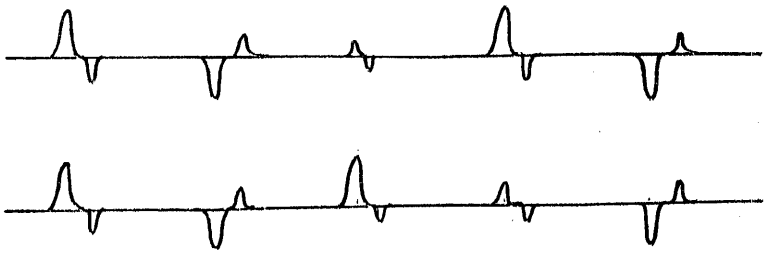


Figure 3

Bias Winding Scheme

R = Read
W = Write
C = Clear

Program:

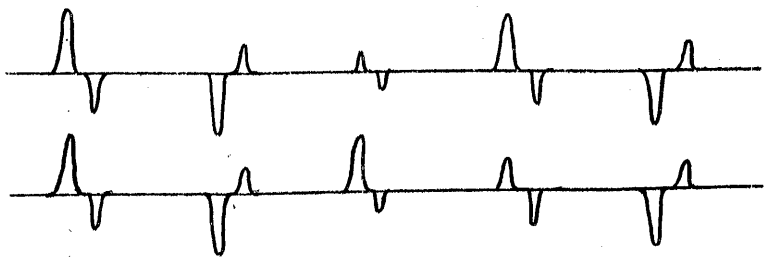


R	W	1/2C	R	W

4 Cores Cleared

R	W	C	R	W

Figure 4a

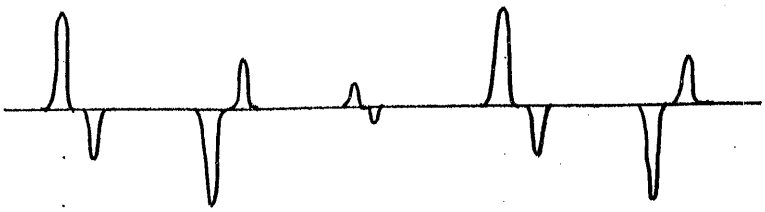


R	W	1/2C	R	W

8 Cores Cleared

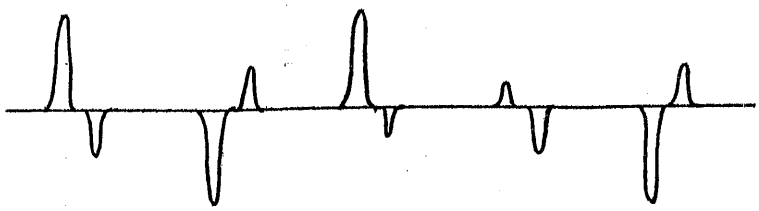
R	W	C	R	W

Figure 4b



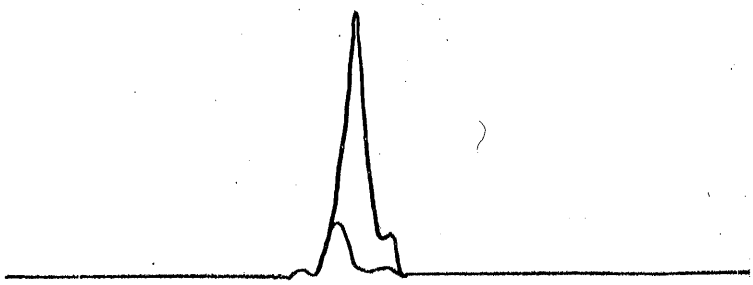
R	W	1/2C	R	W

16 Cores Cleared



R	W	C	R	W

Figure 4 c



Clear to 1/2 clear ratio for a single core after clearing 16 cores.

Figure 4d

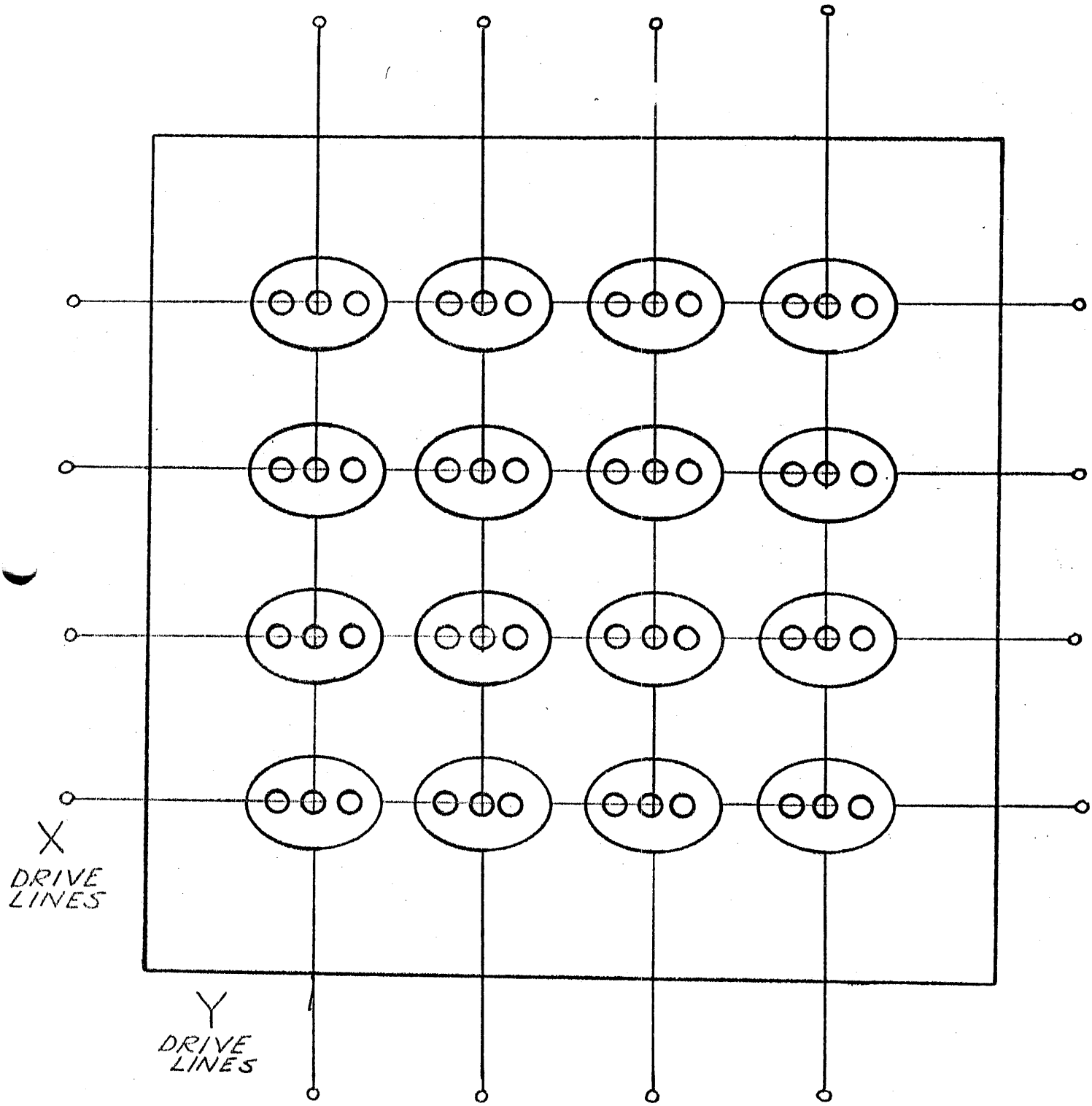


Figure 5

BIAS

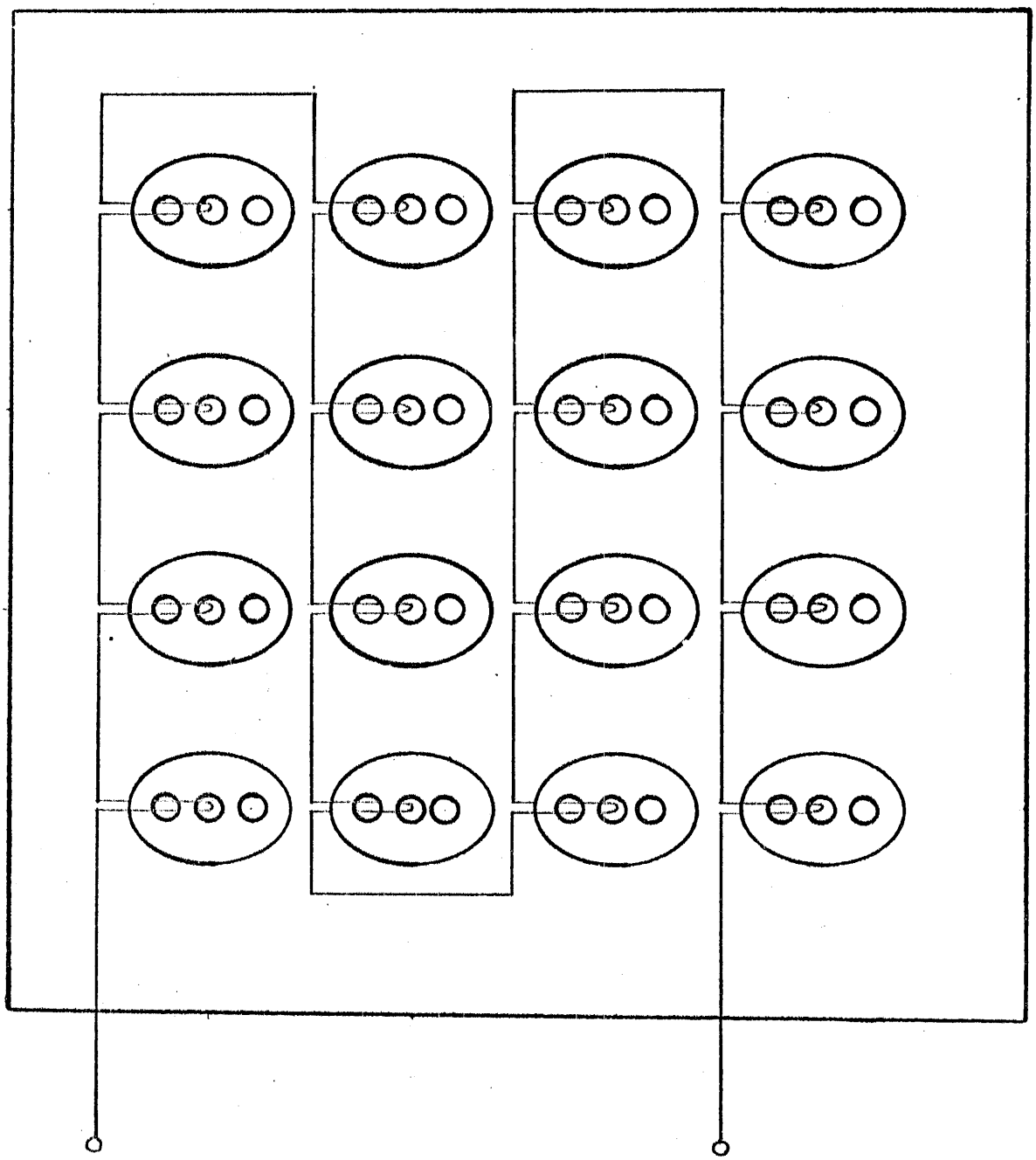


Figure 6

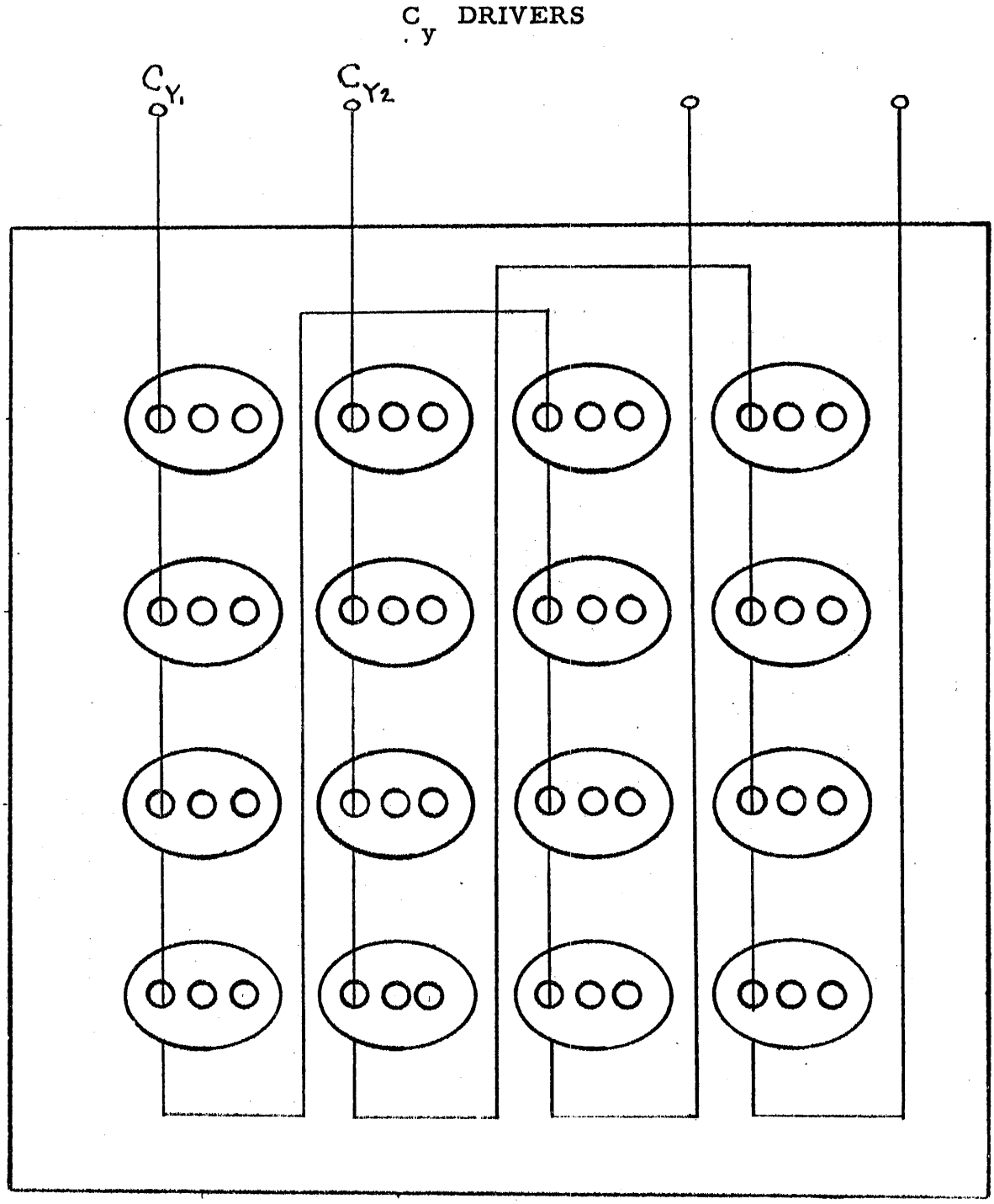


Figure 7

C_x DRIVERS

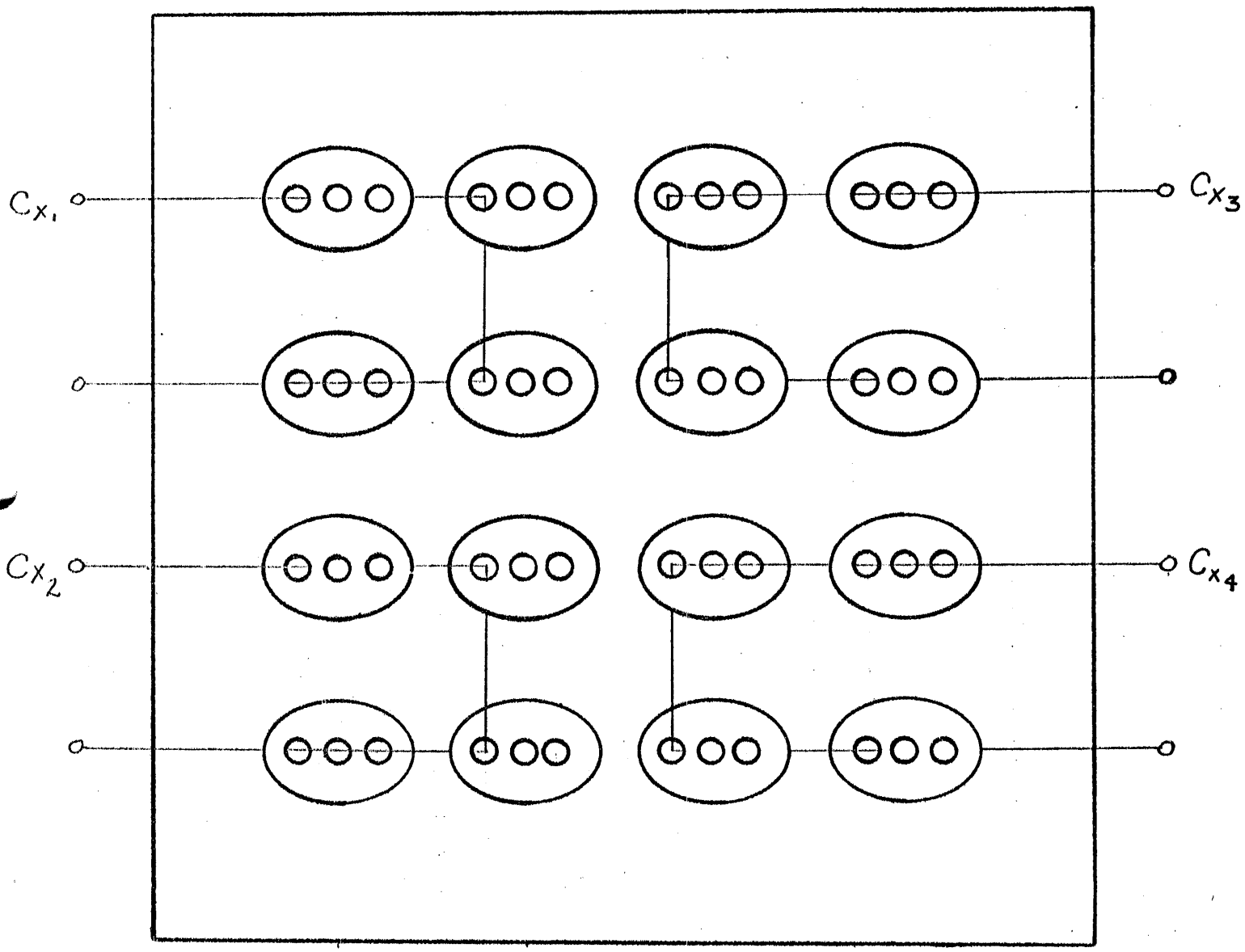


Figure 8

SENSE OUTPUT

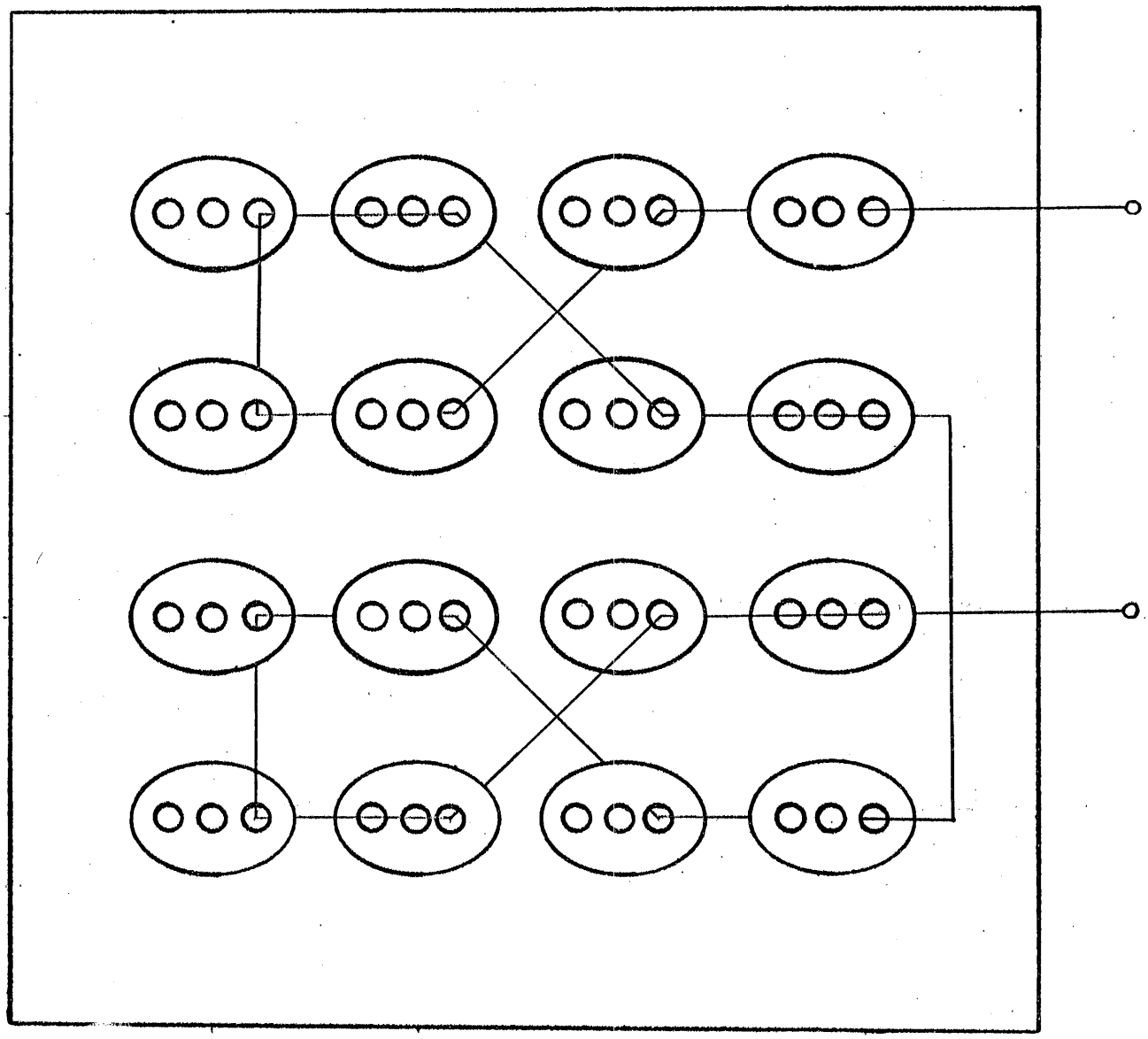


Figure 9