SERIES 7000 CIRCUIT MEMO # 11

SUBJECT: Memory Address Checking

REFERENCE: Project BETA File Memo #14-
February 6, 1956 by W. A. Hunt

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There is a need for address checking in magnetic core memory to determine if the input address was decoded properly and that the correct current drivers were selected.

A scheme for address checking in a magnetic core memory unit has been developed. The method proposed allows address checking to be done during a memory cycle. The method compares the decoded address with the input address.

On each output drive line of a matrix switch a core is placed. Through each core are wound sense lines, the bias line, and the drive line. (See Figure 1.) The sense lines numbered 1, 2, and 3 show which of the eight matrix switches were selected. (See Figure 2.) The other four sense lines show which of the sixteen possible outputs of the matrix switch were selected.

The operation of the encoding matrix is as follows:

> When a drive line is pulsed the sense lines which pass through the core on that drive line have an output. The sense lines are connected to sense amplifiers which detect the signals and send them to the comparison logic. (Figure 3) The input address is also sent to the comparison logic. If the address bits compare, no output is delivered to the alarm circuit from the last logic stage.

Figure 4 shows a memory which has been segmented. An encoding matrix would be on the outputs of each matrix switch. The outputs of the two levels of encoding units would be compared for similarity and then sent to the comparison logic.

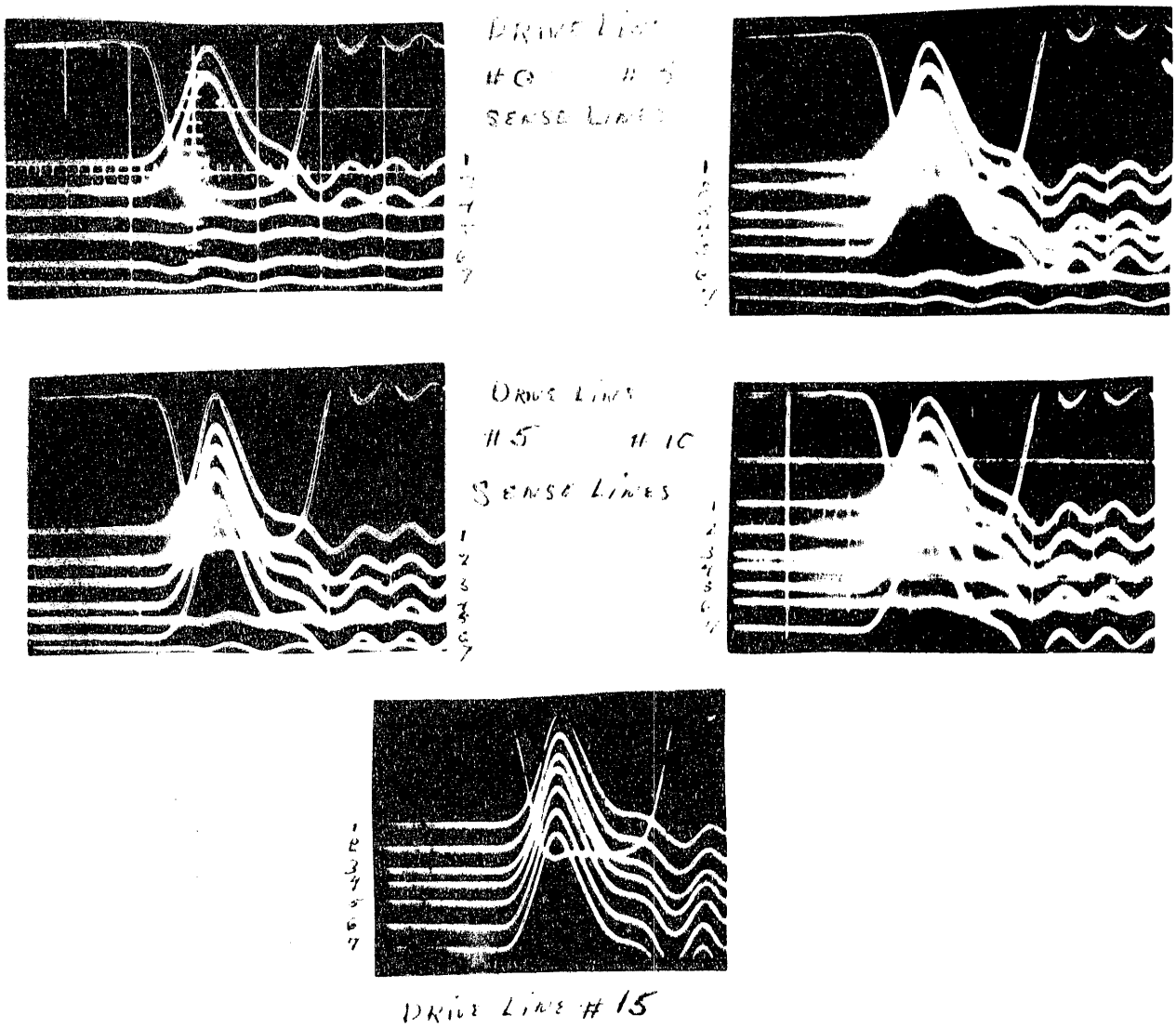
EXPERIMENTATION RESULTS:

Below are shown some of the outputs of a demonstration encoding matrix which was wound as shown in Figure 1. The cores were 50 - 80 toroids of DM-7b material. DM-7b material is an experimental ferrite developed in the Poughkeepsie Research Laboratory. The coercive force is 0.4 oersted, the switching time is 140 mμsec, and the one to zero ratio is 10 to 1. The data is a result of driving 50 - 80 toroids with one ampere turn read-write pulses. The rise time of these pulses was 50 mμsec.

The bias used to reset the cores was 0.26 amperes. In actual operation the bias would be used to prevent switching of the cores by spurious outputs of the matrix switch. The cores would be reset by the write current.

The scales are:

current 0.5 amp/cm
voltage 0.5 volts/cm
time 0.1 μsec/cm



CONCLUSION:

The encoding matrix offers a direct method to compare the decoded address with the input address.

If smaller cores of faster switching material are used, the back-voltage presented to the matrix switch will be less and the outputs. of the encoding units will be available sooner for address checking.

The encoding matrix may be expanded for use in any size memory. For example, in the proposed 512 word memory, the configuration is 32 x 16 words, only five sense lines are necessary.

RJF:dab

SENSE LINES: 1, 2, 3 Show which of 8 POSSIBLE MATRIX SWITCHES WAS SELECTED

SENSE LINES: 4, 5, 6, 7 " " " 16 " OUTPUTS of THE MATRIX SWITCH WAS SELECTED

THE OUTPUTS of THE SENSE AMPLIFIERS, SA, GO TO ADDRESS COMPARISON LOGIC

EXAMPLE: MS - 7 } WAS SELECTED THE CONTENTS of THE S.A's. ARE AS SHOWN
LINE - 10 }

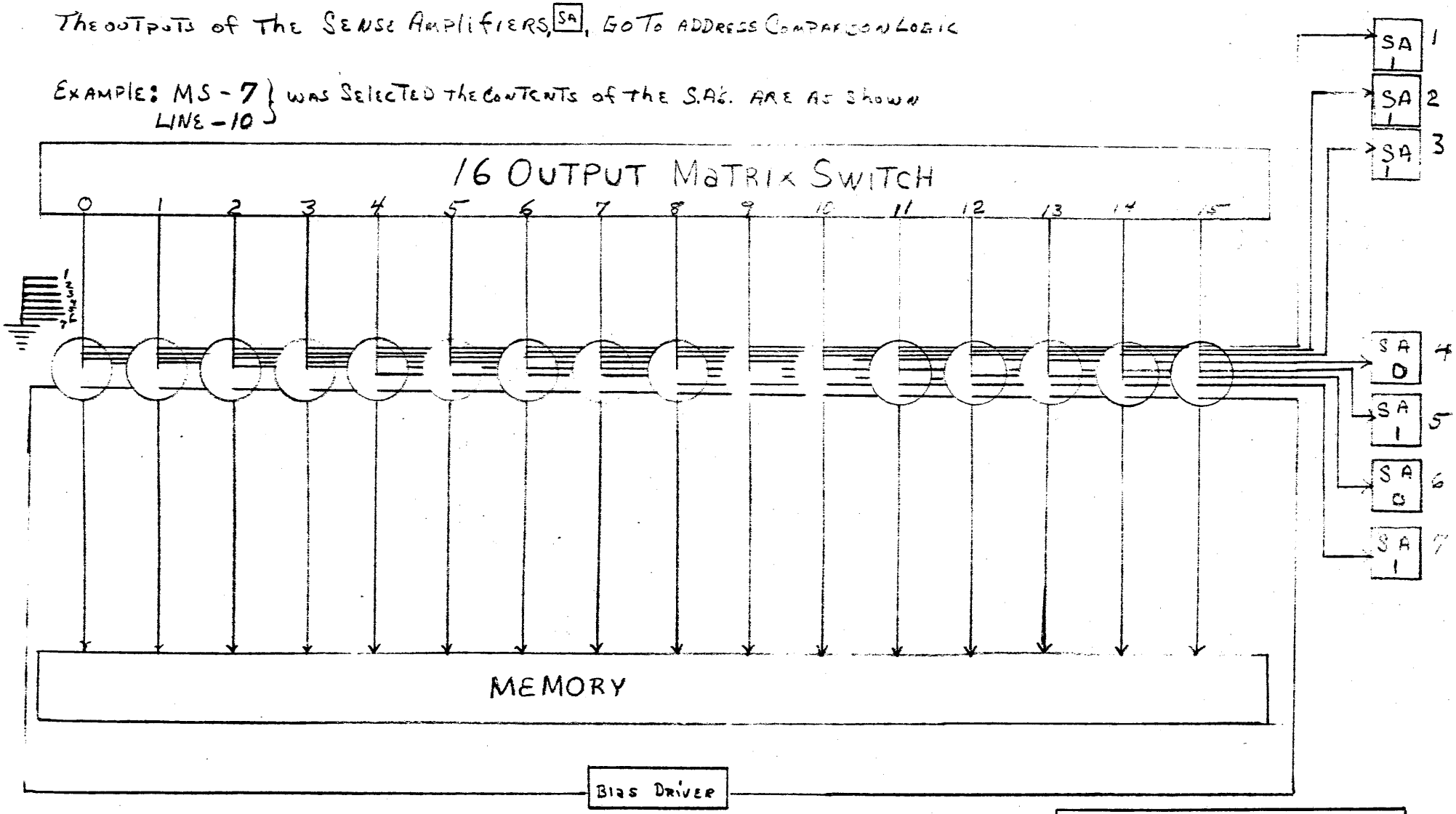


Figure 1

ENCODING SCHEME
FOR ADDRESS
CHECKING
RSK 101024

Checked: R. P. Lamm 3/26/57 R. J. Flaherty 3-25-57

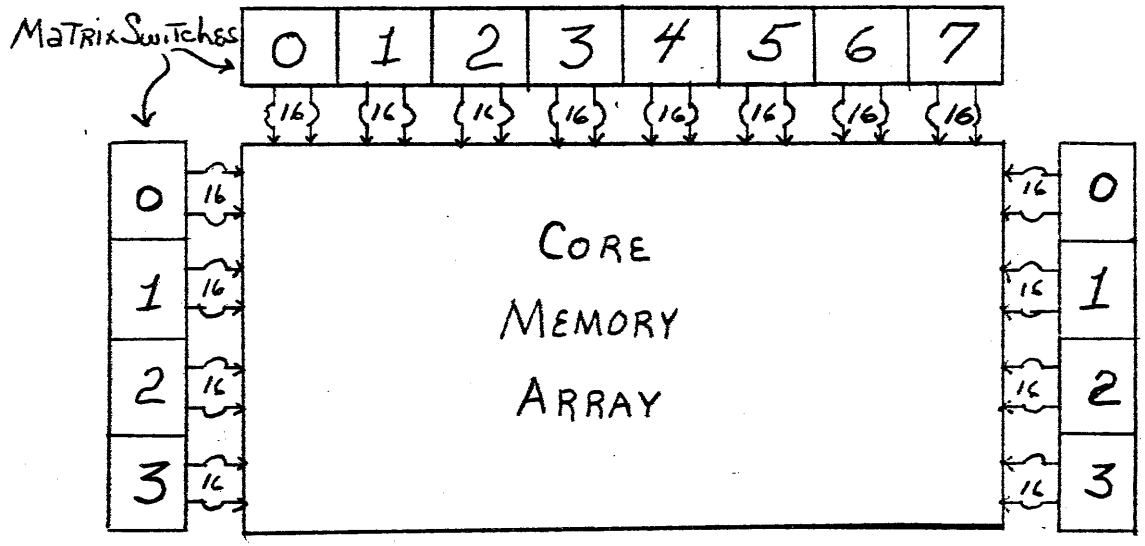


figure 2

Arrangement of Matrix Switches Around a Memory Array

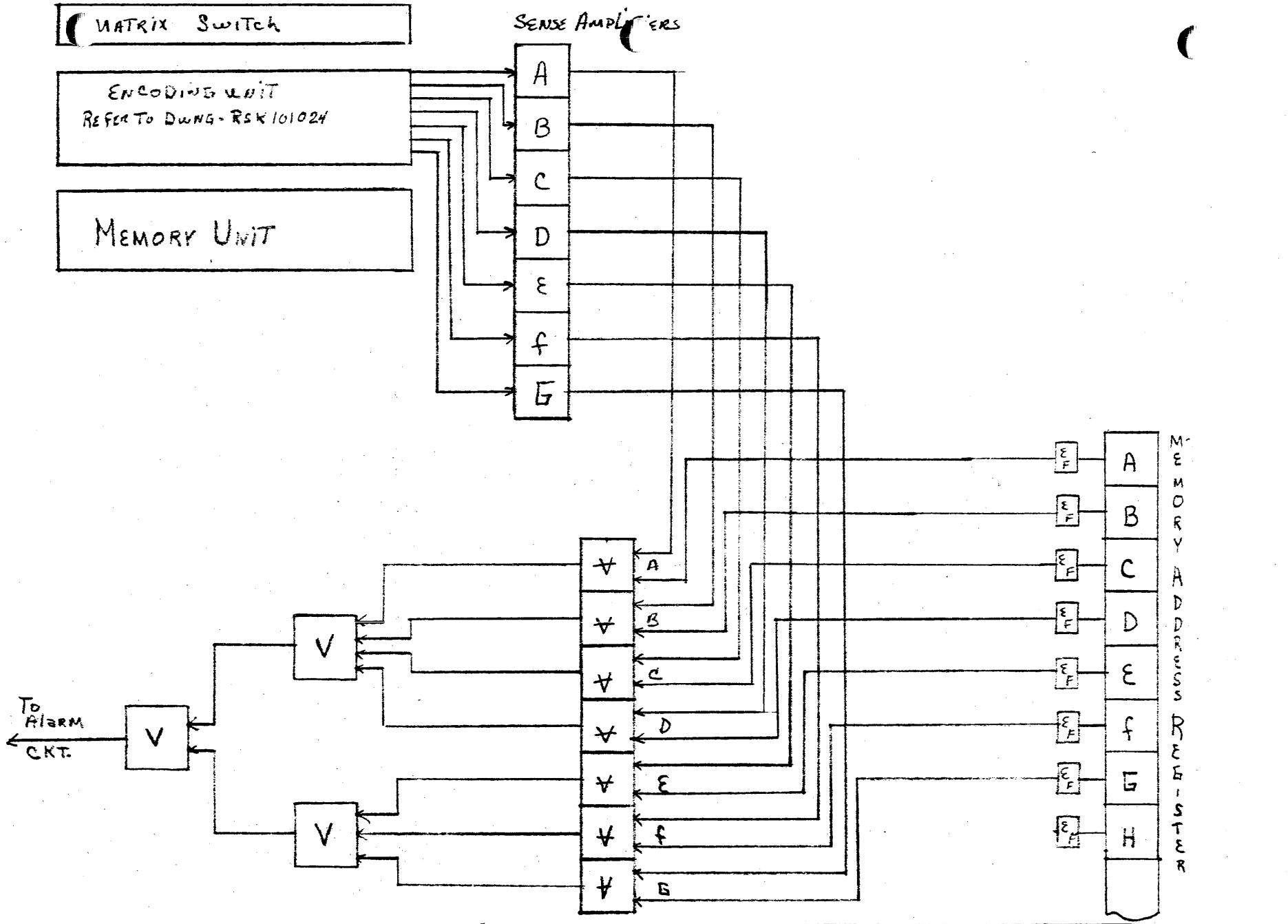


Figure 3

COMPARISON SCHEME
FOR
ADDRESS CHECKING

RSK 101027
3-29-57
R. F. Flaherty

Checked R. F. Flaherty 5/29/57

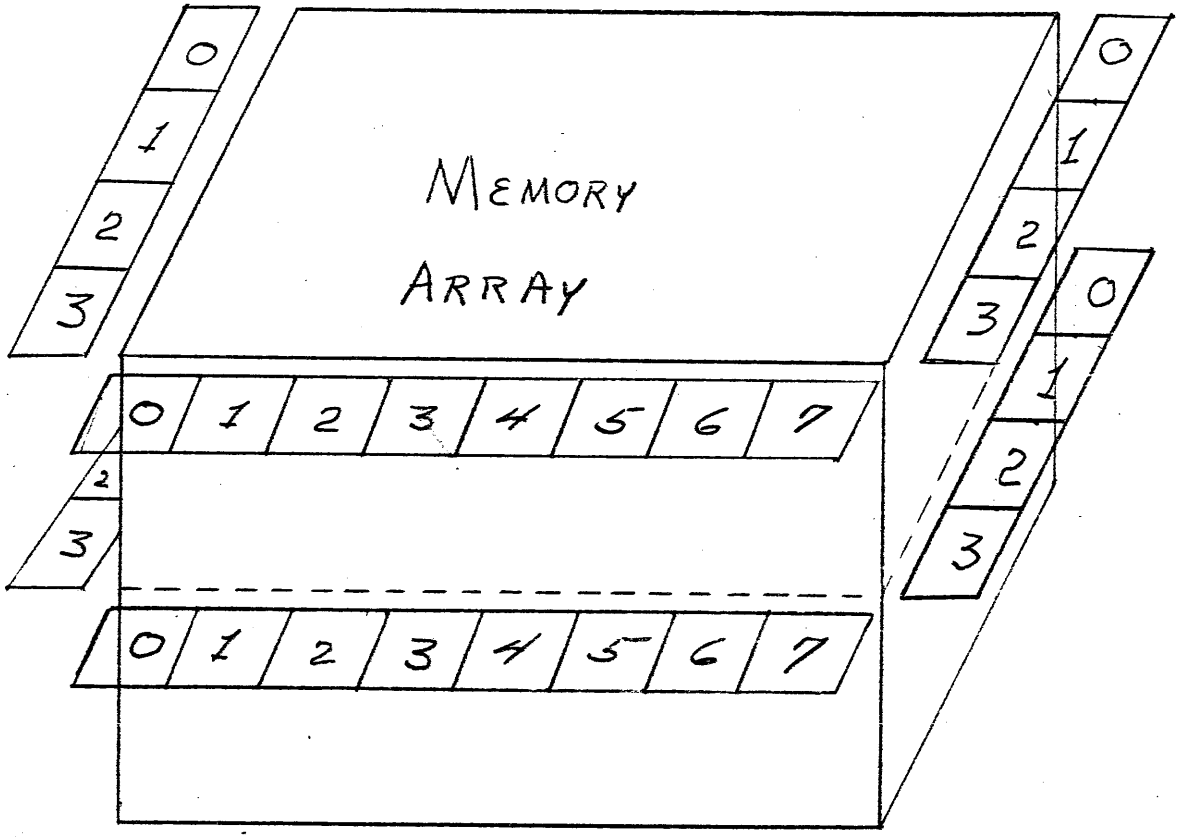


figure 4

ARRANGEMENT OF MATRIX SWITCES AROUND A SEGMENTED MEMORY