COMPANY CONFIDENTIAL

STRETCH CIRCUIT MEMO #5

SUBJECT: The Construction and Evaluation of a Six Bit Arithmetic Model

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SUMMARY: This report describes the construction and test results of a six bit transistorized asynchronous adder and subtracter, utilizing 496 SB-100 surface barrier transistors and 173 zener diodes.

PURPOSE:

The model was constructed, using a logical scheme of J. Pomerene, in order to evaluate the millimicrosecond non-saturating transistor switching circuits.

LOGICAL LAYOUT

The logical scheme used, in this model, is one by which the addition or subtraction operation is not complete until the sum or difference has been obtained and checked.

ADDITION:

Each of the registers are equipped with a S.P.D.T. switch, by means of which a one or zero can be inserted into it. The augend and addend numbers are summed with the carry number in the adder, and the resultant number, which is the adder's answer, is propagated to the subtracter where it is summed with the complement of the addend register. The difference number should be the same as the number in the augend register. These two numbers are then fed into a comparing circuit which gives an indication as to whether the operation was performed correctly.

SUBTRACTION:

The subtracter, in this model, is a two's complement subtracter, which gives a difference by the addition of the minuend number with the complement of the subtrahend number. This number is propagated to the adder where it is summed with the subtrahend number. The resulting number should be equal to the number in the minuend.

The block layout of the logical network is shown in Figure 1.

CIRCUITS

In the arithmetic section, the model consists of three basic circuits:

(a) complemented "exclusive or"
(b) complemented "and"
(c) emitter follower pull-over reset triggers

In these circuits a logical one is denoted by a voltage level of 0.6 volt and a logical zero by -0.6 volt.

ADDER AND SUBTRACTER:

The adder and subtracter sections are entirely constructly with the complemented "exclusive or" circuit as shown in Figure 2. In this circuit, 8 ma., flowing out of the four common collector branch, denotes a one. One unit of current, 4 ma., denotes a zero. In the two common collector branches, one unit of current, flowing out, denotes a one, and no units of current denotes a zero. By the use of this principle, a full adder or subtracter can be reduced to three "exclusive or" circuits. The block layout of these sections is shown in Figures 3 and 4.

AUGEND AND MINUEND REGISTERS:

These registers are constructed with emitter follower pull-over triggers controlled by the complemented "exclusive or" circuit, as shown in Figure 5.

The "exclusive or" control circuit in the augend register operates this stage in the following manner. During the addition time, the input of one section is fed by a S.P.D.T. switch which will insert a one or zero into the register. This section is also fed by a positive signal, G+, from the main control panel. The other section is fed by the difference output and a negative signal, G⁻, from the main control panel. Therefore, the position of the switch will determine whether a one or zero is inserted in the register.

During the subtraction cycle, the G^+ signal is negative and the G^- signal is positive; therefore, the number in the augend register is determined by the difference output number. The block layouts of the augend and minuend registers are shown in Figures 6 and 7.

ADDEND AND SUBTRAHEND REGISTER:

This register is constructed with the emitter follower pull-over trigger, controlled by the complemented "and" circuit as shown in Figure 8. In this register a one or zero is inserted into the register, during the addition or subtraction cycle, through the connection of the S.P.D.T. switch applied to one input of the complemented "and" circuit. A reset pulse, from the main control panel, which is positive during the add. and subt. cycles and negative during the reset cycle is connected to the other input. The block layout of this register is shown in Figure 9.

COMPARING CIRCUIT:

The comparing circuit is constructed with the complemented "exclusive or" and the complemented "and" circuits as shown in Figure 10. This circuit is used to give an indication when the final addition or subtraction cycle has been completed. The complemented "and" circuit has twelve inputs, two from each bit. Each, of these inputs, is set by the output of a complemented "exclusive or" circuit, that is in a positive state if the machine operation is correct. If there is a machine error, one or more of the "exclusive or" outputs will be negative, therefore, setting the complemented "and" circuit's output in a negative state. The block layout of this section is shown in Figure 11.

MAIN CONTROL PANEL:

The main control panel has to be capable of instructing the model to reset, dump, and add or subtract. This system consists of a sine wave oscillator, overdrive amplifier, binary trigger, and two complemented "and" circuits. This unit has to be capable of driving six reset terminals, twelve G^+ terminals and twelve G^- terminals. In order to obtain this driving power, the circuit shown in Figure 12 was used as drivers for the reset, G^+ and G^- outputs.

The output of the sine wave oscillator is fed into the overdrive amplifier, producing a square wave, which is used as the reset pulse and the driving signal for the binary trigger and one input of each of the complemented "and" circuits. The outputs of the binary trigger are used as the other inputs of the "and" circuits. Therefore, a positive signal is obtained at the output of the complemented "and" circuits when their inputs are both positive. The timing chart of the reset, G^+ and G^- signals are shown in Figure 13. The block diagram of this system is shown in Figure 14 and the schematic is shown in Figure 15.

CONSTRUCTION

The various transistor circuits were constructed on individual copper phenolic panels, with three bits to each panel. By joining the panels, a common ground bus is available for the entire model, thereby minimizing the effects of ground currents. The entire model lay-out is shown in Figure 16. This arrangement minimizes the lead length coupling the various stages.

TESTING

In testing the model, the following operations were investigated:

(a) max. total addition and subtraction times.
(b) total addition and subtraction times through one bit.
(c) average carry time per bit.
(d) average logical block delay time.

A. The maximum addition time is for the case of A = 31, B = 1. In this case, a carry signal is developed in the adder of bit 1 and propagated through each stage until an answer is obtained at bit 6. During this same time, a carry is propagated thru the subtracter towards bit 6. Thus, when the subtracter of bit 6 receives the adder's number and sends its number to the comparing circuit, the comparing circuit indicates if the cycle has been completed. The total time for this operation is approx. 196 millimicroseconds, Figure 17, with 120 millimicroseconds, Figure 18, being necessary for the propagation of the adder number from the augend register in bit 1 to the adder output of bit 6.

In this model the control circuits, for the A and T registers, have two logical blocks, while the B registers have one. The total delay, in one bit, between the B signals and the A or T signals is approx. 30 millimicroseconds, Figure 19. This delay causes the B register to begin switching the adder or subtracter before the signal from the A or T registers arrive. In the add cycle, when the signal from the A register arrives the adder is then switched to its true state, thus producing a logical noise pulse on the output of bit one's adder. In the addition case of A = 31, B = 1, the noise pulse is propagated to the subtracter of bit 1. Therefore, the subtracter, of bit 1, will have at its input terminals, the signal from the B register and the noise pulse from the adder, Figure 20. These signals will produce a carry signal, Figure 21, in the subtracter. This carry signal increases the total subtracter propagation time by approx. 20 millimicroseconds. The total add time can be reduced by the time delay caused by the presence of the noise pulse in the subtracter's carry.

The maximum subtraction time is for the case of T = 48 and B = 16. In this case, the total time is determined from the time a 1 appears in the subtrahend of bit 5 until the comparing output goes to its final state. This case constitutes a propagation of the carry

signal thru 5 bits in the subtracter and produces an answer at the subtracter output of bit 6. Since the system of the subtracter is a two's complement, the total time is reduced by the delay time of one logical block, approx. 20 millimicroseconds. The total time is 160 millimicroseconds, Figure 22. This time is also increased due to a noise pulse in the adder's propagative line.

B. The total addition and subtraction times, through one bit, are for the cases where A = 1 B = 0 and T = 1 B = 0. The time for the addition case is shown in Figure 23 and the subtraction case in Figure 24. These times represent the fastest time in which an operation can be completed in the model, which is approx. 130 millimicroseconds.

C. In determining the propagation time of a carry signal through the system, a timing measurement at the outputs of bits one through five was taken for the add. case of A = 31, B = 1. The per bit times are as follows:

A_1 to carry out of bit 1 = 18 millimicroseconds
A_1 to carry out of bit 2 = 39 millimicroseconds
A_1 to carry out of bit 3 = 58 millimicroseconds
A_1 to carry out of bit 4 = 80 millimicroseconds
A_1 to carry out of bit 5 = 100 millimicroseconds

This measurement gives an average propagation time of the carry of 20 millimicroseconds per bit.

D. The average logical delay times in the system can be determined by the number of logical blocks and triggers necessary to produce an output. The average time a signal is switched thru an individual logical block is 20 millimicroseconds and 25 millimicroseconds for the total trigger circuit i.e., the emitter follower pull over reset trigger and it control circuit.

PROBLEMS

The following problems were encountered in the model:

(a) During the initial checking of the model, it was found that for various addition and subtraction settings, the model would not respond correctly. In these cases, if the power supplies were adjusted, the model would then respond correctly. This problem was due to several of the registers' output swings not being sufficient to cause the circuits that they are driving, to switch. By the nature of the construction of the emitter follower,

this portion of the circuit must have an 0.3 volt and -0.9 volt swing at its input in order to maintain a 0.6 to -0.6 volt level at its output. The input swings, in the faulty registers, were approximately 0.3 volts too positive and were corrected by changing the resistor connected to the positive supply, at the junction of the diode and the peaking coil.

(b) As was previously stated, the total addition and subtraction times were increased due to a logical noise pulse. This problem can be eliminated by making the B-register slower i.e., eliminating the emitter follower output and using the output of the collector of the adjacent inverter.

(c) The subtracter initially was a one's complement. During the reset cycle, a one was propagated thru the subtracter's carry causing the line to oscillate. To correct this fault, the two's complement system was employed.

POWER REQUIREMENTS

The total d-c power required by the arithmetic section is approx. 114 watts, of which the positive supply provides 52 watts and the negative supply 62 watts. The main control panel requires approx. 10.9 watts of which 4.3 watts is supplied by the positive supply and 6.6 watts by the negative supply.

POWER SUPPLY VARIATIONS

In order to determine the reliability and effects, of the model, due to power supply, voltage variations, investigations were made of different power supply settings. It was found that the optimum power supply voltages were plus 40 and minus 43. With these settings, the model exhibited its fastest propagation time. If the signs of the power supplies were disregarded, the same time propagation was attained as long as there was a three volt setting between the two supplies i.e., if the positive supply decreased to plus 38, the negative supply should be set at minus 41. This effect seem to suggest that the power supplies used, in the system, should be constructed so that they will vary simutaneously.

If the supplies do not maintain the three volt difference, there will be a decrease in the propagation time. When the negative supply was kept at a constant potential and the positive supply was varied in

both a positive and negative direction, the model failed when the constant emitter current became 3.5 and 5 milliamps respectively or a 12.5% decrease and a 25% increase. This is shown in the following table for the case of A=31 and B=1.

+ Supply (volts)	- Supply (volts)	Propagation Time (μ Sec)
36	43	Failed
37		270
38		260
39		240
40		196
41		200
42		260
43		270
44		290
45		310
46		Failed

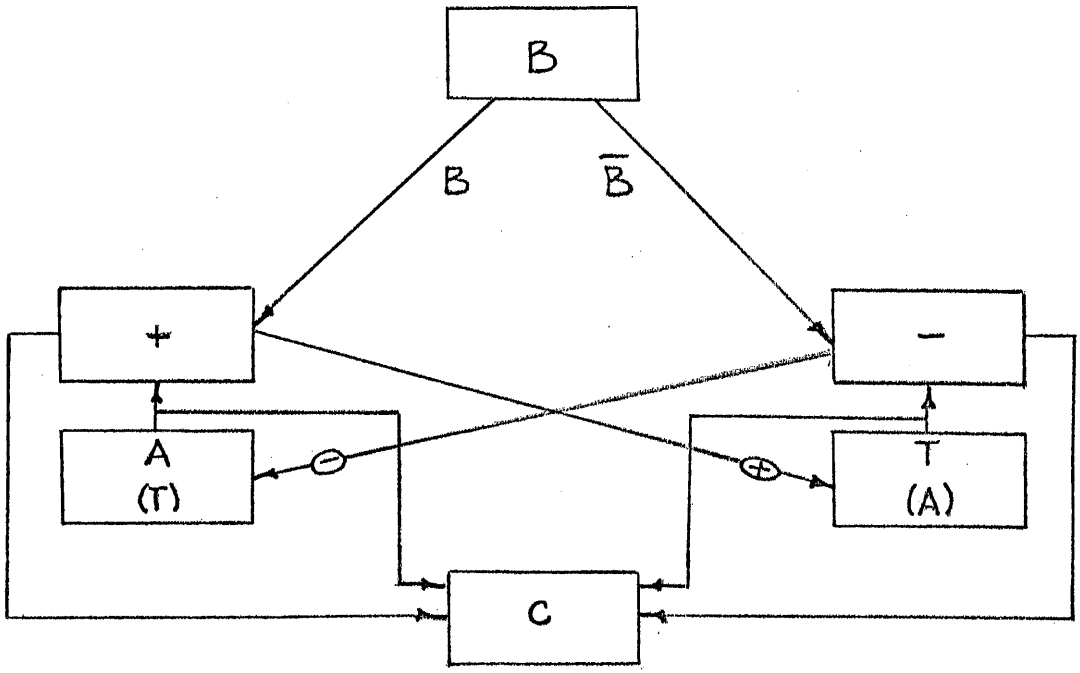


FIG. 1

B = addend or subtrahend register
A = augend or minuend register
T = temporary register
+ = adder
- = subtracter
C = comparing circuit
⊕ = gate open throughout add cycle
⊖ = gate open throughout subt. cycle

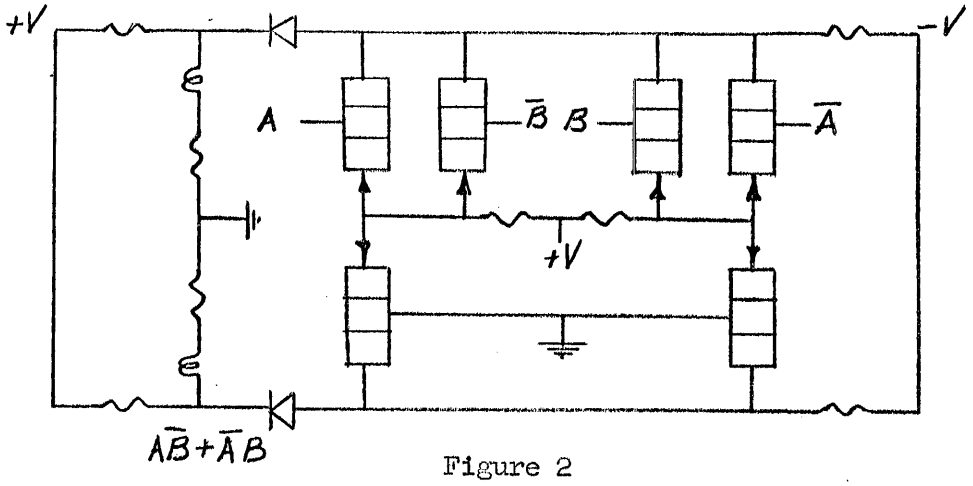


Figure 2

Complemented "exclusive or"

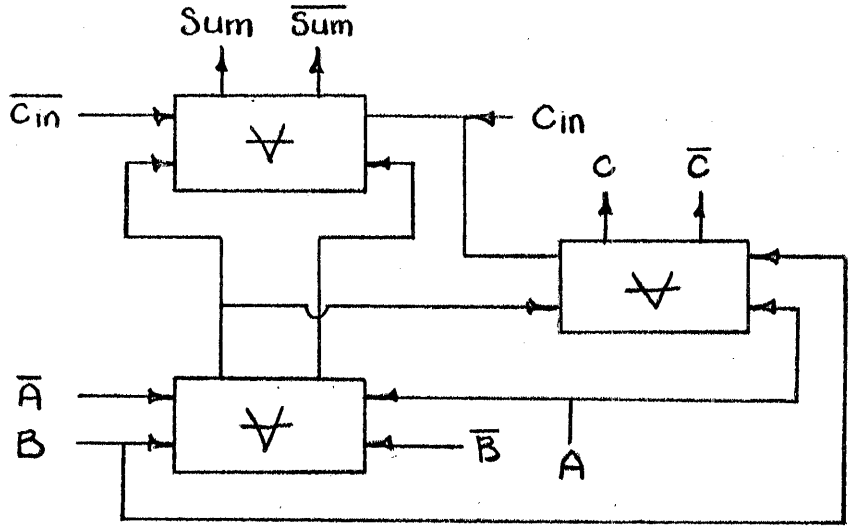


Figure 3

Adder

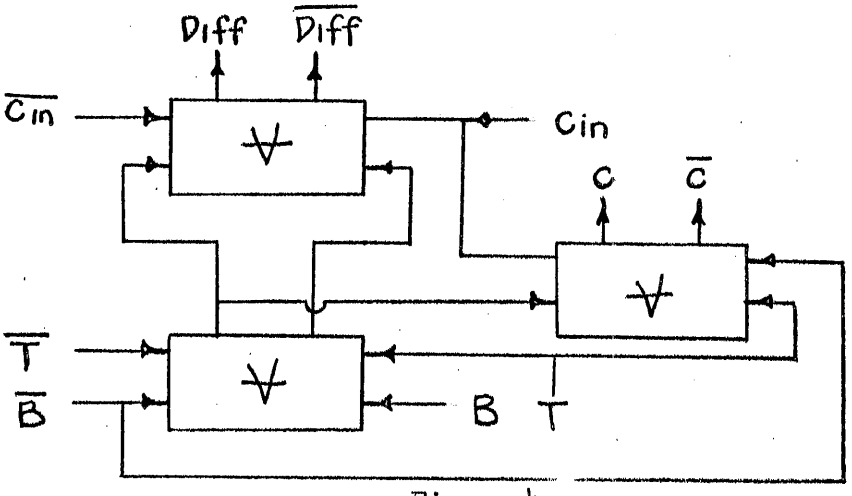


Figure 4

Subtracter

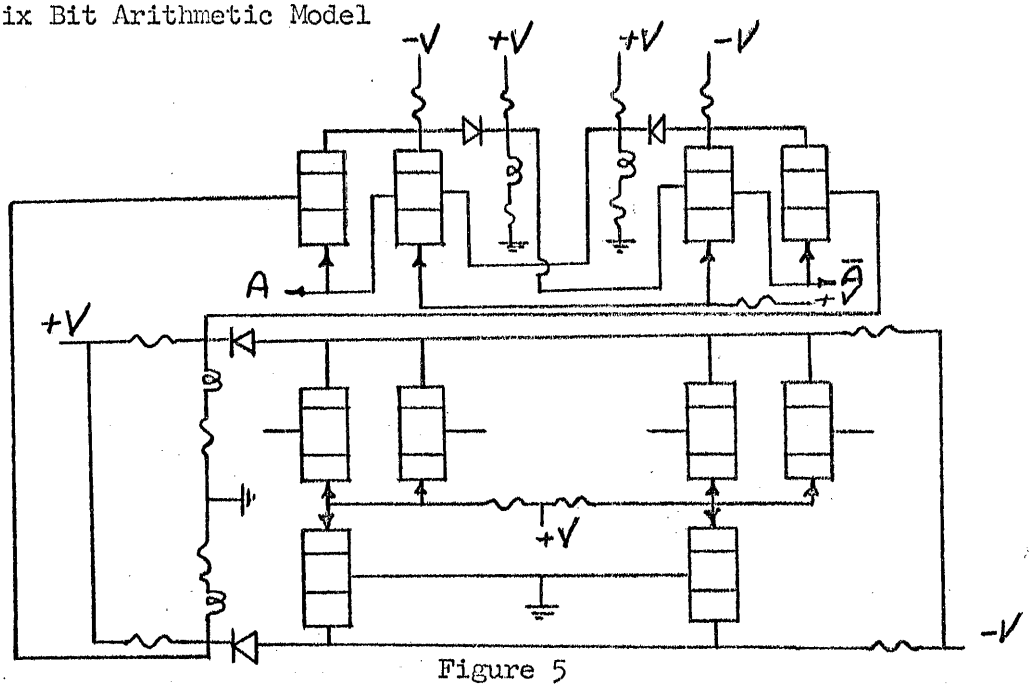


Figure 5

Augend and Minuend Registers

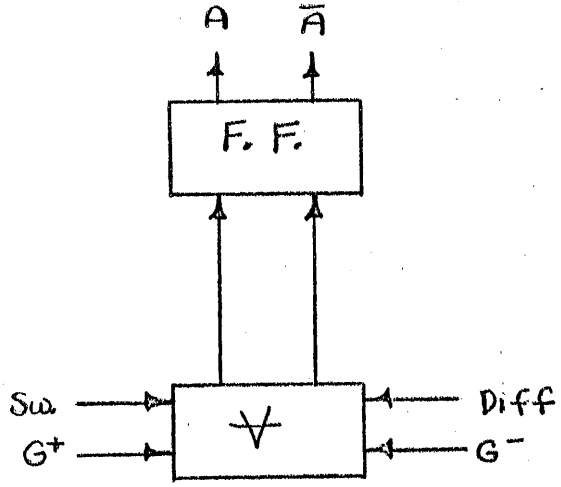


Figure 6

Augend

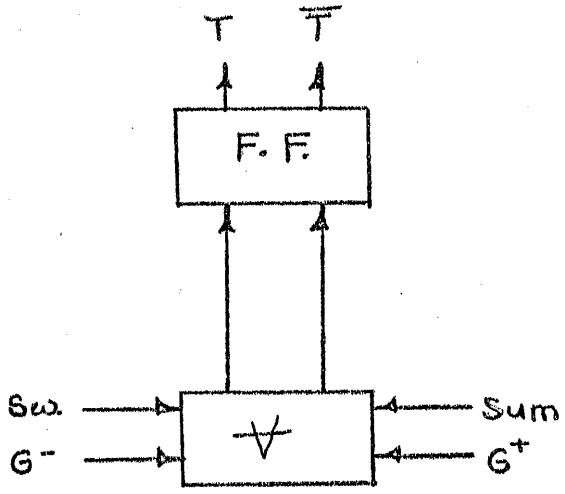


Figure 7

Minuend

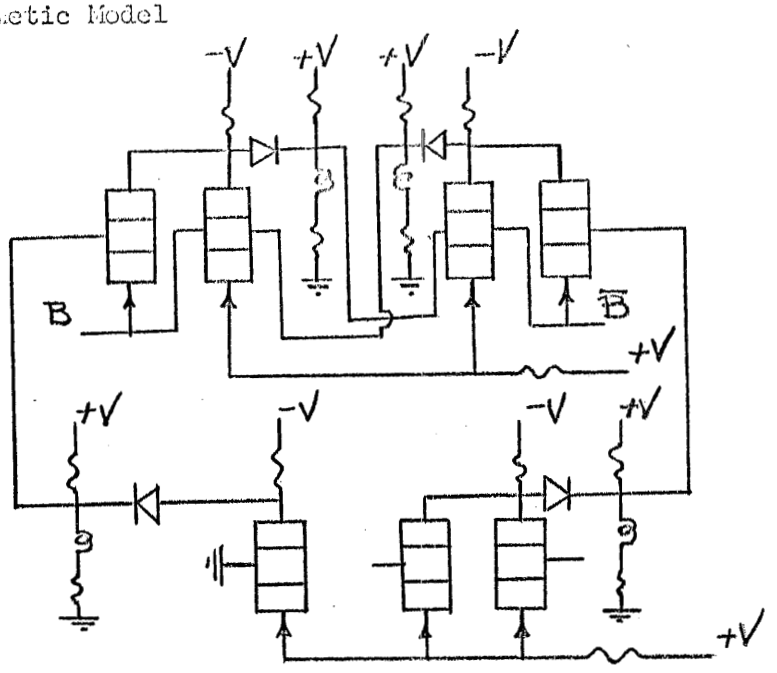


Figure 8

Addend and Subtrahend Register

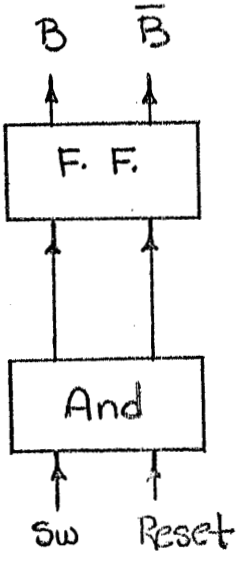


Figure 9

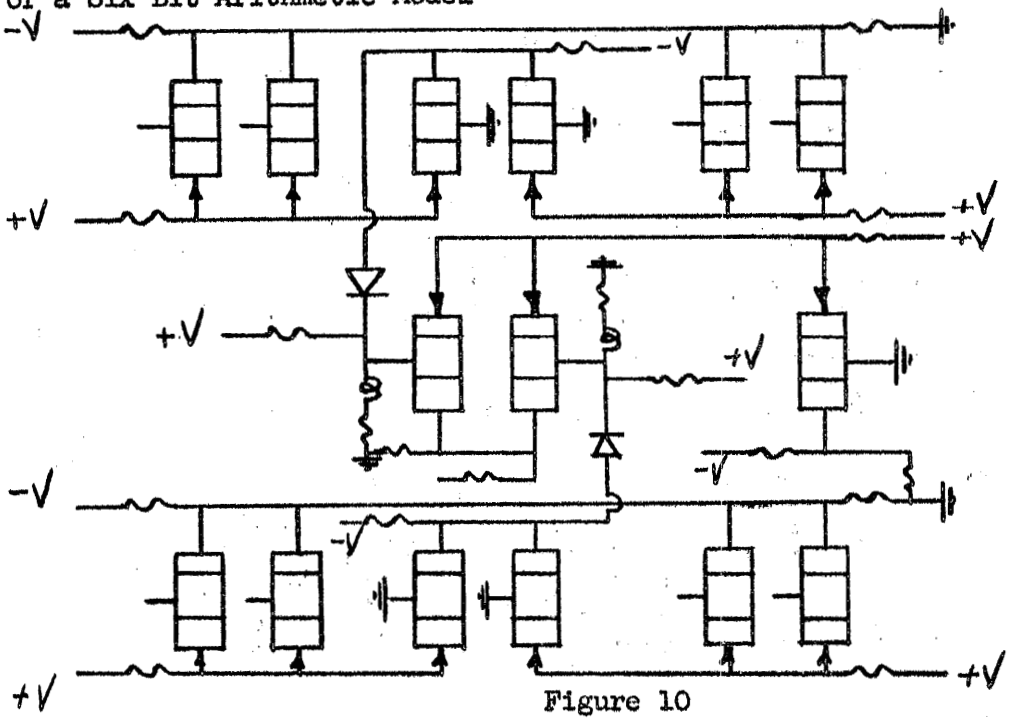


Figure 10

Comparing Circuit

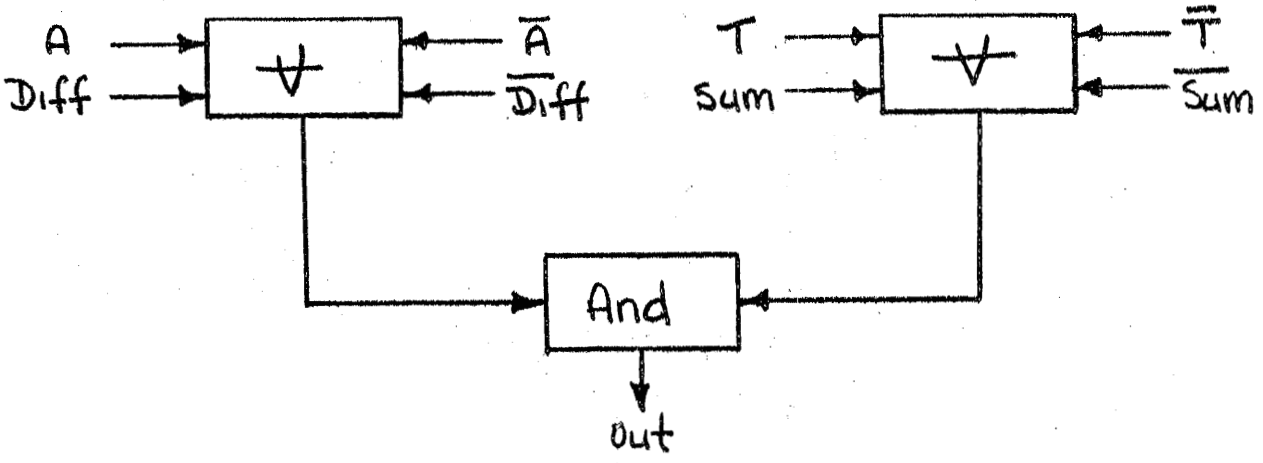


Figure 11

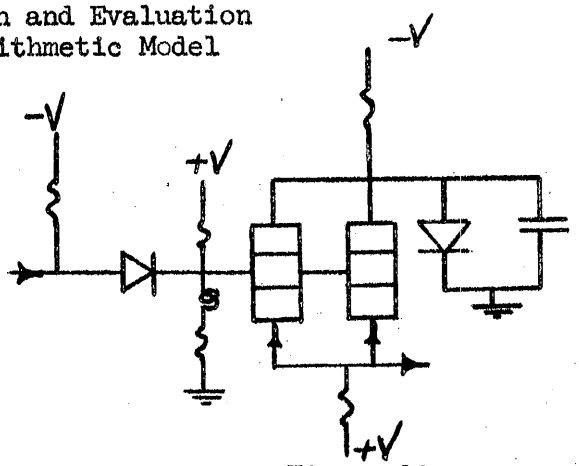


Figure 12

Driver

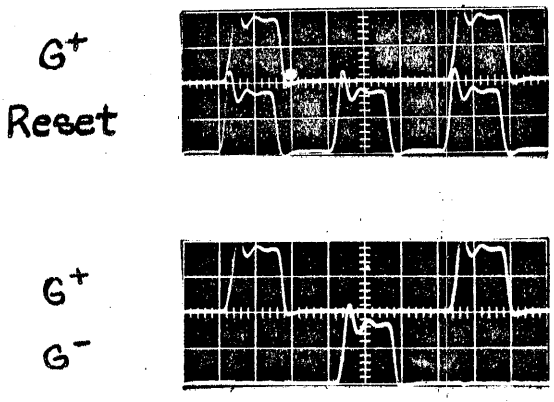


Figure 13

Timing Chart

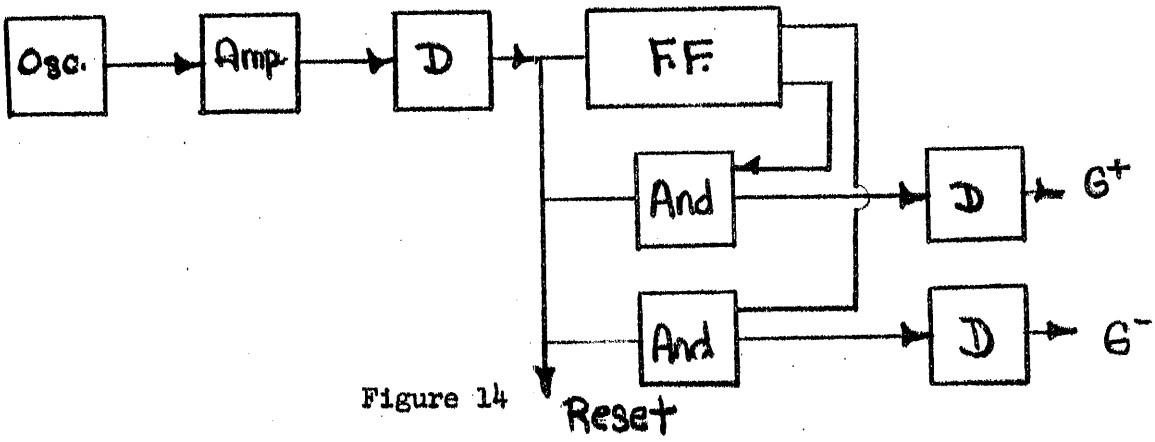


Figure 14

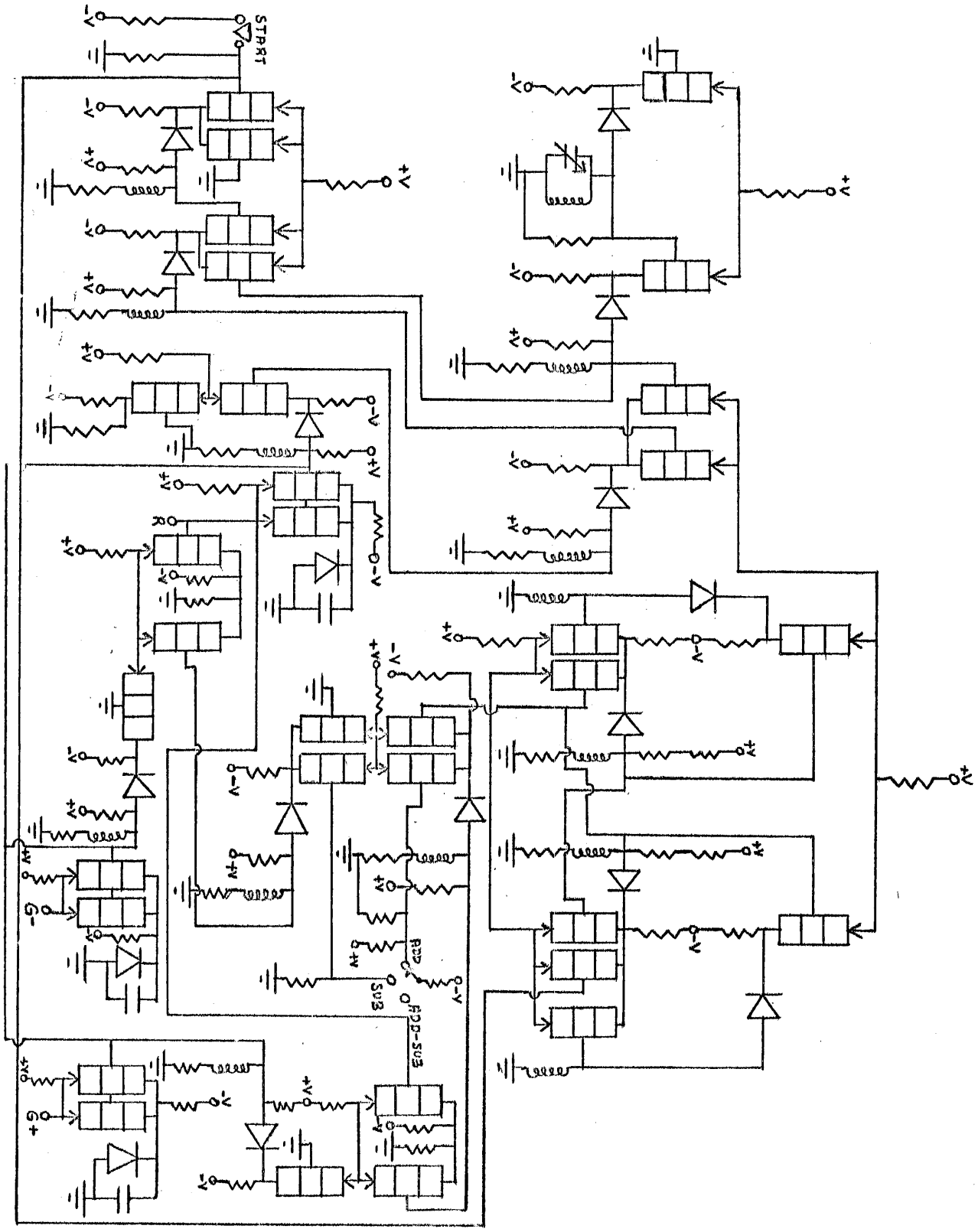


Figure 15

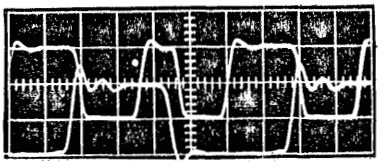
Main Control Panel

Adder		
Augend	$A_6 \rightarrow A_4$	$A_3 \rightarrow A_1$
Addend or Subtrahend	$B_6 \rightarrow B_4$	$B_3 \rightarrow B_1$
Comparing		
Minuend	$T_6 \rightarrow T_4$	$T_3 \rightarrow T_1$
Subtracter		
	Register No. Panel	Control Panel

Figure 16

Model Layout

Comparing output
$Augend_1$ output

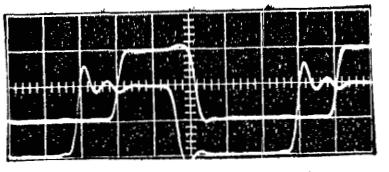


Time = 0.1 μsec/cm

Figure 17

A = 011111
B = 000001

$Adder_6$ output
$Augend_1$ output

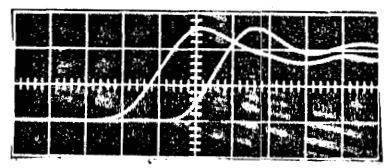


Time = 0.1 μsec/cm

Figure 18

A = 011111
B = 000001

Addend$_1$ output
Augend$_1$ output

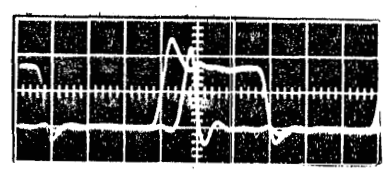


Time = 20 mμsec/cm

Figure 19

A = 000001
B = 000001

Addend$_1$ output
Adder$_1$ output

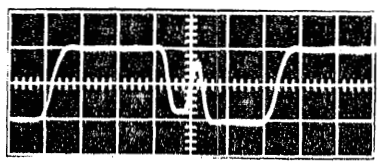


Time = 0.1 μsec/cm

Figure 20

A = 011111
B = 000001

Subt.$_1$ carryout

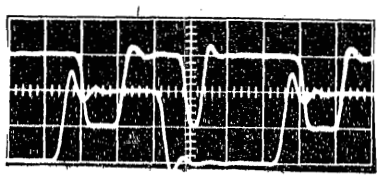


Time = 0.1 μsec/cm

Figure 21

A = 011111
B = 000001

Comparing output
Subtrahend$_5$ output

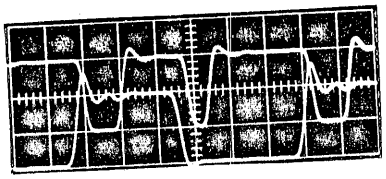


Time = 0.1 μsec/cm

Figure 22

T = 110000
B = 010000

Comparing output
Augend$_1$ output

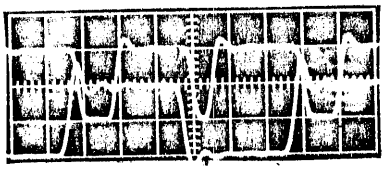


Time = 0.1 μsec/cm

Figure 23

A = 000001
B = 000000

Comparing output
Minuend$_1$ output



Time = 0.1 μsec/cm

Figure 24

T = 000001
B = 000000