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A HIGH SPEED CORE LOGIC READER

An evaluation of core logic and transistor drivers in the proposed Stretch 1,000 card per minute reader.

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Introduction and Objectives

An exploratory investigation into the feasibility of using core logic in the Stretch card reader was made during the month of August, 1957. The immediate objectives were to investigate known core techniques as they might be applied to a high speed reader to ascertain both the advantages and limitations imposed by using core logic. Secondly, the current driver problem using power transistors was investigated by the Stretch Exchange circuits group.

Reader Logic

The investigation was conducted with the assumption that the Stretch card reader would read cards by row and transfer the information to the Exchange between rows at the rate of 1,000 cards per minute. A checking circuit that would indicate the column and row of single errors and double error detection was also considered. Another feature of byte count control was included to allow the operator to use only a portion of each card read. Off line operations were not considered in this investigation.

Building Blocks

Pulse logic and D.C. logic must be compatible in a computing system and to bridge the gap a series of eight different types of compatible circuits have been developed so that the voltage to pulse (V.P.) or pulse to voltage (P.V.) transition can be accomplished. The V.P. and P.V. blocks are used with such devices as C.B.s, emitters, contacts, push buttons, line levels, etc.

One type of V.P. circuit emits a single pulse when a voltage is impressed at the input while still another will emit a train of pulses. A single pulse might be used to advance a counter or set or reset a trigger. A train of pulses senses the presence of some D.C. condition and emits until the level is removed.

Other logical blocks developed are capable of performing all of the logical functions presently found in tube logic.

One block known as a transfer has no equivalent in tube logic but is analogous to the translate block in transistor logic and serves a similar function. It can be used to correct phase relationships in parallel paths of logic, for a branch generator, for clocks, etc. The transfer function generally speaking is the most widely used logical block in pulse work.

The gain through a logical connective is greater than unity and elimin-

ates the need for amplifiers.

Logical Card Requirements

The investigation shows that the core logic version of the reader described would require approximately 444 logical circuits. The count by type and machine logic performed is as follows:

TYPE OF CARD	V.P./P.V.	A_N	X	A	O	TOTAL
Controls	16	20	27	10	12	85
Step Counter and Controls		10	10	10		30
Matrix Controls			20			20
#2 Matrix to Register (Info.)	8		24			32
#1 Matrix to Check Gen.	8					8
Byte Count Trig. -Decoder-Control	6	5	6	28	4	49
#1 Check Gen. for Column		31	12	12	22	77
#1 Check Gen. for Row	8	8	2	4	10	24
#2 Check Gen. for Column		31	12	12	22	77
#2 Check Gen. for Row		8	2	4	10	24
Check Transfer for Column				10		10
Check Transfer for Row			4	4		8
	38	113	119	94	80	444

Packaging

The logical blocks are packaged into cards so that each card is a logical circuit. This is desirable from an assembly view point since all logical cards can be bench tested before becoming part of an assembly.

This unit package is also desirable from a service view point since a faulty card can be replaced as a unit.

A pluggable unit can hold 48 logical cards and occupies a space 1 1/2 " high, 8 1/2 " wide, and 8" long.

It is significant to note here that each card can accomodate a maximum of six cores since there are no logical blocks which exceed this number. The transfer function, which is the most widely used building block, requires only three cores and therefore it is possible to put two transfer blocks on a single card. This results in a space saving technique which amounts to better than one pluggable unit in the reader being considered. The core logic version of the Stretch reader would require eight pluggable units or a volume 12" high, 8 1/2" wide and 8" long.

Core Logic Speeds

The basic machine cycle must not exceed 12.5 us at the present state of the art and is composed of six pulses which operate in an A, B fashion 180^0 out of phase. Each logical connective has an inherent delay of one-half of the basic cycle chosen. This logical delay suggests that high initial access time must be expected.

The 1,000 card per minute reader would operate in a base cycle range of approximately 20 us and would have a byte rate of approximately 80 us. The byte rate chosen allows enough time to read out between rows with an adequate safety factor and also allows the Exchange to consider the reader as an I/O device with a weight count of one since the byte rate falls in the 60 us to 120 us category.

It is possible to operate parallel paths of logic at different speeds which results in fewer logical blocks. The buffer is a good example of this technique. The buffer can be dumped at the byte rate required while the logical circuits needed to generate a parity bit can operate at some even submultiple of the byte rate. It is possible, therefore, to do many logical operations between bytes and have the logic and information in phase at the output. Logical speeds other than the base machine cycle also requires a separate driver. The advantage gained in dual speed logic out weighs the disadvantage of the added driver.

Buffer and Control

Through the use of core logic it is possible to set the buffer cores directly with the brushes and read out the buffer cores using the core logic as a driver source.

The row buffer matrix which is 8 x 10 could be read out broadside (eight bits per byte) using a transfer block which is capable of driving up to 13 type 50-80 memory cores with reliability as a drive source. Since the Stretch reader is dealing with binary numbers it would be possible to have a one bit in all eight positions which is well within the drive source capabilities.

The buffer output is sense amplified using two transistors per bit line and converted to pulses with a V.P. block. The conversion is for logical reasons and finally the information pulses would set output transistor triggers directly to convert to levels for system compatibility.

It is significant to note here that due to the sequential nature of core logic most gating problems are eliminated. Core logic cards can also be reset simultaneously throughout the machine by blocking the A and B sync. pulses while all other drive pulses continue to drive in the normal manner. This technique might be applied on a machine reset operation.

LOGIC TRANSISTOR REQUIREMENTS

To achieve system compatibility, all input and output lines required will have to be D.C. levels. Certain other functions will use transistors as a matter of convenience or economy i.e., reserve for computer, control, etc. The investigation shows a need for 164 logic transistors and 32 power transistors or a total count of 196. The requirements are as follows:

	Triggers (6 XSTRS each)	I/O Lines Power (2 XSTRS each)	Sense Amp. (2 XSTRS each)
Output Register	8	8	
Parity	1	1	
Error	1	1	
Overall Parity	1		
E.O.M.	1	1	
E.O.F.	1	1	
Reserve for Comp.	1		
Control	1		
Read	1		
Write (Byte Count)	1		
Byte	1		
Feed	1	1	
Service Request	1	1	
Cancel	1	1	
Not Ready	1	1	
Matrix Output			16
	22	16	16

POWER TRANSISTOR DRIVERS

It is imperative that the core logic be driven by solid state devices to fully realize the inherent high reliability of such a union and to keep the number of power supplies to a minimum. At best, the driver requirements are severe since the fast switching times of the multiple turn connectives induce a high back voltage. The back voltage generated limits the number of logical cores that can be switched simultaneously by a given driver.

Another factor to consider is current regulation. The drivers will be looking into variable impedance loads each machine cycle. Consider a driver which feeds a number of cores, any, all, or none of which may be switched on any given base machine cycle. It is therefore self evident that regulation as well as back voltage will restrict the number of cores that may be driven by a single driver.

To ease the driver duty cycle the base machine cycle should be made as long as possible. Since the logic is sequential, it may well be possible to predict a driver load for any given cycle and through proper drive current distribution a more nearly balanced load impedance can be achieved. The technique of current distribution might require grouping of certain logical blocks in a given pluggable unit or have a more elaborate current distribution system on the back panel.

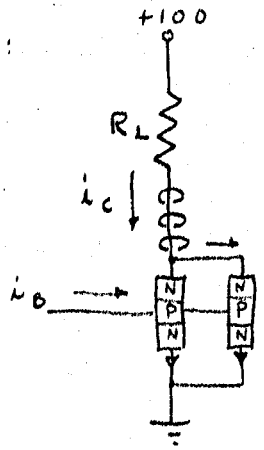
Some logical blocks will switch to one every cycle and represent a fixed load. By design the logical blocks which represent a fixed load are not widely used functions. They are the Not And, Not Or, and the Inverter.

The following calculations are indicative of the number of logical cores that could be driven in series (max. back voltage) using drift power transistors. The power dissipation is based on a 12.5 us duty cycle.

DRIVER	TURNS	RISE	DUR.	AMP.	BACK E (SW)	(NOT SW)	REG.
A, B	3	.35	1.8	1.7	1.98	0.6	+25% -0
SA, SB	5	.35	.9	2.0	3.5	2.0	+25% -0
RA, RB	2	.5	4.5	1.25	0.2	0	±10%

DIRECT TRANSISTOR DRIVE

A, B DRIVER:



REG = .25 $\quad .25 \times 100 = 25$ VOLTS

$R_L = \frac{100-25}{1.7} = 44\,\Omega$

NO. CORES $= \frac{25}{1.98} = \underline{12}$

$i_c = .85$ PER TRANS.

$V_c = 6V. \quad P = 6 \times .85 = 5.1$

DUTY FACTOR $= \frac{1.8}{12.5} \quad P = \frac{5.1 \times 1.8}{12.5} = \underline{.74}$ WATT

(IN FREON)

SA, SB DRIVER: CKT. SIMILAR TO ABOVE.

REG. = .25 $\quad .25 \times 100 = 25 \quad R_L = \frac{75}{2} = 37.5\,\Omega$

NO. CORES $= \frac{25}{3.5} = \underline{7} \quad i_c = 1$ PER TRANS.

$V_c = 6 \quad P = 6 \quad$ DUTY FACTOR $= \frac{.9}{12.5}$

$P = \frac{.9}{12.5} \times 6 = \underline{.43}$ WATT (IN AIR)

RA, RB REG = .1 $\quad .10 \times 100 = 10$ V. $\quad R_L = \frac{90}{1.25} = 72\,\Omega$

NO. CORES $= \frac{10}{.2} = \underline{50} \quad P = \frac{4.5}{12.5} \times 6 \times .6 = \underline{1.3}$ WATT

(IN FREON)

If a duty cycle of 20 u s were chosen, the power dissipation would break down as follows:

A, B	Driver	.457	watts	(in air)
SA, SB	Driver	.27	watts	(in air)
RA, RB (2 in parallel)	Driver	.41	watts each	(in air)

The present estimates of heat dissipation for drift transistors with a copper sink is from 200-500 milliwatts in air and from 2-4 watts in freon. Since transistors submerged in freon may hold the key to power dissipation, an investigation into a self contained device of transistor, freon, and an appropriate radiator should be conducted. Such a device would have to cycle the freon between the liquid and a gaseous states, be physically small, and should be potentially economical.

Clock, Waveform Generator, and W. F. Switch

The basic machine cycle waveforms will be generated by a crystal controlled clock. The proposed clock would require approximately 50 transistors and 12 power transistors. The waveform switch to operate logic at speeds other than the base machine cycle speed requires approximately 15 transistors and 4 power transistors.

SUMMARY

Advantages

1. All known factors concerning core logic points to very high reliability.
2. At the present state of development, the upper limit on speed of operation exceeds the requirements for a 1,000 c.p.m. reader.
3. Logical cores can be used as buffer switch cores. (No separate drivers.)
4. Each logical function is mounted on a separate card. (Unit package.)
5. A logical card is easy to bench test before assembly in a 48 card pluggable unit.
6. The proposed reader would require approximately 444 core logic cards or eight pluggable units. (A package approximately 12" high, 81/2" wide and 8" long.)
7. The demand on transistors is low. (Approximately 229 transistors and 48 power transistors excluding the drivers.)

8. Parallel paths of logic can run at different speeds. (Saves transfer connectives.)

9. Pulse logic can set output triggers directly. (Pulse to voltage conversion.)

10. The sequential nature of core logic eliminates most gating problems.

11. Two transfer functions can be placed on a single card. (Transfer is the most widely used connective in core logic.)

12. A faulty logical card can be replaced as a unit.

13. The gain within a logical connective is greater than one eliminating the need for amplifiers.

14. Core logic is easily machine reset. (Block SA, SB drive pulses.)

15. The signal to noise ratio is 20:1.

Disadvantages

1. Current driver requirements are severe due to the high back voltage per card and also regulation considerations. Chart for 20 us duty cycle.

Driver	Power (watts)	Regulation	No. of cores driven
A, B	.457	25%	12
SA, SB	.270	25%	7
RA, RB (2 in parallel)	.410 each	10%	50

2. Logical speeds other than the base machine cycle requires a separate "A" driver.

3. Branching is limited to three outputs per card. (One output is used for feedback in dynamic trigger circuits.)

4. For compatibility reasons, voltage to pulse and pulse to voltage conversions must be made.

5. To correct phase relationships in parallel paths of logic, the transfer function must be used.

6. A high initial access time must be expected.

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