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COMPANY CONFIDENTIAL

August 5, 1957

Exchange Memo No. 21

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SUBJECT: High Speed Disk Storage - Definition for Stretch Project

1.0 General

1.1 Purpose

This memo is intended as an elaboration and minor revision of the Proposal by Mr. P. Howard dated April 11, 1957. By this means, it is hoped that the physical machine can be described in functional terms in enough detail so that the development responsibility for each part of the machine can be assigned. It is not intended that this definition will be final or complete, particularly in the High Speed Exchange area, but will serve as a guide until a more complete definition can be made.

1.2 Objectives

The Ultra Fast Disc Unit for the Stretch Machine will provide for rapid transmission of large quantities of data to and from the main memory. Data can be transmitted to and from memory simultaneously at the rate of 8 microseconds per word in each direction. The data will be addressable in blocks of 1024 words each. An entire file of data blocks may be transmitted consecutively by means of a single instruction from the computer.

1.3 Development

The Disk machine for purposes of development responsibility can be described as consisting of 3 parts as shown in Figure 1 and 2 attached. The High Speed Disk Files and the Disk Control will physically be packaged as one unit but development responsibility for the former would rest with the San Jose Development Laboratory. The Disk Control and the

High Speed Exchange design and development would be done in Poughkeepsie because of the need for close coordination with the rest of the Stretch Project. The High Speed Exchange will be physically separate from the Disc Unit in order to provide for the accommodation of High Speed Tape Storage Unit (s) which will have a comparable information rate. The necessary control lines and data flow between these 3 parts are indicated in Figure 1 and 2.

1.4 Addressing

The 4096 Blocks of information are logically divided into two 2048 Block files. The 11 required address bits are transmitted to the Disk Control Unit during a LOCATE operation over 11 of the 20 Control Info lines. Whether reading or writing is done at this location depends upon the I/O address of the subsequent READ or WRITE instruction.

1.5 Data Flow

Data Flow will occur along 2 separate channels in order to provide for simultaneous read and write. Data will be transferred between the H.S. Exchange and Main Storage in 72 bit words. Data between the H. S. Disk Unit and the H. S. Exchange will be moved in 19 bit Bytes which will include a 1 bit parity check.

1.6 Instructions

The planned machine vocabulary includes READ, WRITE, LOCATE, CONTROL and DISCONNECT. The individual instructions are described in paragraph 2.

1.7 Controls

Writing will be controlled by a Write Pulse Generator located in the Disk Control. Reading will be done under control of 19 so called self clocked circuits in order to realize the high bit packing required by the information rate. The necessary synchronizing control lines are described in paragraph 2.

1.8 Checking

The 72 bit data word from Main Storage includes 64 bits of information and 8 check bits. By means of these check bits, single

errors may be not only detected but corrected during the reading operation. This will be done as the word is being transferred to Main Storage. In addition, as each 18 bit byte is sent to the Write Amplifiers, a parity bit is added and recorded on the disk. This parity is checked during the reading operation and any odd number of bit errors detected. The computer will be notified that an uncorrectable Data Word Error has been detected. Consideration is also being given to a horizontal parity check (as distinguished from vertical parity above) as a preferred alternative to an "echo" check of the write amplifier output. In order to be equivalent, it would necessarily take place shortly after writing a block of words and would require a R/W head with a separate write and read probe. These must be physically spaced so that reading could take place less than 50 words after writing. The bit count of each of the 19 information paths would be recorded at the write amplifier station as the bits are written and compared with the count obtained by means of the read probe. Thus a check of the written record would be available before starting to write the succeeding block.

2.0 The planned Instructions and Control Lines are described in the following paragraphs:

2.1 Locate

This instruction, as it comes from the computer, consists of a 1 bit command, a 9 bit I/O address, and an 11 bit block address. The decoded I/O address will direct the block address to the proper file address circuitry. While the addressed file is locating the block indicated, the H. S. Exchange will reject a second locate instruction directed to this same file. As soon as the particular block is located, a synchronizing pulse will be sent to the H. S. Exchange signalling that a read or write operation could begin. This pulse will be repeated each disk revolution as the addressed block is reached until a read or write operation begins. Sequential stepping from track to track will take place when and if the word count of the related control word requires it.

2.2 Read

The instruction consists of a 1 bit command, 9 bit I/O address and a 20 bit Control Word address. As soon as the control word has been obtained from Main Storage and registered in the H. S. Exchange a Read Status signal will be sent to the Disk Control Unit. Coincidence between this signal and the address located signal described above will cause reading to commence. A word will be assembled in the H. S. Exchange and sent to Main Storage as soon as 4 bytes have arrived from the Disk Unit and access to Main Storage can be obtained. This process continues until the word count in the control word equals the Words Read count at which time an End of Message signal will be sent to the Computer. For a description of read clocking, de-skewing, and parity checking refer to the description in sections 3.0, 4.0 and 5.0 below.

2.3 Write

Similar to the Read instruction. After obtaining the Control word and synchronizing with the Disk, writing will be under the control of a Write Pulse Generator and the Words Written Counter. At the end of each 1024 words, writing will be suspended until the next Block Mark is reached. End of Message is handled in the same manner but with separate comparing and counting circuits in order to allow simultaneous read and write.

2.4 Control

This instruction will have a 1 bit command, 9 bit I/O address, and 20 bits of instruction to be transmitted to the I/O device addressed. In the case of the 2 Disk Files these 20 bits will have the following formats.

1. Write File Protect (2 bits), Start Block Address (11 bits), Block count (7 bits).

2. Erase File Protect (2 bits), Start Block Address (11 bits), Block Count (7 bits).

3. Turn on RESERVED light (2 bits).

4. Turn off RESERVED light (2 bits).

The File Protect operation causes a protect bit to be written at the beginning of the block addressed on a 20th information path. Write File Protect would continue until the Block Count is reduced to zero. A subsequent Write operation would be suspended upon detection of a F.P. bit and the Computer so notified. Thus a maximum of 128 consecutive blocks could be protected with one Control Instruction. The "Turn on RESERVED Light" control instruction would set a trigger and turn on a "RESERVED" signal light on the control panel of the Disk Unit and would indicate that the unit was not to be taken off line.

2.5 Disconnect

This instruction will consist of a 1 bit command and a 9 bit I/O address and would place under program control the termination of a READ, WRITE, or CONTROL operation.

2.6 Control Lines

File I (II) Address Located -

This line will come up as soon as the track and block addressed is located. This will not be a continuous signal but would come up on a pulse basis once each disk revolution as the beginning of the addressed block passes the R/W heads.

Ready

This will be a continuous signal when the disks are up to speed, no fuses are blown, and the disk Unit is in readiness to receive instructions and function as instructed.

Shift Access Unit

This line will come up once each disk revolution as a pulse and will signal the beginning of the 1st block.

Block Mark

This line will come up 4 times each revolution signalling the beginning of each of the 4 blocks. The resulting pulses, will be separated by 90^{o} in time.

File I (II) Read (Write)

These 4 lines will control the information switches located between the R/W heads and the Read and Write amplifiers.

File I (II) Busy

These two lines will be steady state up when the respective file is executing an instruction that would obviate its accepting another except on a hold basis.

Read (Write) Control

These two lines will be up when the disk unit is actually engaged in sending (or receiving) bytes to (from) the H.S. Exchange for assembly (disassembly) into words. These lines would not be up, for instance, in the small interval between blocks.

Read (Write) Status

These two lines would be steady state up from the time a control word is registered in the H.S. Exchange until an End of Message condition is reached.

Read (Write) End of Message

These two lines will come up as soon as the Words Read (Written) Counter equals the Word Count of the Control Word. These lines when associated with the proper I/O address will signal the computer that the particular operation is completed.

(Additional control lines between the H.S. Exchange and the Main Storage or the Computer are not described herein but will be covered in a later memo.)

3.0 High Speed Disk Files

3.1 Specifications

1.	Number of disks	40
2.	Disk spacing	0.3 in
3.	Disk size	24 in
4.	Tracks per inch	50
5.	Tracks per side	256
6.	Speed	1800 r.p.m.
7.	Maximum access time	100 m.s.
8.	Track to track access time	33 m.s. (max)
9.	Bit Rate	2 us

Since these specifications are intended as a guide, minor changes may be made in the interest of standardization.

3.2 Data Organization

The 72 bit word from the main memory consists of 64 data bits and 8 error correction code bits. This 72 bit word is recorded serially in 4-18 parallel bit bytes. In order to provide for proper operation of the self clocking oscillators when a long series of zeros or ones is recorded in any one track a synchronizing byte will be recorded after every two words. Information will be recorded in blocks of 1024 data words. A small gap of approximately 50 bits will be left between blocks. There will be 4 blocks per track. A summary of information concerning data organization is tabulated below.

Bits/track/word	4 bits
Words/block	1024 words
Synchronizing bits/block	512 bits
Inter-block gap	50 bits
Bits per inch	466 bpi
Bits per second	559,000 bps
Addressable locations	4096 blocks
Disk Unit capacity	4,192,304 words

3.3 Logical Division

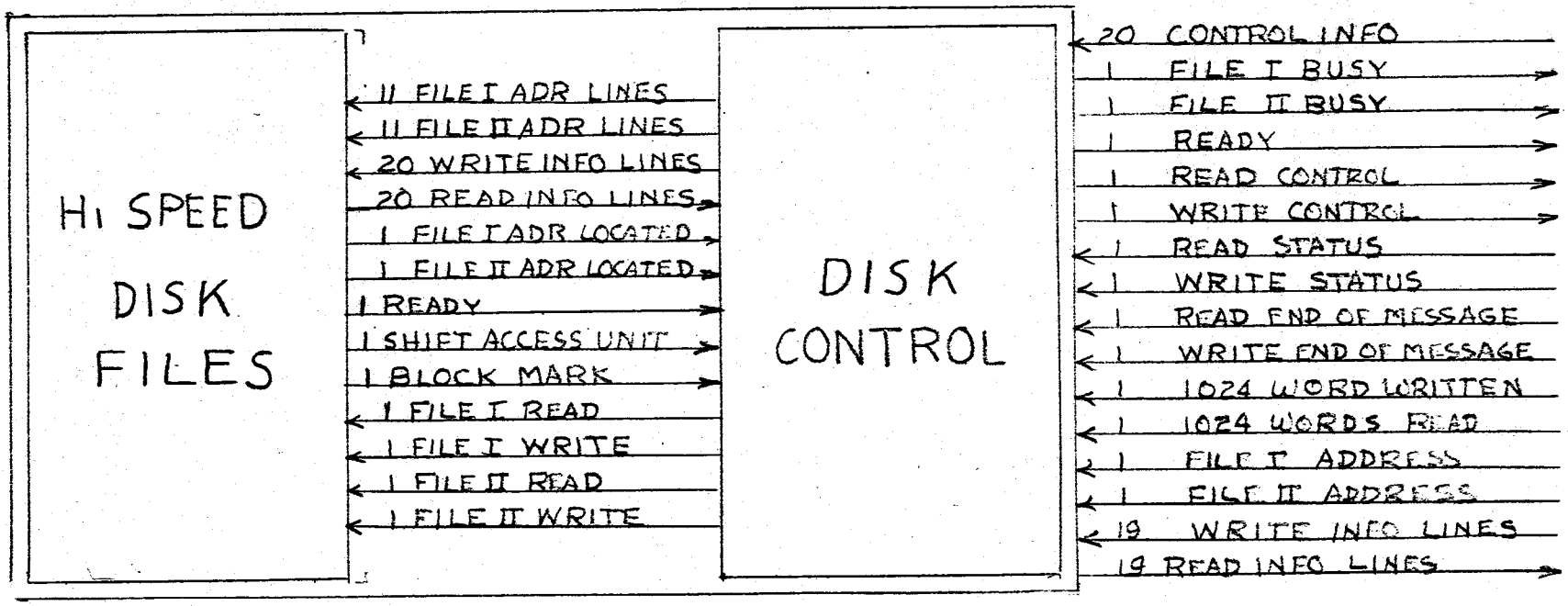
a. Two Files

Two logically independent files should be provided to allow simultaneous read and write operation.

b. Four Access Unit

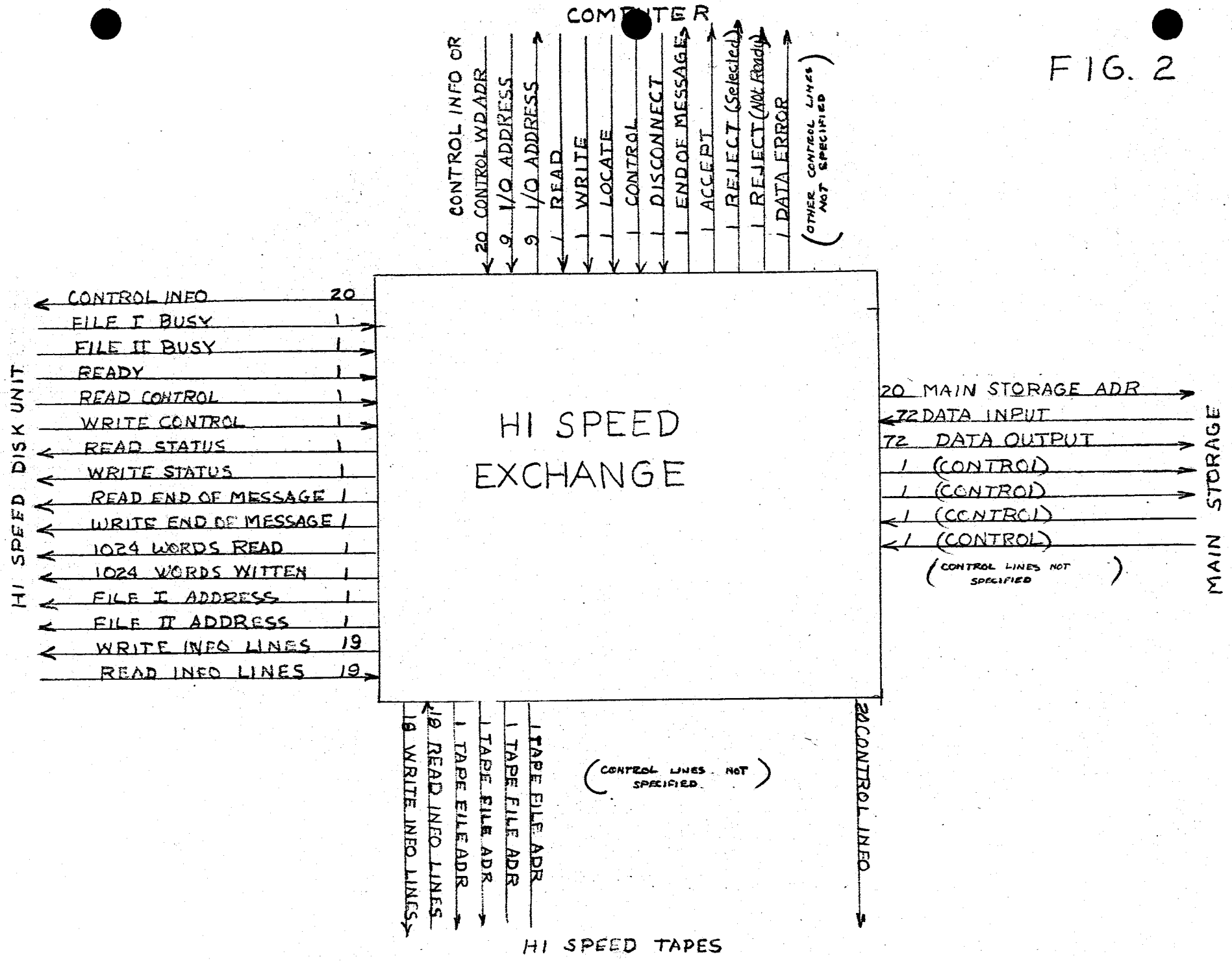
Two access units are to be used per file. The A unit is to position a set of read/write heads to even tracks, while the B

FIG 1



HI SPEED DISK UNIT

FIG. 2


COMPUTER
CONTROL INFO OR
20 CONTROL WD ADR
6 I/O ADDRESS
9 I/O ADDRESS
1 READ
1 WRITE
1 LOCATE
1 CONTROL
1 DISCONNECT
1 END OF MESSAGE
1 ACCEPT
1 REJECT (Selected)
1 REJECT (Not Ready)
1 DATA ERROR
(OTHER CONTROL LINES NOT SPECIFIED)
HI SPEED DISK UNIT
CONTROL INFO 20
FILE I BUSY 1
FILE II BUSY 1
READY 1
READ CONTROL 1
WRITE CONTROL 1
READ STATUS 1
WRITE STATUS 1
READ END OF MESSAGE 1
WRITE END OF MESSAGE 1
1024 WORDS READ 1
1024 WORDS WITTEN 1
FILE I ADDRESS 1
FILE II ADDRESS 1
WRITE INFO LINES 19
READ INFO LINES 19
HI SPEED EXCHANGE
20 MAIN STORAGE ADR
72 DATA INPUT
72 DATA OUTPUT
1 (CONTROL)
1 (CONTROL)
1 (CONTROL)
1 (CONTROL)
(CONTROL LINES NOT SPECIFIED)
MAIN STORAGE
1 TAPE FILE ADR
1 TAPE FILE ADR
1 TAPE FILE ADR
12 READ INFO LINES
18 WRITE INFO LINES
(CONTROL LINES NOT SPECIFIED)
24 CONTROL INFO
HI SPEED TAPES

access unit handles the odd tracks. When the A heads are reading (writing) the B access unit positions it heads to the succeeding track so that the information flow may be switched from the A heads to the B heads at the beginning of the next track.

3.4 Block Marks

The disk files are to be divided vertically into four quadrants. This division is to be accomplished by means of 4 marks arbitrarily assigned the names of Block Mark I, Block Mark II, etc. Block Mark I has the further significance of indicating the beginning of a track, and is used to produce the Shift Access Pulse discussed below.

3.5 Access Registers

Associated with each access unit is an access register which stores the initial track and block address during a locate instruction During a read or write operation /this register stores only the track address since the track advance signal is derived from the Block Mark I pulse which precludes the need for block information. During a locate operation the output of the access register in conjunction with a checking emitter and comparator, signals Disk Control by means of either the File I Address Located line or the File II Address Located line, that the file is properly positioned at the correct address.

3.6 Data Flow

Data flow to and from the disks takes place on a nineteen or twenty bit basis. Eighteen of these bits are actual data, the 19th is a redundancy bit, while the 20th occurs once each block if it is desired to protect the block against accidental over writing.

3.7 Information Switch

Since simultaneous reading from and writing on disks is to occur, one data path is provided for reading and one data path is provided for writing. Each path consists of 20 information lines which are connected to the disk file by means of an information switch. The information switch in turn gates the write lines to the file which is supposed to be written on and the read lines to the file which is to be read from. The switch is under control of the file read/write lines developed in the Disk Control Unit.

IV Disk Control

4.1 Disk Control contains all circuitry necessary to control the disk Files which cannot be shared with the High Speed Tape.

4.2 Since Disk Control contains a group of functionally independent logical blocks which cannot be described as a unit, each block will be named and described as follows:

4.3 Oscillator and Clock Pulse Generator

The fundamental timing source of the Disk Unit, and H.S. Exchange.

4.4 Write Control Circuits

Information is stored on the disks in the form of 1024 word blocks, four blocks to the track, and 256 tracks to the side. In order to begin to write in a given track a signal must be obtained from the disk Files indicating that the write heads are located at the correct track and that the correct block has been reached. Furthermore the High Speed Exchange must signal that it is in Write Status. When these two conditions are obtained in coincidence writing begins.

Seventy-two bit words from memory are disassembled into bytes in the High Speed Exchange where a parity bit is generated and added to the byte. This 19 bit byte is transmitted to the disks.

In order to be able to use the self-clocking circuits described below one byte of sync bits is written every two words. When 1024 words have been counted by the Write Word Counter, located in the High Speed Exchange, a signal is sent to the Write Control Circuits which stops writing. Writing begins again when the next block mark is sensed. Data continues to be written block by block until an End of Message situation exists. At that time the Write Status condition is terminated and writing stops.

4.5 Read Control Circuits

The Read Control Circuits areso similar to the Write Control Circuits that only the differences between the two will be pointed out.

When reading; sync bits are read as ordinary data and are not eliminated until transmission between the Disk Control Unit and the High Speed Exchange occurs.

While data written on the disks can be timed by means of an external clock, the amount of skew existing, and the desired bit packing prohibit the use of an external clock for timing read. Therefore,

self-clocking circuitry and a de-skewing register are required. These are described in the next paragraph.

4.6 Self-Clocking Read Circuits

These circuits are divided into two parts.

1. Two oscillator- pulse generator circuits per bit position which are used in conjunction with a counter to provide necessary gating when information bits are absent.

2. A Skew Register capable of storing a sufficient number of bytes to insure that all bits of a byte are present before the byte is transferred to the Byte to Word Converter in the High Speed Exchange. Sync bits are necessary because a large number of zeros may occur in a given bit position of a data path.

4.7 File I (II) Track Advance Circuits

Section 3 of this memo contains a discussion of the need for two access registers and two access units per file. As pointed out in that section the Disk Unit must read or write continuously, so some means of alternately advancing each track access mechanism must be used. The circuits to advance the access mechanisms are located in the Disk Control Unit and functions as follows:

The Shift Access Unit pulse, in addition to switching the read/write heads, is used once every other revolution of the discs to increase the address stored in two registers, named File I Track Register and File II Track Register, by one. The new addresses, thus obtained, are transferred to the proper access Registers and the registers in turn signal the access mechanisms to seek the new addresses.

4.8 Locate Control Circuits

When a Locate instruction is received by the H.S. Exchange that instruction is accepted or rejected depending on the condition of a Busy Register. A file is considered busy so far as a Locate instruction is concerned if it is in the process of reading or writing or has received a previous Locate instruction which has not been completed. Providing the instruction is accepted, the address portion of that instruction is sent to the proper Access Registers and the locate operation begins.

When the correct track has been located, and the block address in the access registers is equal to the block address of the disk file, a signal called File I (II) Address Located is sent to the Disk Control Unit from the Disk Unit. This signal which continues to occur once each revolution, signifies that Locate is complete, and combined with the receipt of a read or write instruction for this file signals the High Speed Exchange to begin to read or write.

4.9 Busy Read or Write

When a read or write or control instruction is received, the file is considered busy only if the file is performing a read, write, or control operation, not if the file is locating.

4.10 File Protect

One bit is recorded on a separate disk for each block of information to be protected. This bit is located in time between the Block Mark, and the first byte of data. When at a later time new information is to be written at this location, the presence of the bit is sensed and will signal the High Speed Exchange that this block is protected. Depending on the instruction, the High Speed Exchange may either ignore the bit or start an End of Message cycle.

V High Speed Exchange

The High Speed Exchange contains the circuitry which can be shared by X100 Tape and High Speed Disk.

This circuitry has a fourfold function as follows:

1. To handle all instructions from the computer, reject those instructions in error, accept those that should be accepted, and channel the accepted instructions in whole or in part to the memory, the Disk Control unit, or to the Tape Control Unit.

2. To accept 72 bit control and data words from memory when writing, disassemble the words into bytes, and transmit the bytes to the proper I/O device.

3. To accept bytes from an I/O device when reading, assemble the bytes into words, and transmit the words to memory.

4. To keep track of the length of a message and terminate the operation when the correct number of words have been handled.