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Block Representation of Transistor Circuits

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The subject of representing the transistor logical circuits operating in a current mode operation by block diagrams was discussed. Those contributing to the discussion were:

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A specific logical system was laid out with two different modes of representation of the building blocks developed by the Transistor Circuit group. The evaluation of the two indicates that one form of representation can be more easily grasped and may render less difficulty in servicing the machine.

A tentative set of rules which are to be followed in using the circuits as building blocks was decided upon as a result of the discussion. Only the basic blocks are described. The basic block contains the symbol which discribes the logical operation of the circuit. The location of the circuit within the pluggable unit, the location of the pluggable unit, the production part number and any other necessary information pertaining to the location of the block are to be added to the basic block at a later time. This memo supersedes Exchange Memo 6 and 13.

Reference: Stretch Circuit Memo 3
Stretch Exchange Memo 6 and 13

I BASIC CIRCUIT

Basically, there is only one circuit configuration that performs a logical AND and OR operation. The circuit can be composed of transistors of either PNP or NPN type. It provides two outputs which are complement to each other. Figure (1) shows the actual circuit configuration and the relative positions of the two output terminals as they appear on a block diagram.

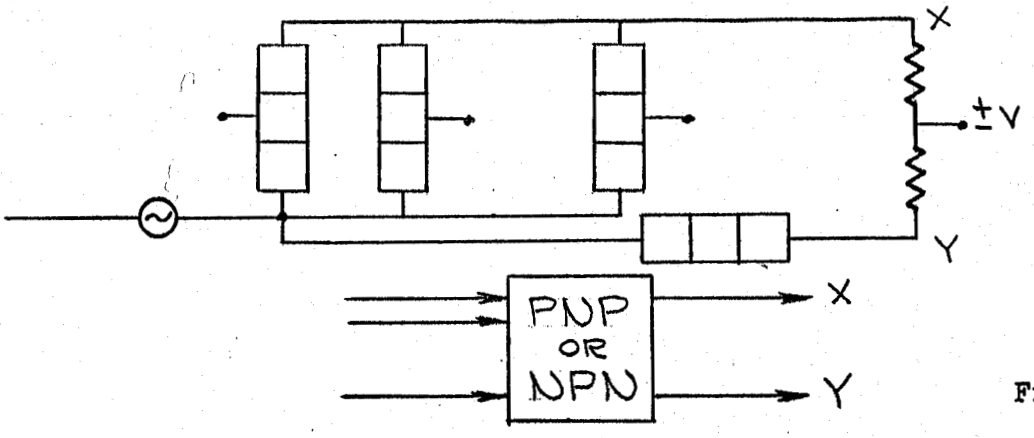


Figure 1

The inputs to one type of building block can assume either one of two levels whereas the outputs of the same type building block assume a different set of levels. The system therefore involves four levels. Depending on the definitions associated with the signal level indicative of a "logical one," the outputs of the circuit assume different logical statements of the inputs.

II A SET OF RULES

a) In conformity with the I.B.M. General Standards, transistor types are to be designated "P" (P blocks) for "NPN units and "N" (N blocks) for "PNP" units.

b) The signals that appear at the output of the two types of blocks are differentiated by symbols. The outputs of the N blocks (made of PNP transistors) are disignated with p and the outputs of the P blocks (made of NPN transistors) are disignated with n.

c) The outputs of the P blocks (n lines) can be used only to drive N blocks, whereas the outputs of the N blocks (p lines) can be used only to drive P blocks.

d) The binary signal levels on a p line differs from those on a n line.

e) All lines will be labelled as follows:

Channel Available (+ n) →

Channel Available (− n) →

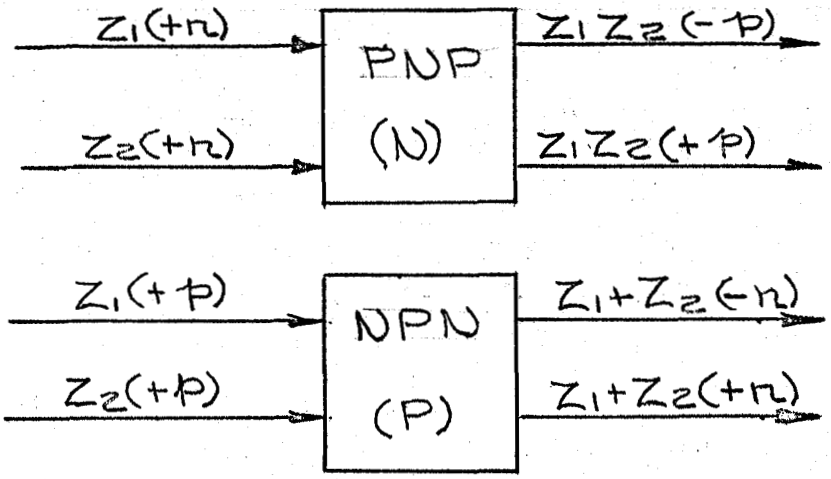
Channel Available (+ p) →

Channel Available (− p) →

The sign in front of the symbol p or n specifies the state of the line when the condition labelled on the line is satisfied. For instance, when there is a channel available, the first and third line will be at the more positive of the two values that an n or p line can assume respectively, whereas the second and fourth line will be at the more negative of the two values that an n or p line can assume respectively.

f) The definition to be adopted in the present system is that the signal on both p line and n line is a "logical one" if it is in its most positive voltage. This definition is not the same as that used in Exchange Memo 6 and 13.

g) It follows from the definition of the voltage levels that Boolean-wise, the functional relation performed by the basic circuit can be written as follows:



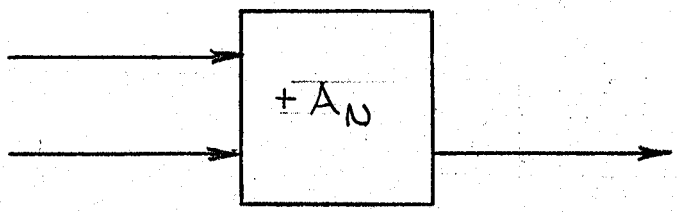
h) Each building block has two outputs that are complement to each other. The bottom output is always the in-phase output. The top output is therefore the out-of-phase output. By in-phase, it is meant that the bottom output performs the function of the inputs as specified by the symbol in the block.

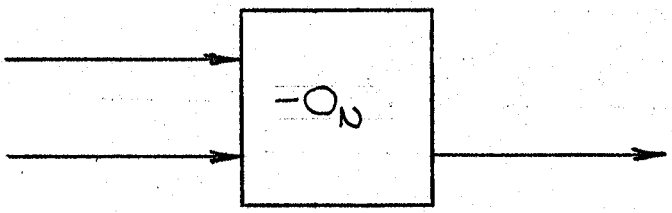
i) Unless otherwise denoted, the output of a block that has a subscript N is a p line and the output of a block that has a subscript p is a n line.

j) If Emitter Follower is to be used for powering, the load resistance of the basic logical circuit has to be changed since Emitter Follower introduces a level shift. When the load resistance is other than the standard size resistance, it will be indicated.

III BUILDING BLOCKS

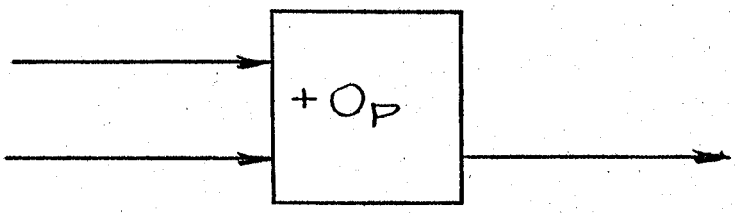
a) Positive AND or negative OR.
The basic circuit is composed of PNP transistors.
The in-phase output of the block is the "positive AND" or a "negative OR" of the inputs. Both blocks

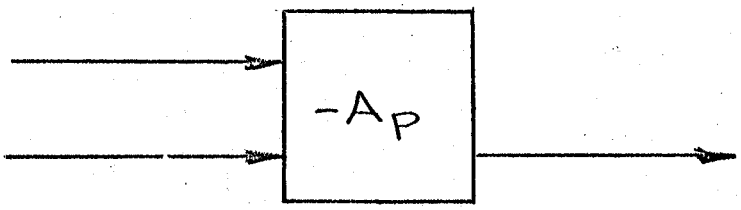




represent the same circuit and perform the same logical function. The out-of-phase output is the positive OR of the inputs if complements of the inputs are used.

b) Positive OR or Negative AND.
The basic circuit is composed of NPN transistors. The in-phase output of the block is the positive OR or a negative AND of the inputs. Both blocks represent the same circuit and perform the same logical function. The out-of-phase output is the positive AND of the inputs if complements of the inputs are used.





c) Inverter

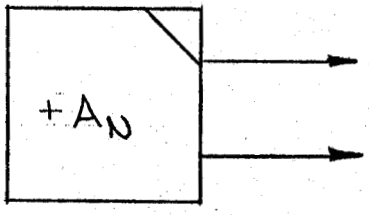
A symbol to represent an Inverter block is omitted since:

1. The complement of the signal is always available, and

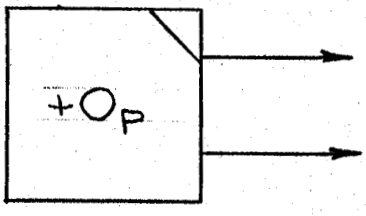
2. it is implied by taking the out-of-phase output of a single-legged AND or OR circuit.

d) Line Converter

The load circuit of basic building blocks may be modified by inserting a Zener diode with extra power supplies. A diagonal line drawn across the corner of the basic block indicates that the load circuit of the output coming from that corner has been modified. Depending on the direction of the diode and the type of power supplies, the modified load circuit converts a p line to an n line or vise versa. It does not alter the logical statement of the line. The diagonal line serves as a flag that the load circuit of the basic circuit has been modified.



This block represents that the out-of-phase output is a n line instead of a p line as adopted by the convention. The logical statement of the line remains the same.

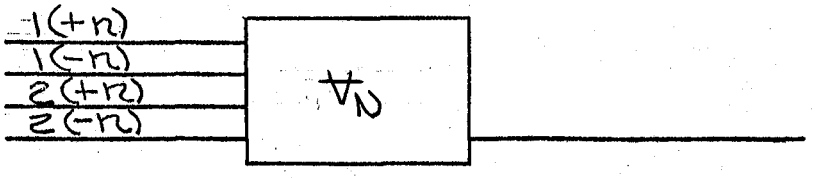


This block represents that the out-of-phase output is a p line instead of a n line as adopted by the convention. The logical statement of the line remains the same.

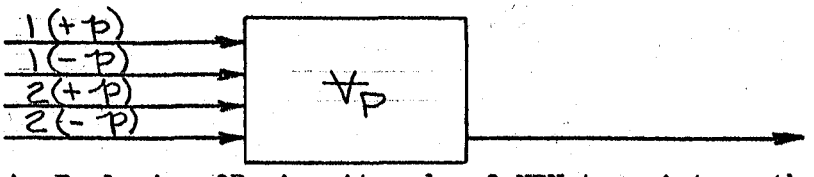
e) Exclusive OR.

The Exculsive OR circuits require both the signals and their complements be connected at its input.

e.1) Two way Exclusive OR.



An Exclusive OR circuit made of PNP transistor, the in-phase output is the Exclusive OR relation of the condition on line 1 and line 3.



An Exclusive OR circuit made of NPN transistor, the in-phase output is the Exclusive OR relation of the condition on line 1 and line 3.

e.2) M way Exclusive OR.

Circuits that can perform an Exclusive OR relation of M inputs through one block will be represented in the same way as a two way Exclusive OR with 2M input lines. The inphase output is the Exclusive OR relation of the input lines 1, 3, 5, etc.

IV FLIP-FLOPS

4.1) Flip-Flop composed of both NPN and PNP type transistors.

The actual circuit configuration and the relative positions of the output terminals as they appear on the block diagram are shown in Figure (2).

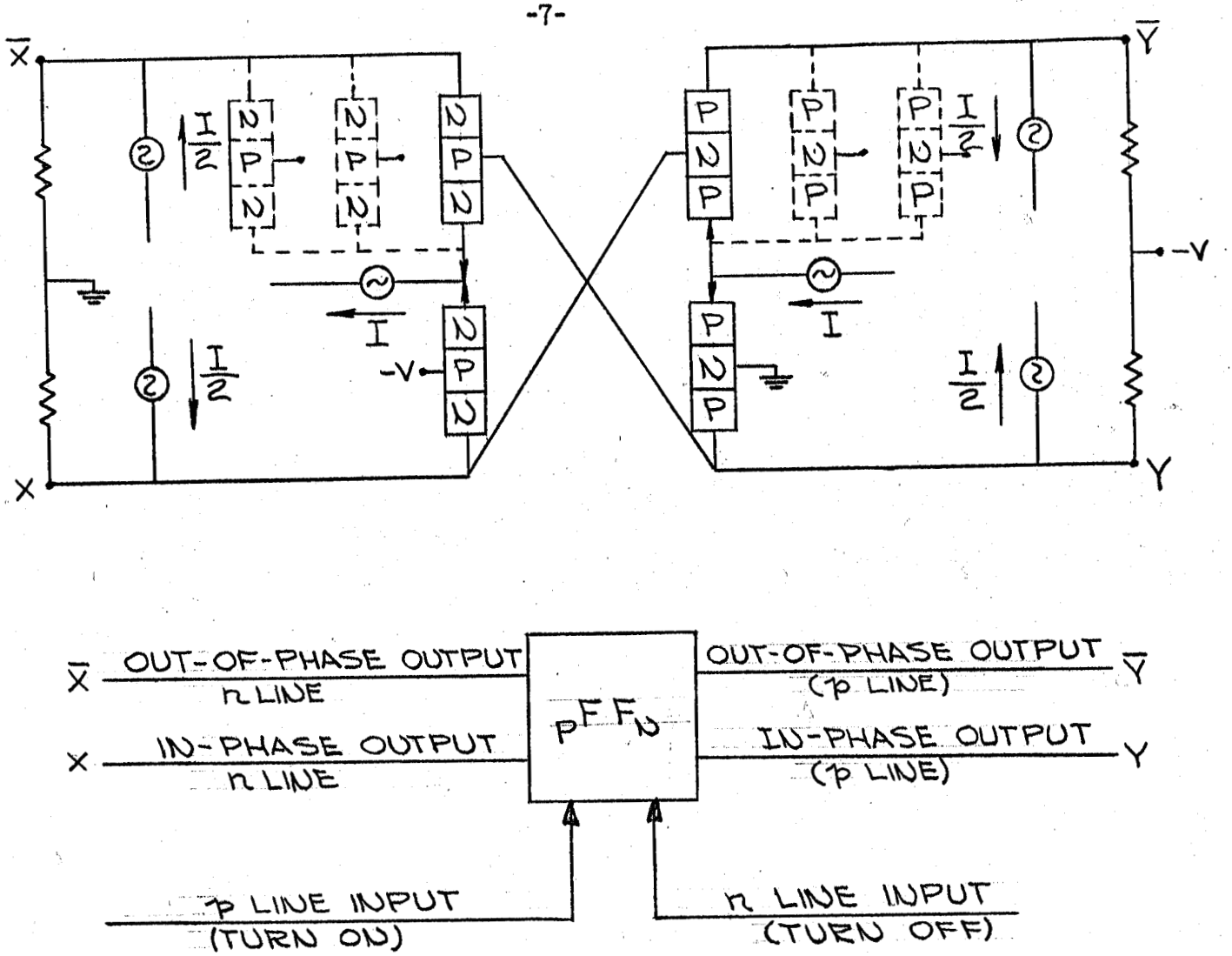


Figure 2

The rules are:

1) The bottom outputs are the in-phase output with respect to the relative position of the inputs. For instance, the bottom right hand terminal is the in-phase output of the bottom right hand input (labelled TURN OFF in Figure 2).

2) All Flip-Flops will be considered "ON" when the right hand in-phase output is at the more positive of the two values (i.e., it is at a signal level which is indicative of a "logical one.")

2A) The in-phase outputs of the Flip-Flop composed of both type of transistors carry the same logical statement.

3) A positive going signal on a p line will turn the Flip-Flop on. The p line input is normally at the negative of the two signal levels.

4) A negative going signal on a n line will turn the Flip-Flop off. The n line input is normally at the positive of the two signal levels.

5) As it has been explained in Exchange Memo 13, the parallel transistors shown dotted in Figure (2) serve as an OR function of the number of inputs.

6) To make clear the number of inputs which are to be ORED together by the input transistors, two modes of representation have been proposed.

a) Figure (3) shows the representation to which the inputs are connected to one line.

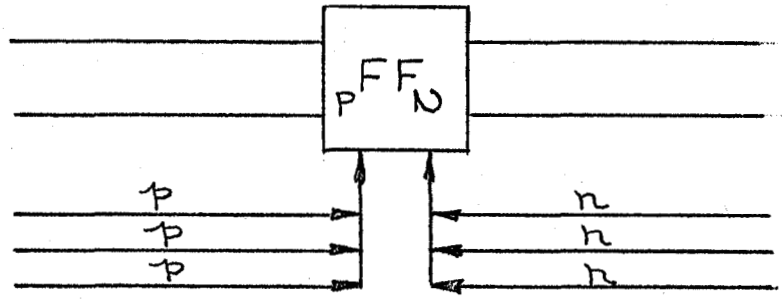


Figure 3

b) Figure (4) shows the representation to which two blocks are added for ease of drawing.

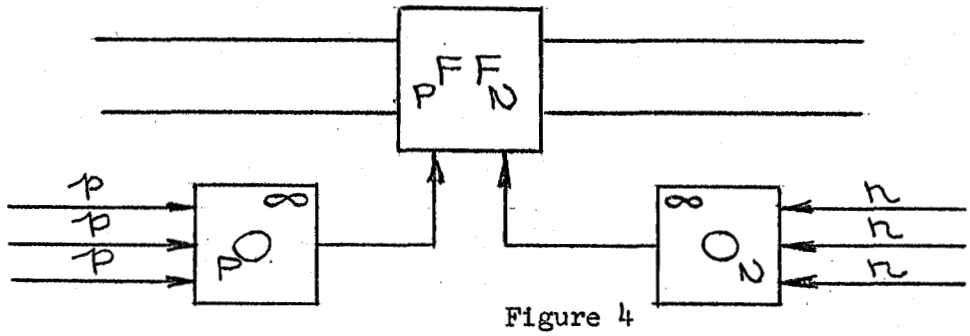


Figure 4

The two small blocks perform the function of a OR circuit for the inputs. The ∞ sign signifies that the OR block is actually part of the Flip-Flop.

Figure (3) is certainly a simple way of representing the inputs. However, a question has to be resolved before it can be adopted. The question is whether the base of the input transistor can be tied to the outputs of many blocks or if it is restricted to be driven by the output of only one block.

7) It is proposed that for Flip-Flops composed of both types of transistors, the NPN type transistors will always be drawn on the left side of a circuit diagram.

4.2) By incorporation Zener diodes and extra power supplies, Flip-Flops can be composed of either PNP type transistors or the NPN type transistors.

4.2.1.) Flip-Flop composed of PNP type transistors.

A block diagram in the form shown in Figure (6) may be used to represent the circuit shown in Figure (5)

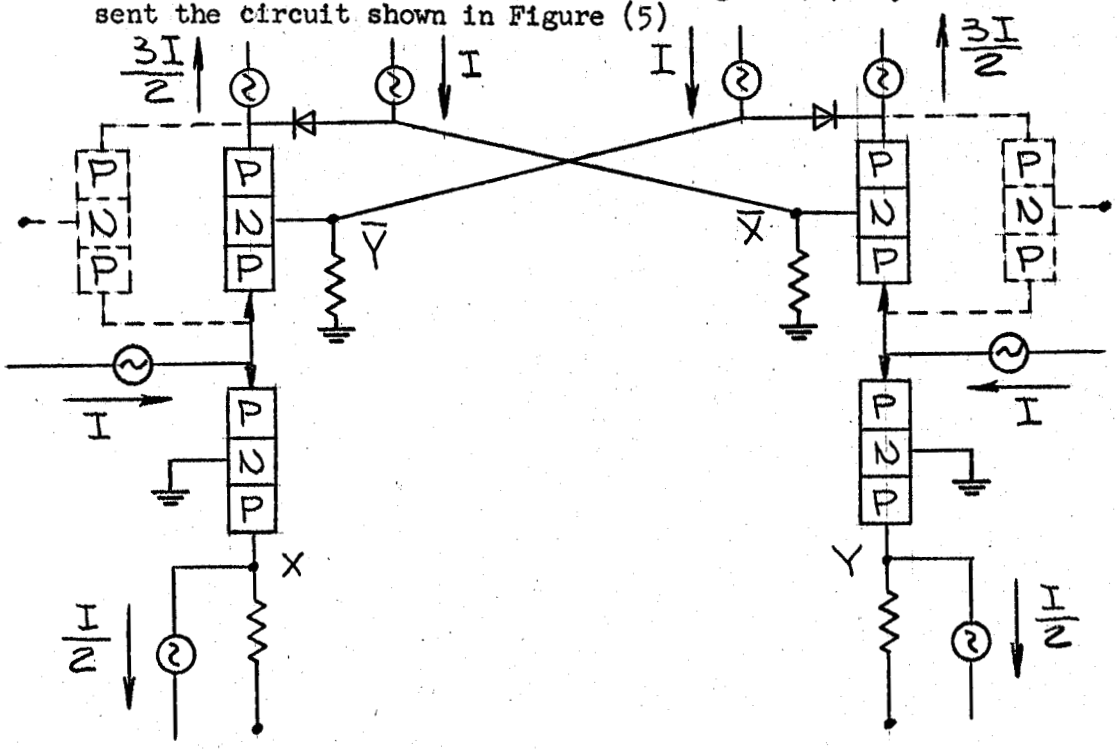


Figure 5

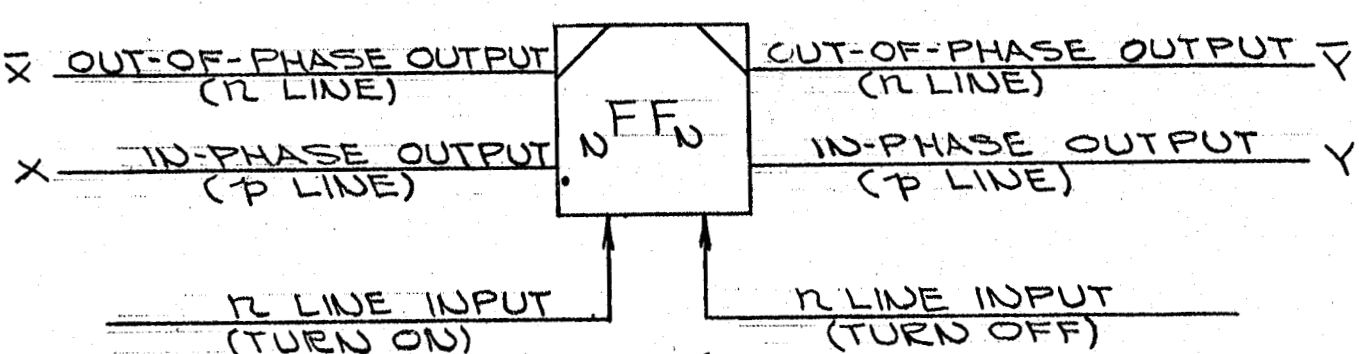


Figure 6

This block follows the same rules as the Flip-Flop that is made of both types of transistors.

1) The in-phase outputs do not carry the same logical statement.

2) The Flip-Flop is considered "ON" when the right hand in-phase output is at the more positive of the two values. (i.e., the right hand in-phase output is at a voltage signal level which is an indicative of a "logical one" on a p line.)

3) A negative going signal on the left n line input will turn the Flip-Flop on.

4) A negative going signal on the right n line input will turn the Flip-Flop off.

5) The two out-of-phase outputs will always be n lines since the load at those terminals consists of the Zener diodes.

6) The n line outputs are indicated by diagonal lines in order to follow the convention that a N block always has a p line output.

4.2.2) Flip-Flop composed of NPN type transistors.

The circuit of Figure (5) also applies to NPN type transistors by reversing the polarities of the diodes and the power supplies. It could be presented by a block diagram as shown in Figure (7).

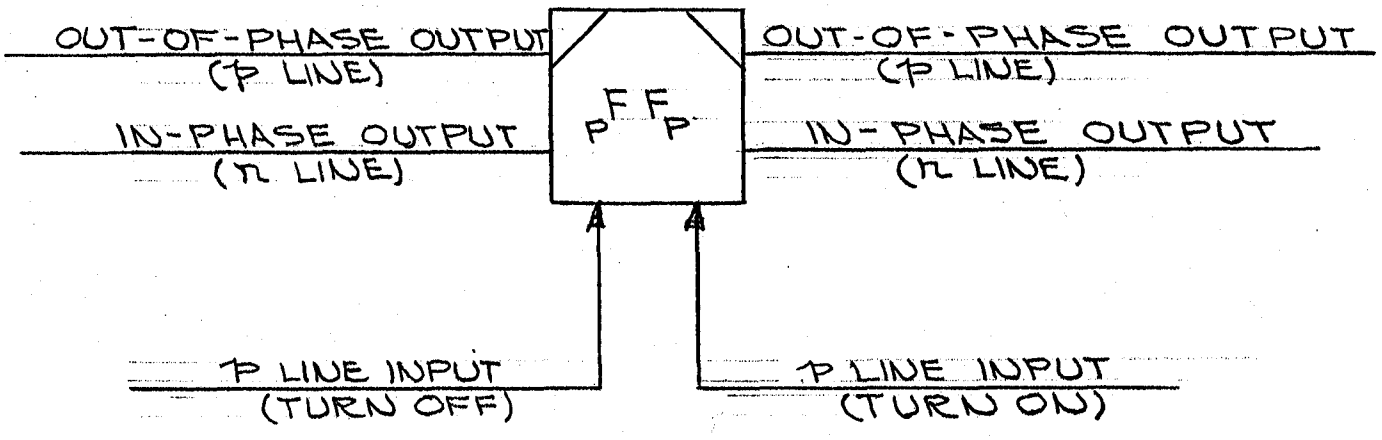


Figure 7

The rules are the same as that stated in (4.2.1) except the following:

1) In order to be consistent with the convention that the Flip-Flop is considered ON if the right in-phase output is at the more positive of the two, a positive input from the left will turn it off instead of turning it on as the previous case. This is unavoidable due to the nature of the transistor circuits.

2) A positive going pulse at right will turn the Flip-Flop ON.

3) The two out-of-phase output will always be p lines since the load at those terminals consists of the Zener diodes.

4) The two in-phase outputs do not carry the same logical statement.

4.3) In the case where the Flip-Flop is composed of both types of transistors, both in-phase outputs carry the same logical statement. The ON condition of a Flip-Flop, therefore, is also the condition that both in-phase outputs are at the signal level indicative of a "logical one".

4.4) Binary Flip-Flop

A proposed block diagram representation of a binary Flip-Flop that is composed of both types of transistors is shown in Figure (8). The characteristic of the block diagram should conform to those presented in Section 4.2.

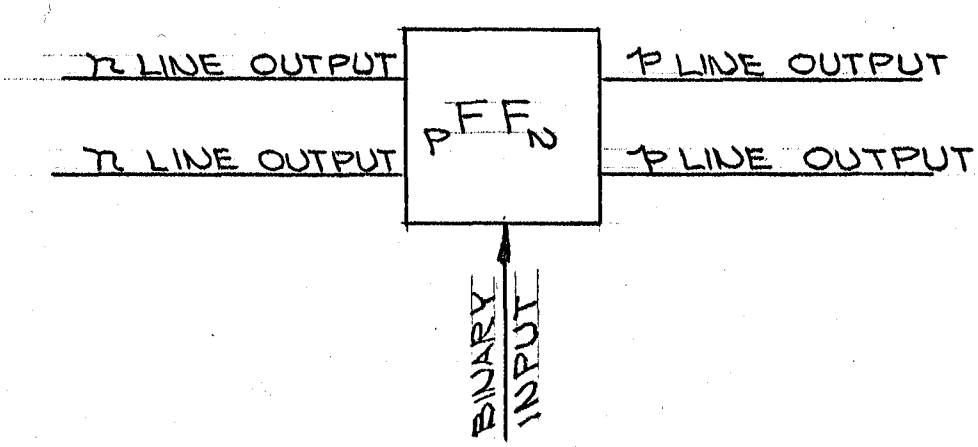
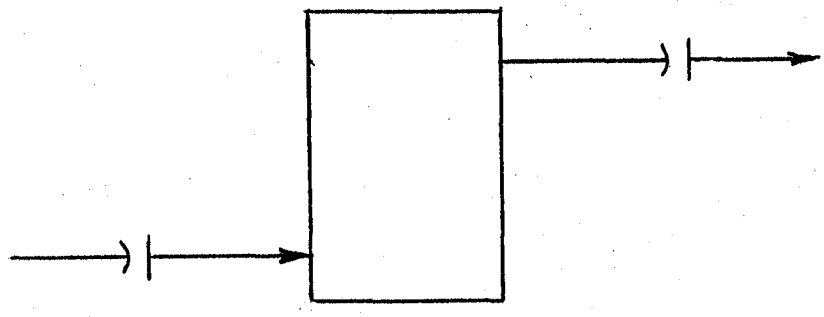


Figure 8

1) Depending on the input transistor, the binary input may be a n line or a p line.

2) The binary Flip-Flop will be considered "ON" if the right hand bottom output is at the more positive of the two signal levels. (i.e., it is at a signal level which is indicative of a "logical one").

4.4 All a.c. coupled stages will be indicated by a capacitor symbol on the input or output line.



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