

*Griffith*

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Generation of Parity Bits

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A parity bit is an even-odd count of the number of 1's contained in a group of information bits. The generation of an even parity bit (to make the total number of 1's even) is the Exclusive OR relation of all the inputs, whereas the odd parity bit is the complement of an even parity bit. Let X represent an even parity bit and  $Z_1, Z_2, \dots, Z_m$  be the information bits, then

$$X = Z_1 \vee Z_2 \vee \dots \vee Z_m$$

1) Two Way Exclusive OR

The generation of a parity bit by 2 way Exclusive OR circuits is by taking the inputs two at a time and combining the resultant outputs in the same manner and so on until the tree is narrowed down to one line. For M inputs, the generation of a parity bit requires (M-1) 2 way Exclusive OR blocks. It is reduced from the general expression given by Equation 1.

The total delay is measured by the number of logical blocks cascaded in series.  $D = \lceil \log_2 (M-\Delta M) \rceil + 1$ , where  $\Delta M$  is the smallest positive number such that  $(M-\Delta M)$  is the binary number next to M. If M is a binary number itself, then  $D = \log_2 M$ . Each 2 way

Exclusive OR circuit requires 6 transistors. A parity bit for M inputs can be formed by  $6(M-1)$  number of transistors.

## II) m Way Exclusive OR Circuit

The expression for an even or odd parity bit for m information bits consists the OR relation of  $2^{m-1}$  number of terms which are in its canonical forms. From the Truth Table, the expression can be written as  $X = H_1 + H_2 + \dots + H_{2^{m-1}}$ . Each term  $H_i$  is the AND of a combination of all the inputs. For example,  $H_1 = \bar{Z}_1 Z_2 \dots \bar{Z}_m$ . The canonical form implies that if any one of the terms is equal to 1, the remaining ones are to be 0. If  $H_j = 1$ , then  $H_i = 0$ . (for  $i = 1, 2, \dots, 2^{m-1}$ , but  $i \neq j$ ).

It is theoretically possible to construct an m way. Exclusive OR Circuit so that the parity bit for m inputs can be generated in one logical block delay. (The synthesis of net works for orthogonal expressions is discussed in a Memo by P. Halpern) The sketch of the circuit is shown in Figure 1.

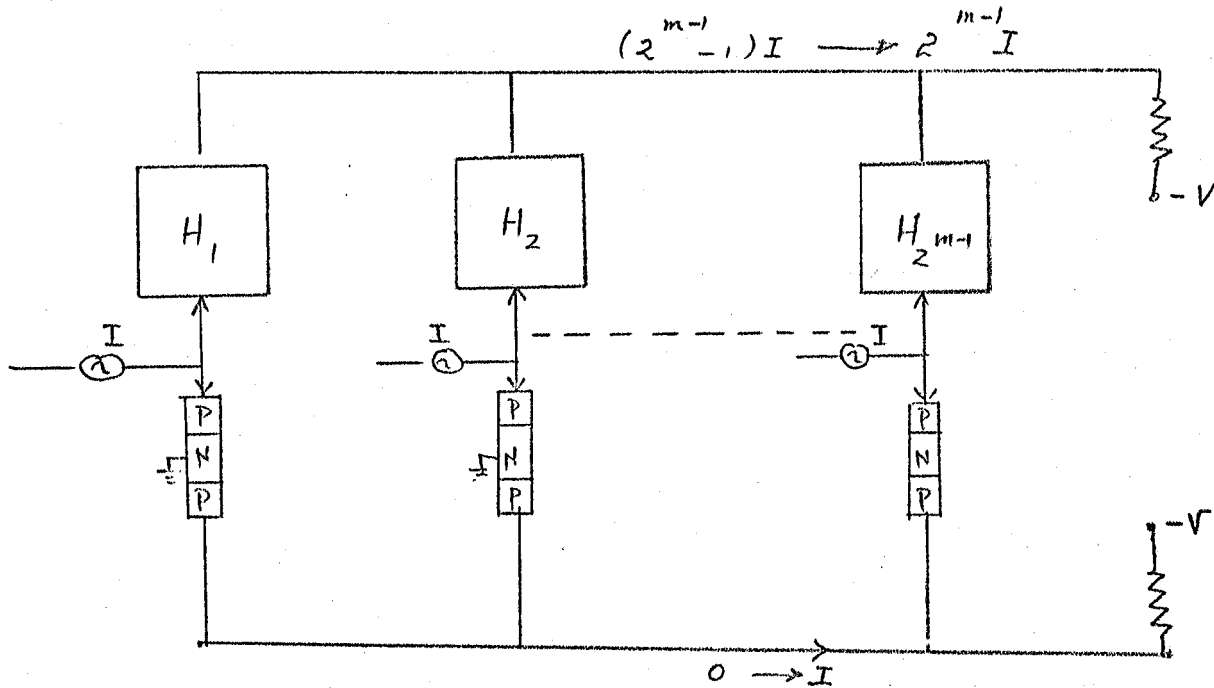


Fig. 1

With the above connection, none or at most, only one of the many bottom transistors will be in conduction. If  $H_i = 1$ , then the conducting transistor is that one associated with  $H_i$ .

Each  $H_i$  box consists of  $m$  parallel transistors. The actual connection at the  $m$  terminals requires that the complement of each literal appearing in  $H_i$  be connected. This is necessary since when  $H_i = 1$ , each literal appearing in  $H_i$  is also equal to 1, but all the complements of each literal are equal to 0. The actual connection, therefore, switches the current to the bottom transistor associated with  $H_i$ . For example, if  $H_i = Z_1 \bar{Z}_2 = 1$ , then  $\bar{Z}_1 = Z_2 = 0$ .

The following properties are observed:

- 1).  $m = \text{odd}$ . The expression resulting by complementing each literal but not the connectives from the expression for an even parity bit is the statement for an odd parity bit and vice versa. It is also the complement of the overall expression.

For example, given 3 inputs  $Z_1$ ,  $Z_2$ , and  $Z_3$ .

$$\text{Even parity} = \bar{Z}_1 Z_2 \bar{Z}_3 + Z_1 \bar{Z}_2 \bar{Z}_3 + Z_1 Z_2 Z_3 + \bar{Z}_1 \bar{Z}_2 Z_3$$

$$\text{Odd Parity} = Z_1 \bar{Z}_2 Z_3 + \bar{Z}_1 Z_2 Z_3 + \bar{Z}_1 \bar{Z}_2 \bar{Z}_3 + Z_1 Z_2 \bar{Z}_3$$

2.  $m = \text{even}$ . For each term  $H_i$  in the expression, there is always another term which is identical in form with the given term, but with each literal complemented. For example, with  $m = 2$  and inputs  $Z_1$  and  $Z_2$ .

$$\text{Even parity} = \bar{Z}_1 Z_2 + \bar{Z}_2 Z_1$$

$\bar{Z}_2 Z_1$  is the term resulting from complementing each literal in  $\bar{Z}_1 Z_2$ . It is, therefore, not necessary in the actual connection, to complement each literal since the resulting term is part of the overall expression.

To Exclusive OR  $m$  inputs through one logical block, there will be  $2^{m-1}$  number of H's, each one of which consists of  $m$  transistors.

By adding an extra transistor for each H, the total number of transistors required is  $(2^{m-1})(m+1)$ . It is seen that the collector of all the transistors are tied together through a common load. Furthermore, each current source at the emitter sees  $(m+1)$  transistors. The inherent limitations of the transistor restricts the number of transistors to be connected in parallel at the collector.

In practice a 3 or 4 way Exclusive OR Circuit may be realized. Forty transistors are required to construct a logical block for a 4 way Exclusive OR Circuit. By using three 2 way Exclusive OR circuits, the same expression can be obtained with only 18 transistors. The delays, however, are not the same. If the delays per logical block remains the same, the 4 way Exclusive OR circuits, although require more transistors, cut down the delay by sometimes a factor or two with respect to the existing 2 way Exclusive OR Circuits, according to the following equations:

The general expression for the number of logical blocks (L) required to generate a parity bit for M inputs is

$$L = \sum_{k=1}^N \frac{(M-\Delta M)}{W^k} + f(\Delta M) \quad (1)$$

where  $W$  is the maximum number of inputs per block, and  $AM$  is the smallest positive integer such that

$$M - AM = W^N \quad (2)$$

$f(AM)$  is a positive integer where

$$f(AM) = \frac{AM}{W - 1} + \epsilon \quad (3)$$

for  $0 \leq \epsilon < 1$

The number of logical blocks cascaded in series is a measure of the delay. It is given as

$$D = \left[ \log_W (M - AM) \right] + S \quad (4)$$

where  $S = 0$  if  $M$  is a power of  $W$ , and  $S = 1$  if otherwise.