J. E. Griffith

September 28, 1956

PROJECT STRETCH
LINK COMPUTER MEMO NO. 11

SUBJECT: Thoughts on Machine Organization

BY: W. A. Hunt

A study has shown the need for the concept of continuous streams of information. To handle this concept the controls of Machine Specifications #1 and #2 were advanced. Another concept of equal importance is that of juxtaposing two groups of bits to form a partial address in memory. This, together with the desirability of dividing memory into groups of bits which are powers of two, led to the adoption of the 64 bit word, which will cause bytes, which are not powers of two, to overlap word boundries. The continuous stream concept, also, requires that information be continuously available to the processing unit.

These requirements suggest a ring type of register, of which half is loaded while the other half is being used. The exact size of this ring will have to be determined by timing studies. Present thinking is that each ring will be either 64 bits or 128 bits in length. Three of these double-pair ring registers will be needed for the continuous stream type of operation, two for sending information to the logic and the third for receiving information from the logic unit. Since the exact form of these registers has not been determined, it is not known at present whether the functions of the registers can be interchanged or not.

The continuous stream registers and their controls are the subject of a document by Mr. S. W. Dunwell entitled "Machine Specification Report #1". Some of the information of the previously mentioned document will be repeated here for the purpose of clarity.

For the continuous stream register concept certain things about the three pairs of registers are quite similar.

1. The two registers (the A and B registers) feeding the logic unit will probably be identical.

2. The control information required to control information to and from the logic unit is quite similar. This information is:

a. The memory word address,
b. The byte address,
c. The byte advance.

(The byte size of Machine Specification Report #1 should probably be thought of as the byte advance. The byte size may need to be controllable from the logic unit. This will give additional flexibility which is desirable.)

Some additional functions are being considered. One of these is mentioned in Machine Specification Report #1 as "spiralling". The need for this arises in that if the spiral is short, of the order of 5 bytes, the conventional method of obtaining an instruction and of modifying the address with the contents of an index register may require a good portion of the processing time. If the spiralling feature proves worthwhile enough to incorporate in the machine as an automatic feature, the byte advance of the previous paragraph can be considered as a special case of spiralling, and a byte advance other than the byte size may not be needed as such.

The continuous stream register is a first level of automatic indexing. If the spiralling operation is to be automatic, this is a second level of automatic indexing. This second level of automatic indexing steps through the memory space in a regular fashion. However, if it is desired to step through memory in an irregular fashion, for very short cycles, the efficiency of the operation will probably be decreased.

Although it has not been mentioned, it probably will be quite desirable to step through the information in memory in either direction, both by byte and by word.

The speed of operation imposed upon each of the three double-pair registers is such that an adder will probably be required for each control to advance (or subtract) the byte advance from the byte address to obtain the new byte position. However, if we have automatic spiralling, it may be possible to use one adder (or subtracter) to modify for the new starting address of each of the three

controls. A further reason for this is that it is more likely that the programmer will wish to modify two controls rather than three at any one time.

Assuming spiralling, a problem which must be answered is how should this be done? To further complicate the problem, the controls of the logic unit must be reset at the same time; however, this resetting of the controls of the logic unit is facilitated by the fact that the portion of the instruction pertaining to the logic unit need not be modified in any manner during a spiralling type operation.

Since the continuous stream controls permit the logic unit to be completely separated from address modification, it may be desirable to put a small loop of instructions in a high speed memory associated with the logic unit. By placing in each instruction of the logic unit, the address of the next instruction the logic unit could proceed through a complicated loop of instruction without attention from the master program control. Such a small high speed memory may, also, be a practical means of storing the information needed for automatic spiralling.

Since the continuous stream register control system may be used part time as a search operation, it will be necessary, upon an indication of success, to be able to read the approximate location or locations at which this success was obtained. Therefore, the program must be able to obtain the contents of the control registers or the contents of registers containing equivalent information to the control registers, without disrupting the information contained in the continuous stream registers.

In addition to these requirements a small high speed memory may be desirable as a source of index quantities and data.

If such a small high speed memory is provided, it may be practical to impose upon the master control unit, which has the function of address modification already, the requirement of address modification for spiralling. Assuming that the information necessary to control the advance of one spiral may be put into one word of the small high speed memory, and that the cycle of the small high speed memory is 0.2 mocrosecond, it might be possible to read out, advance, and restore the new information needed for the control register in about 0.4 mocrosecond. In order to determine a practical system, the times for the various functions must be assumed or

determined and timing charts must be laid out.

In addition to the control function described above, the C register control will have additional functions imposed upon it. (The C register receives information from the logic unit.) This is evidenced by the fact that sometimes the C register will assemble addresses and other times assemble data for storage or for the return to one of the input registers. (The input registers are the A and B registers.) Since the continuous stream concept takes care of the storing of data, with the exception, perhaps, of inserting pieces of data into memory words, the problem of storing data will not be discussed further.

The A and B registers will often be used either singly or together to form a partial stream of addresses. It will usually be necessary to combine this partial address with a prefix and a suffix to form the complete address. Such a function as just described is needed for counting in memory (Machine Specification Report #3) or in some operation such as a translation of codes via table lookup.

In an operation such as a translation, the result of the table lookup must be brought down and entered in a continuous stream fashion into a register for storage. Since it will not be desirable to dump the contents of the A and B registers, additional equipment must be provided to extract the portion of the table from memory if it is desired to do this extraction immediately. (This portion of the table is by previous definition 2 to some power bits in length.) If such equipment is needed for other operations, such an operation may conceivably be practical. However, it is more likely that such an operation should be broken into two distinct operations which may be:

1. The forming of the partial address

2. Using this partial address as an "index" quantity for a second operation.

Since address modification equipment already exists in the master control unit, it may be practical to send a partial address to the master control unit and treat it as the contents of an index register. This address when formed would then be sent to memory for a count one, or to look up the contents of a table. This method however does not get around the problem of extracting a part of a word to

obtain the contents of the address. Therefore, a more practical solution may be to store away the partial addresses in a continuous or discontinuous fashion, and then to use these partial addresses as index quantities either with or without a continuous stream register for later operations. One of the two input registers could then be used to extract a portion of the table.

This second method could use one of the input continuous stream registers as a source of continuous index quantities under control of the master control system. The second input continuous stream register would then be available for extracting the contents of the table. Such a second system as this seems desirable for other applications.

If the partial address mentioned previously is formed by arithmetic, the table entries do not need to occupy spaces in memory which are powers of 2.

WAH/jh

W. A. Hunt