September 27, 1956

PROJECT STRETCH
LINK COMPUTER MEMO NO. 9

SUBJECT: Link Instruction Format Meeting

BY: F. P. Brooks

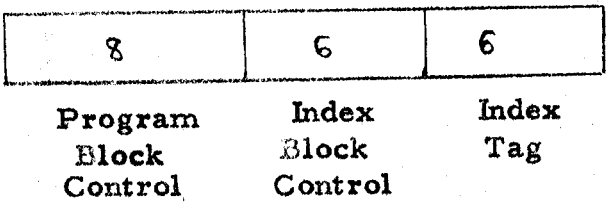
Messrs. W. Buchholz, F. P. Brooks and W. Wolensky, in a meeting on August 31st, discussed instruction word format and related problems. There were several tentative conclusions:

1) Specification of a full 20 or 26 bit address in each instruction is unduly extravagant. The full 20 bits to specify a word should be divided into a high order part, the block address, and a low order part, the word address. Block address would be set from time to time and remain in some suitable register until changed. Word address of from 12 to 16 bits should be specified in the instruction.

2) Index register tags in instructions, should in general consist of fewer bits than memory address, from 6 to 10, and should be specified within memory block by a subblock structure similar to that proposed for memory addresses.

Example:

Memory Address



3) Machine status or mode should be set with a single machine control word whose bits would specify many different model operations.

4) On break-ins in a program, the machine control word and other necessary words should be stored at some specified place within the memory block currently in use.

5) Streaming operations of the link should be controlled by a control word and mechanism similar to, or identical with, that used by the Exchange. Provision should be made for storing tables of control words with automatic stepping from one to another.

6) Indexing should involve the use of one and only one central register, whose contents are added to given direct addresses before they are interpreted. Multiple indexing would be accomplished by repeated filling of the central index register and modification of the address awaiting interpretation. Specification of data to enter the central index register, could be made partly within the basic instruction (for single or double indexing) and partly within trailer instruction half-words; or such specification could be made entirely in trailer half-words. This latter method has disadvantages when indirectly addressed quantities are to be indexed.

7) If words as short as 48 bits are to be used, full-word modules appear necessary for basic instructions and for some operations, full word trailers would also be necessary.

8) If words of 60 or 64 bits are used, it may be possible and would, in general, be desirable to use half-word modules for basic instructions, with one or more half-word trailers when needed to provide more instruction information.

9) Some possible formats are:

Operation Code	8	8	8	7	7
Memory Address	10	12	20	10	12
Mode of Addressing	2	2	2	2	2
Trailer Following Tag	1	1	1	1	1
Indexing quantity	10	12	12	10	6
Mode of Indexing	3	3	3	3	3
	34	38	46	33	31

10) The mode of addressing tag distinguishes between direct, indirect and immediate addresses.

11) The mode of indexing tag specifies:

a. Whether the contents of the central index register are to be used for the modification of the memory address,

b. Whether the data specified as the indexing quantity is to replace, increment, or decrement the contents of the central index register,

c. Whether the next half-word instruction is to be interpreted as a multi-indexing control trailer.

12) For some instructions, it may prove desirable to interpret the mode of addressing bits as applying to the indexing quantity, rather than the memory address.

13) Trailers would, in general, be necessary to revise or specify byte size, bit address, length of bit or byte field, and multiple indexing quantities.

F P Brooks

FPB:gmp

F. P. Brooks