Griffiths

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COMPANY CONFIDENTIAL

Link Exchange Memo No. 7

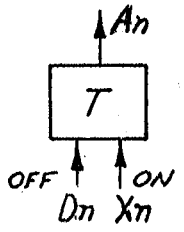
The Synthesis of a Sequential Circuit in the Link Exchange

Summary

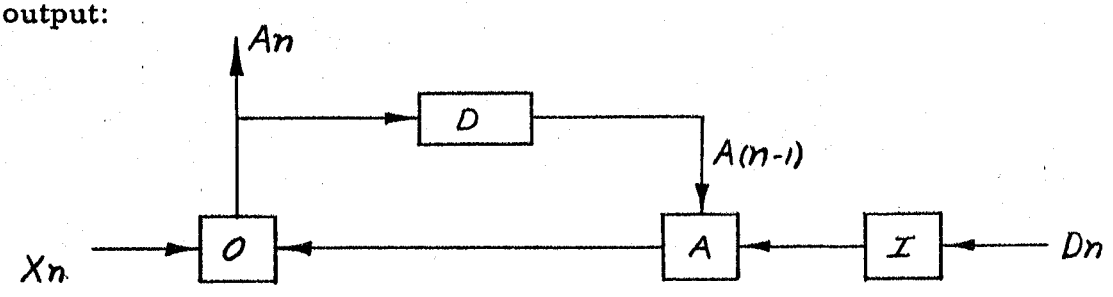
By considering triggers as delay circuits, it is possible to handle sequential circuits in the same manner as combinatorial circuits. The following is an example of this method.

Sequential and Combinatorial Circuits

In a combinatorial circuit, any given input produces a definite output, the nature of which is determined in advance. In a sequential circuit, the output is a function not only of the input, but is also a function of the state of the circuit. In other words, a sequential circuit has a history, resulting from previous inputs, which is a factor in the present functioning of the circuit. These past inputs can be represented by recirculating delay lines. For example the trigger



can be represented as follows, with n representing the time of an input or output:



This trigger circuit can be symbolized by the recursive expression:

$$A_n = X_n \vee A(n-1)\,\bar{D}_n$$

where A(n-1) is the previous state of the circuit, produced by prior inputs.

Assuming the original state of the circuit to be zero, we can represent the history of the circuit as follows:

$$\begin{aligned} A_o &= X_o \vee A(-1)\,\bar{D}_o \\ &= 0 \vee 0 \\ &= 0 \end{aligned}$$

$$\begin{aligned} A_1 &= X_1 \vee A_o\,\bar{D}_1 \\ &= X_1 \vee 0 \\ &= X_1 \end{aligned}$$

$$\begin{aligned} A_2 &= X_2 \vee A_1\,\bar{D}_2 \\ &= X_2 \vee X_1\,\bar{D}_2 \end{aligned}$$

$$\begin{aligned} A_3 &= X_3 \vee A_2\,\bar{D}_3 \\ &= X_3 \vee (X_2 \vee X_1\,\bar{D}_2)\,\bar{D}_3 \\ &= X_3 \vee X_2\,\bar{D}_3 \vee X_1\,\bar{D}_2\,\bar{D}_3 \end{aligned}$$

$$\begin{aligned} A_4 &= X_4 \vee A_3\,\bar{D}_4 \\ &= X_4 \vee (X_3 \vee X_2\,\bar{D}_3 \vee X_1\,\bar{D}_2\,\bar{D}_3)\,\bar{D}_4 \\ &= X_4 \vee X_3\,\bar{D}_4 \vee X_2\,\bar{D}_3\,\bar{D}_4 \vee X_1\,\bar{D}_2\,\bar{D}_3\,\bar{D}_4 \end{aligned}$$

$$A_n = X_n \vee X(n-1)\,\bar{D}_n \vee X(n-2)\,\bar{D}(n-1)\,\bar{D}_n \vee \ldots \vee X_1\,\bar{D}_2\,\bar{D}_3 \ldots \bar{D}_n$$

An output is thus the result either of a present input, or of some past input not followed by an inhibition.

Channel Selection in the Link Exchange

A circuit is required in the Link Exchange which will assign channels upon the receiving of a service request. The circuit should always assign the first available channel. For example, if Channel I and III

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FIGURE 1

p X_n	q $A^1(n-1)$	r $A^2(n-1)$	s $A^3(n-1)$	t $D^1(n-1)$	u $D^2(n-1)$		$A^1{}_n$	$A^2{}_n$	$A^3{}_n$	B_n
0	0	0	0	0	0		0	0	0	0
0	0	0	0	0	1		0	0	0	0
0	0	0	0	1	0		0	0	0	0
0	0	0	0	1	1		0	0	0	0
0	0	0	1	0	0		0	0	1	0
0	0	0	1	0	1		0	0	1	0
0	0	0	1	1	0		0	0	1	0
0	0	0	1	1	1		0	0	1	0
0	0	1	0	0	0		0	1	0	0
0	0	1	0	0	1		0	0	0	0
0	0	1	0	1	0		0	1	0	0
0	0	1	0	1	1		0	0	0	0
0	0	1	1	0	0		0	1	1	0
0	0	1	1	0	1		0	0	1	0
0	0	1	1	1	0		0	1	1	0
0	0	1	1	1	1		0	0	1	0
0	1	0	0	0	0		1	0	0	0
0	1	0	0	0	1		1	0	0	0
0	1	0	0	1	0		0	0	0	0
0	1	0	0	1	1		0	0	0	0
0	1	0	1	0	0		1	0	1	0
0	1	0	1	0	1		1	0	1	0
0	1	0	1	1	0		0	0	1	0
0	1	0	1	1	1		0	0	1	0
0	1	1	0	0	0		1	1	0	0
0	1	1	0	0	1		1	0	0	0
0	1	1	0	1	0		0	1	0	0
0	1	1	0	1	1		0	0	0	0
0	1	1	1	0	0		1	1	1	1
0	1	1	1	0	1		1	0	1	0
0	1	1	1	1	0		0	1	1	0
0	1	1	1	1	1		0	0	1	0
1	0	0	0	0	0		1	0	0	0
1	0	0	0	0	1		1	0	0	0
1	0	0	0	1	0		1	0	0	0
1	0	0	0	1	1		1	0	0	0
1	0	0	1	0	0		1	0	1	0
1	0	0	1	0	1		1	0	1	0
1	0	0	1	1	0		1	0	1	0
1	0	0	1	1	1		1	0	1	0
1	0	1	0	0	0		1	1	0	0
1	0	1	0	0	1		1	0	0	0
1	0	1	0	1	0		1	1	0	0
1	0	1	0	1	1		1	0	0	0
1	0	1	1	0	0		1	1	1	1
1	0	1	1	0	1		1	0	1	0
1	0	1	1	1	0		1	1	1	1

Figure 1

p X_n	q $A^1(n-1)$	r $A^2(n-1)$	s $A^3(n-1)$	t $D^1(n-1)$	u $D^2(n-1)$		$A^1{}_n$	$A^2{}_n$	$A^3{}_n$	B_n
1	0	1	1	1	1		1	0	1	0
1	1	0	0	0	0		1	1	0	0
1	1	0	0	0	1		1	1	0	0
1	1	0	0	1	0		1	0	0	0
1	1	0	0	1	1		1	0	0	0
1	1	0	1	0	0		1	1	1	1
1	1	0	1	0	1		1	1	1	1
1	1	0	1	1	0		1	0	1	0
1	1	0	1	1	1		1	0	1	0
1	1	1	0	0	0		1	1	1	1
1	1	1	0	0	1		1	1	0	0
1	1	1	0	1	0		1	1	0	0
1	1	1	0	1	1		1	0	0	0
1	1	1	1	0	0		1	1	1	1
1	1	1	1	0	1		1	1	1	1
1	1	1	1	1	0		1	1	1	1
1	1	1	1	1	1		1	0	1	0

are unassigned, a service request should cause the assigning of Channel I. Channels can be disconnected at random, but a disconnect signal cannot occur at the same time as a service request. When all channels are assigned, a busy signal is to be produced.

Figure 1 shows a truth table expressing these conditions. The following inputs are regarded as present:

X_n = service request
$A^1(n-1)$= state of assignment of Channel I
$A^2(n-1)$= state of assignment of Channel II
$A^3(n-1)$= state of assignment of Channel III
$D^1(n-1)$= disconnect signal for Channel I
$D^2(n-1)$= Disconnect signal for Channel II

To avoid expanding the truth table, a $D^3(n-1)$ signal for disconnecting Channel III was not included. The subscript (n-1) attached to the disconnect signals is intended to represent a disconnect signal occurring sometime between n-1 and n. The literals, "p", "q", "r", "s", "t", "u" can be used to facilitate handling the symbols in the truth table.

The outputs are:

A^1_n = signal assigning Channel I
A^2_n = signal assigning Channel II
A^3_n = signal assigning Channel III
B_n = busy signal

All input conditions for these outputs are disjoined in the usual manner, and the resulting expressions simplified. The following are the final expressions for the outputs:

$$A^1{}_n = X_n \vee A^1(n-1)\,\bar{D}(n-1)$$

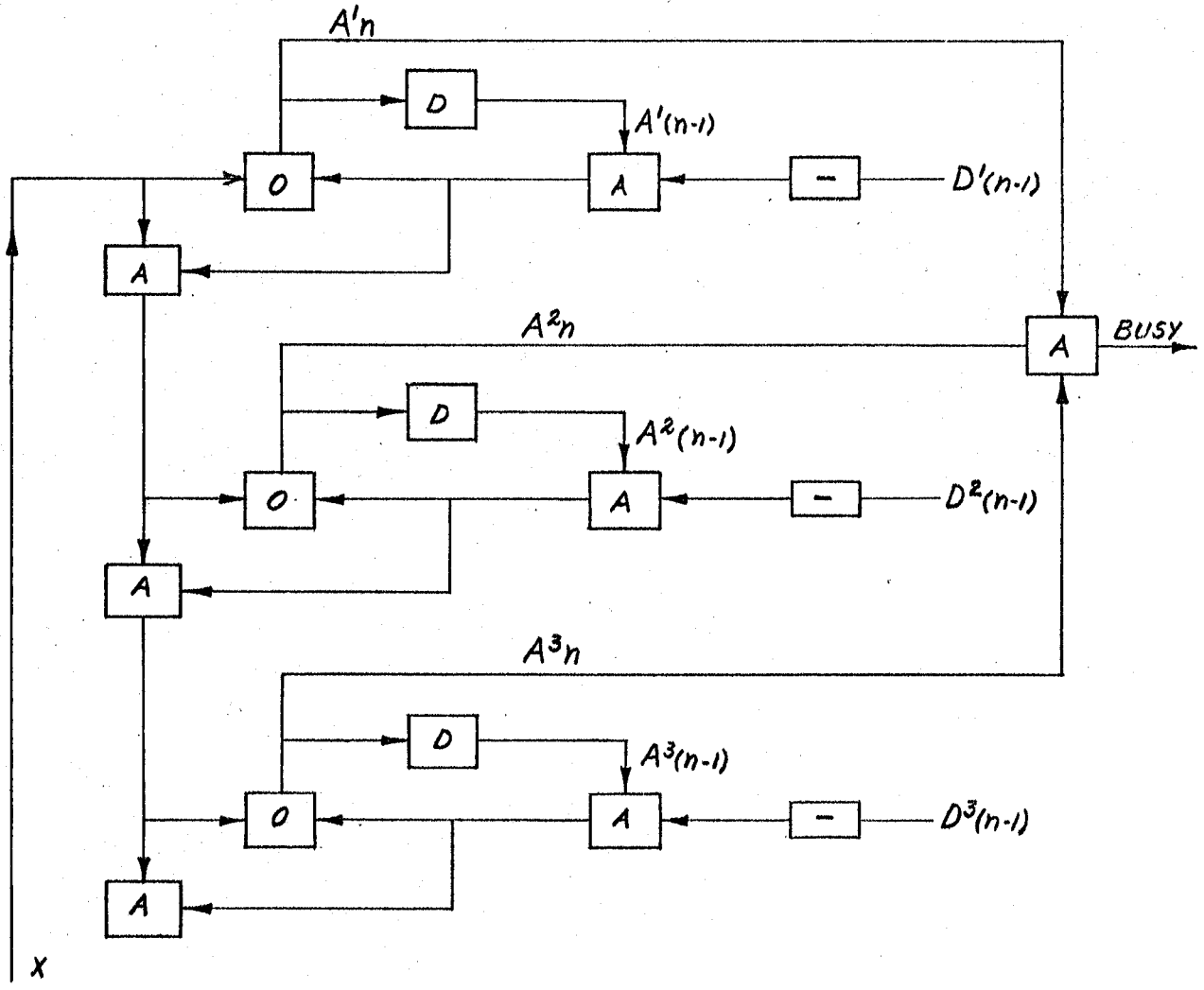
$$A^2{}_n = A^2(n-1)\,\bar{D}^2(n-1) \vee X_n\,A^1(n-1)\,\bar{D}^1(n-1)$$

$$A^3{}_n = A^3(n-1) \vee X_n\,A^1(n-1)\,A^2(n-1)\,\bar{D}^1(n-1)\,\bar{D}^2(n-1)$$

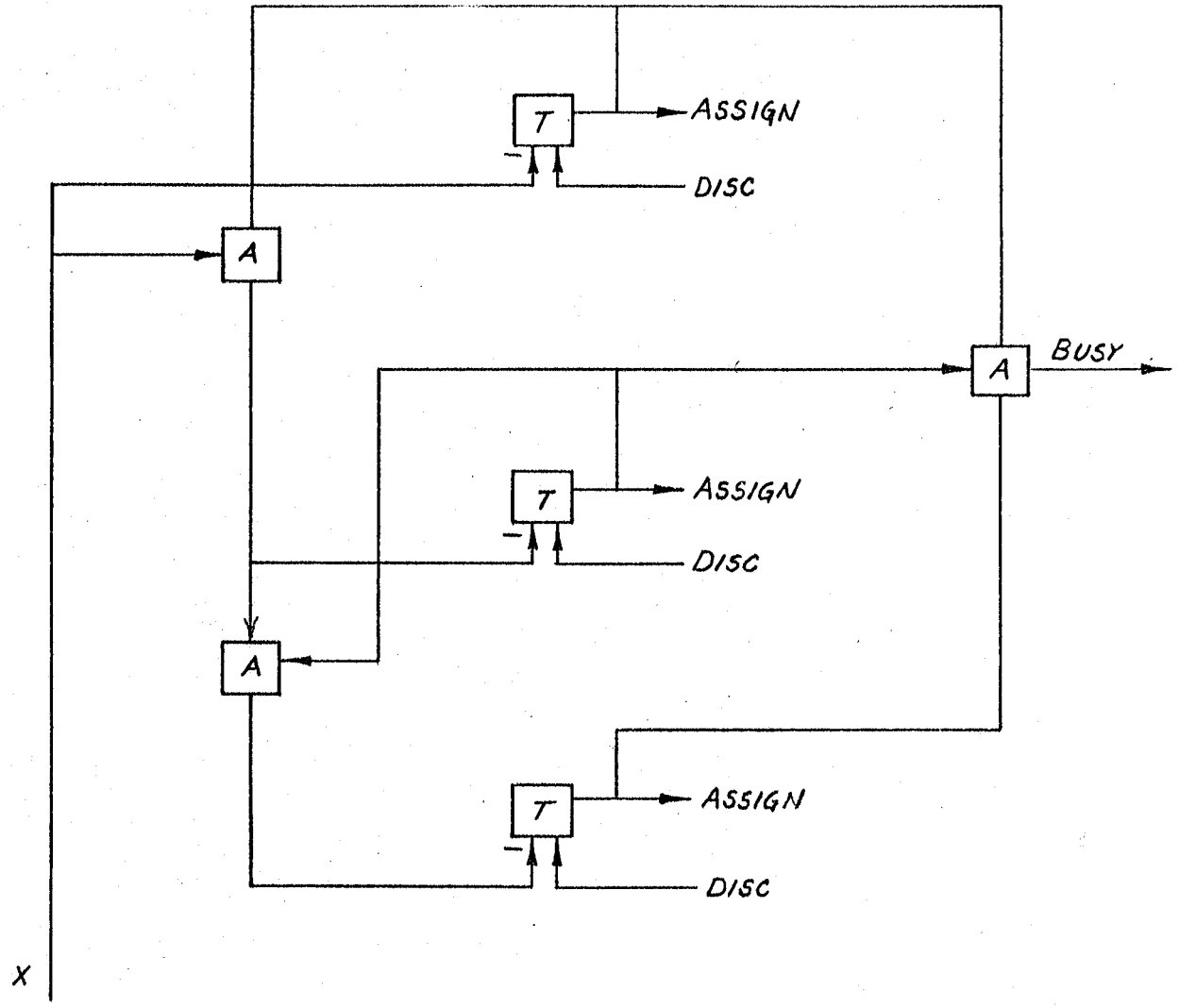
$$B_n = X_n\Big[A^1(n-1)\,\bar{D}^1(n-1)\,(A^3(n-1) \vee A^2(n-1)\,\bar{D}^2(n-1)) \vee A^2(n-1)\,A^3(n-1)\,\bar{D}^2(n-1)\Big] \vee A^1(n-1)\,A^2(n-1)\,A^3(n-1)\,\bar{D}^1(n-1)\,\bar{D}^2(n-1)$$

To draw the actual circuit it is merely necessary to interpose a delay after, say, A_n to create A(n-1). Since this is a multiple output circuit, a degree of skill is required for using common factors in the most advantageous way.

The circuit which results is as follows:



We may now replace the delay-line circuits by triggers, to obtain the following circuit:



This circuit contains three "and" gates, as compared with seven in the circuit prepared without the aid of Boolean algebra, which is shown in the diagram below.

WHD:ja W. H. Desmonde