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how Counters work in Exchange

PROJECT STRETCH

FILE MEMO #37

SUBJECT: A Method of Rapidly Advancing or Decreasing a Binary Number by 1.

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DATE: May 14, 1956

For the 1 column, it can be seen that

$$1_o = \overline{1}_i$$

where 1_o determines the output of the device and 1_i the input for the 1 column.

Further: $2_o = 2_i \not\vee 1_i$

$$4_o = 4_i \not\vee 2_i\ 1_i$$

$$8_o = 8_i \not\vee 4_i\ 2_i\ 1_i$$

and if a table of higher orders were constructed it can be shown that

$$16_o = 16_i \not\vee 8_i\ 4_i\ 2_i\ 1_i$$

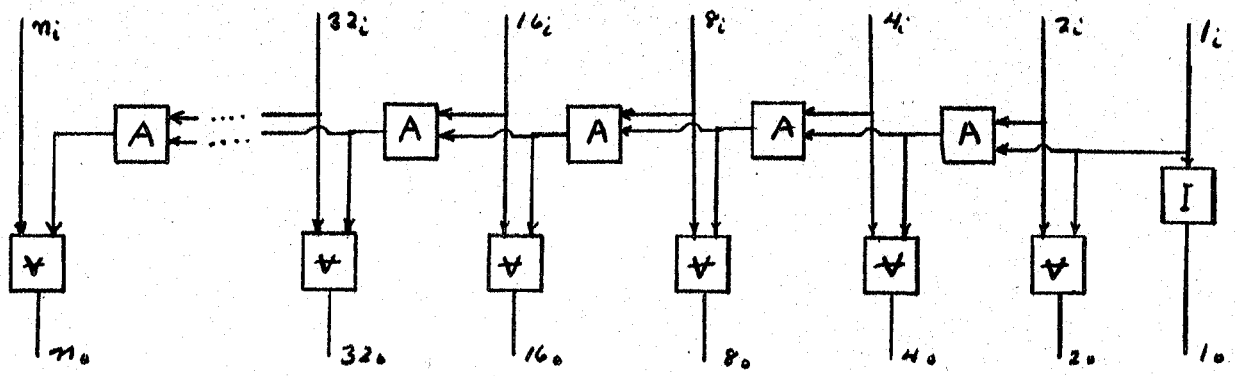
and $$32_o = 32_i \not\vee 16_i\ 8_i\ 4_i\ 2_i\ 1_i$$

or a general expression can be written for any order variable:

$$n_o\ 6\ n_i \not\vee [(n-1)_i \cdot (n-2)_i; (n-3)_i \ldots\ldots 2_i \cdot 1_i]$$

where n-1, n-2, etc. refer to successive lower order binary variables to the nth order.

For a minimum number of components, a chain can be constructed involving generally one 2-way AND and 1 Exclusive-OR per order except for the 1st and 2nd orders.



The delay between input and output would be determined by the rise times of the Exclusive-OR components and the AND circuits.

May 14, 1956

A Method of Rapidly Advancing or Decreasing a Binary Number by 1.

One of the tentative design considerations of the I/O Communications system for Stretch involves a technique of reading out an address of 20 binary bits from memory, modifying it by stepping the binary number up by 1, and storing it back into memory. It is desired to do this within one memory cycle of 2 μsecs.

Essentially what is needed is a black box, the input of which is the original binary number and the output of which is the number advanced by one. The time between input and output should be as close to zero as possible. An approach different from trigger counters or adders shall be investigated.

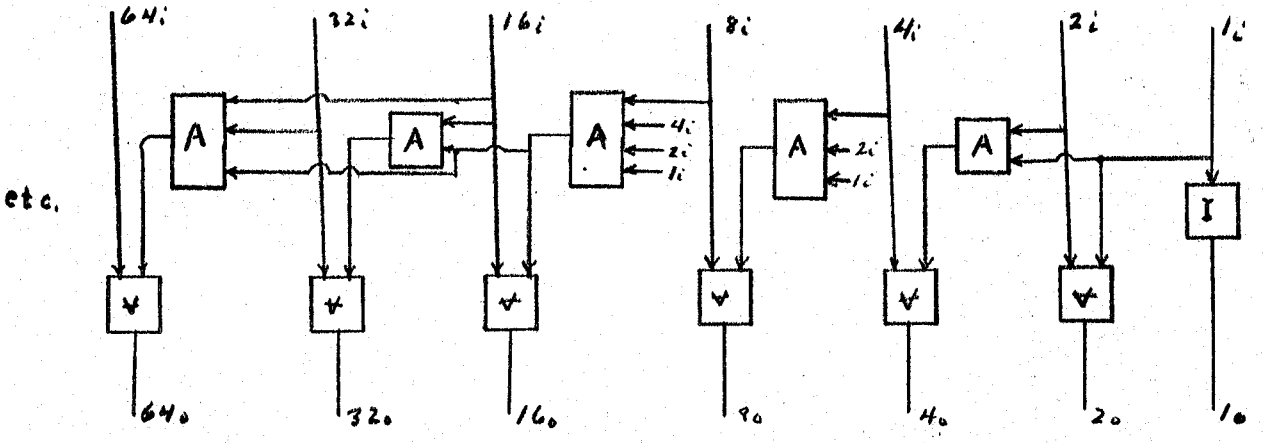
Constructing the following table of 4 binary variables

8	4	2	1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

one can determine upon examination an expression by which, for a given binary number, its successor can be determined.

It can be seen that in the worst case a carry must be propagated through the entire chain of AND circuits before the result is stabilized.

If this carry propagation time becomes restrictive at the speeds we are interested in, the carry time can be minimized by breaking the n bit binary number up into convenient sections and only propagating carries between sections. The entire carry propagation time would therefore be the rise time of one AND circuit multiplied by (number of sections -1). For example, if the number is broken up into sections of 4 bits each, the following configuration would result;



which reduces the carry propagation time considerably.

A method for constructing a logical connective arrangement which counts down by one can also be derived. It is desired that the output of the device be the input binary number decreased by 1.

In this case, we can write the expressions for each column as follows:

$$1_o = \overline{1_i}$$

$$2_o = \overline{2_i} \vee 1_i$$

$$4_o = \overline{4_i} \vee (2_i \vee 1_i)$$

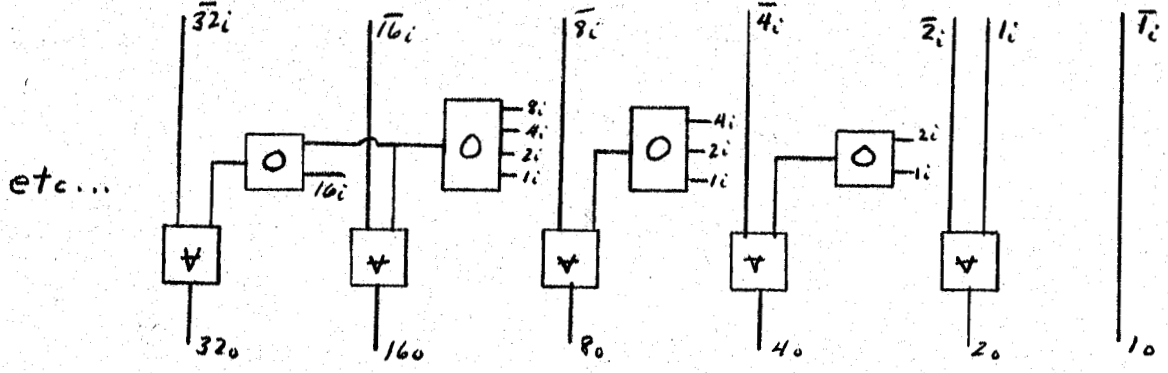
$$8_o = \overline{8_i} \vee (4_i \vee 2_i \vee 1_i)$$

$$16_o = \overline{16_i} \vee (8_i \vee 4_i \vee 2_i \vee 1_i)$$

and in general terms for the nth column of binary variables

$$n_o = n_i \vee \left[(n-1)_i \vee (n-2)_i \ldots\ldots\ldots 2_i \vee 1_i \right]$$

The off side of the triggers composing the register can be utilized to obtain the denial of the input in each case. An example of a few orders of such a counter would be as follows:



In the foregoing methods, counting has been restricted to counting one up or down. It should be pointed out that with the addition of some gating the input number can be modified by any single binary order, 1, 2, 4, 8, etc., by merely gating the denial of the value of that variable into the counter into the proper position. The number then could be advanced or decreased by 1 or 2 or 4 or 8, etc., depending upon which denial was gated in.

Such a counting device would be extremely useful in the Communicator. The same device would also be useful operating in conjunction with other memories of the machine where upon command a word could be read out of memory, stepped by 1 and returned in the same cycle.

The usefulness of a single component to perform the Exclusive-OR functions becomes readily apparent. Continuing investigation serves to emphasize the need for an Exclusive-OR component and the desirability of increasing the activity relating to its development.

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