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COMPANY CONFIDENTIAL

PROJECT STRETCH

FILE MEMORANDUM #32

SUBJECT: Buffering

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The purpose of this memo is to set down some observations bearing on the choice of a buffering system for LINK (the name being used for the input-output section of the STRETCH system). Details of the system chosen will be covered in later memos.

1. The addition of separate buffers to the early EDPM machines was a significant step of progress towards higher performance. We have since learned another step forward, which is to time-share the main memory for input, output, and computing, thus getting all the benefits of buffering at a considerable reduction in cost.

2. Buffering in memory is essential to the real-time operation which in turn is a basic requirement of LINK. LINK must be able to deal with many, perhaps hundreds, of low-speed input-output devices, such as keyboards, typewriters and transmission lines. Separate buffer storage devices would represent a very substantial amount of extra equipment. Buffering in memory also avoids the delay involved in transmitting information between separate buffers and memory, and it even permits the program to start processing the early part of a record before the remainder has been read.

3. For buffering very high speed tape and RAM units, operating at rates of a word every few microseconds, it will be necessary to provide a set of registers to hold at least

(a) the current data word being transferred to or from memory,

(b) the memory address for the current word, and

(c) the count of words yet to be transferred.

As each data word is transferred, the memory address is selected, the address is advanced by one, and the count is reduced by one. Because of the speed required, this process must be fully automatic, the only computer

time required being a single reference to memory per word. The computer program merely starts the process and interrogates occasionally to see how the record is progressing. (See STRETCH Memorandum #5 for details.)

Each very high speed tape and RAM unit operating simultaneously must have its own set of these registers in order to realize the high speeds.

4. For buffering very low speed units, operating in the area of 10 words a second or less, it is possible to time-share a single set of data and control registers (see 3 above) among all the units. In fact, cost dictates time-sharing of equipment.

Suppose the control information (address and word count) occupies one word of 60 bits. When an input-output unit is ready to transfer a word, the control information is called out of a memory location set aside for this particular input-output unit, entered into a control register, used, modified, and returned to memory. (Whether this can reasonably be squeezed into one memory cycle remains to be determined; for now we will assume it takes two cycles.) The control register is then available for use with any other low-speed input-output unit.

5. For medium-speed units, such as card readers, printers, and Type 727 tape units, the case is not as clear. If memory speeds are relatively low, these units may have to be treated like high-speed units (as in 3 above). If memory speeds are high enough, complete time-sharing as for the low-speed units (see 4 above) is entirely feasible. Compromises are also possible. A proper balance of speed and equipment is currently being determined as part of the detailing of the buffering system.

6. The medium and lower speed input-output units typically transmit only one character of 6 bits (plus check bit) at a time. 10 such characters are needed to fill a 60 bit memory word. There are several ways of assembling the 10 characters into a word at the input, or splitting a word into 10 characters at the output.

(a) Provide one shift register, or equivalent, for every input-output unit that is to operate simultaneously with others.

(b) Provide only one shift register and time-share it, with partially assembled words being stored in pre-determined memory locations.

(c) Provide a special core memory for partially assembled words, transmitting the words into main memory only after complete assembly.

(a) and (c) are really the same thing, except that (c) combines a set of individual data registers into a core array for greater economy. In either case, separate memory is provided to relieve the main memory of the extra memory cycles involved in assembling a set of 10 characters.

(b) is an extension of (4) where a single set of equipment is time-shared at the expense of extra memory references. There could be a considerable reduction in equipment.

7. There is some question whether a reduction of references to main memory is the desired goal since it comes at the cost of adding less flexible, special-purpose memory equipment. Moreover, if the simplest form of time-sharing of registers with a single memory turns out to load the memory with too many references, it is always possible to increase the performance again by providing a second block of "main memory". This building-block approach provides the user a choice of either a simpler machine or a higher-performance machine.

The questions to be resolved by further study are:

(a) How much equipment is involved in either approach?

(b) Is input-output performance impaired by time-sharing?

(c) Is computer performance impaired by time-sharing?

8. The extent to which buffering occupies main memory can be determined by calculating the "memory occupancy" S, that is, the percentage of the time that memory is occupied with input-output references and not available for computing:

$$S = 100\ K\ m \sum_i \frac{1}{p_i} \%$$

where m = length of memory cycle (sec.)
p_i = time interval between successive accesses to memory by the i th input-output unit (sec.)
K = number of memory references needed for each input-output access to memory.

Examples:

(a) Buffering 4 magnetic tape units, Type 727, (15,000 characters/sec.) by assembling 10 characters in separate one-word registers (see 6a or 6c).

$p = 670 \times 10^{-6}$ sec.
K = 1

Assume a memory cycle

$$m = 2 \times 10^{-6} \text{ sec.}$$

Then $S = 200 \times \frac{4}{670} = 1.2\%$

(b) Same as (a) except that data and control registers are time-shared and characters are assembled in memory (see 6b).

$$p = 67 \times 10^{-6} \text{ sec.}$$

$$m = 2 \times 10^{-6} \text{ sec.}$$

K = 3(one reference for the data word and two for the more elaborate operations involving the control word)

$$S = 3 \times 200 \times \frac{4}{67} = 36\%$$