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COMPANY CONFIDENTIAL

PROJECT BETA February 6, 1956

FILE MEMO #14

SUBJECT: Memory Address Decoder Error Detection

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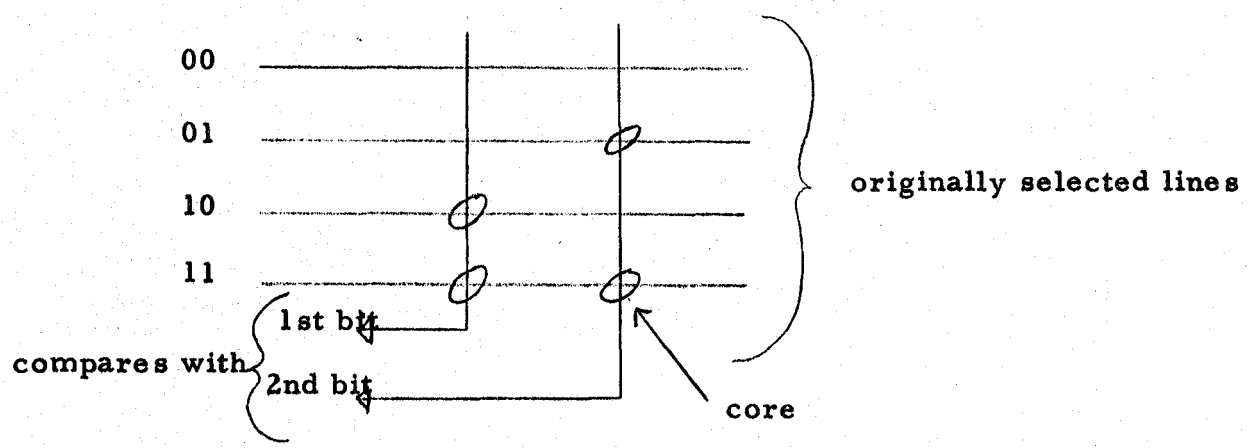
The following describes a system to check to see if the correct drive line is selected during a core memory read out. The system works essentially like this: The X or Y line selected is represented initially in a memory address register by a certain number of bits. The bits are supposed to cause a certain X or Y plane to be driven to select the word to be read out. If a few additional cores are attached to the particular X or Y line and are caused to read out such that they produce the address of the line selected, this address can be compared with the original address to check for errors in decoding. Using a 2 bit address for the X portion, the following gives a rough outline of the scheme.



This is essentially an inverse decoder using cores. The cores are arranged in a fixed configuration to give the desired address.

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