December 20, 1955

PROJECT STRETCH

FILE MEMO #16 COMPANY CONFIDENTIAL

SUBJECT: Editing - Part I

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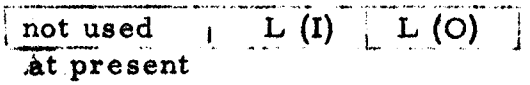
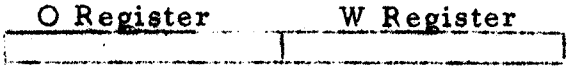
I. The Editing organ of the Stretch machine will be composed of the four registers of the arithmetic unit. These registers will normally not be available for arithmetic uses when Editing instructions are being executed.

The four registers are labeled separately for control by the Editing instructions:

I Register - This register is used as the editing input register. It is reloaded automatically for memory when its contents have been scanned and such automatic reloading is desired. It is loaded and reloaded under control of the D register.

D Register - 

This register is divided into three 20 bit fields. The field L (I) contains the memory address of the next word to be loaded into the I register. The field L (O) contains the memory address of the next word to be stored from the O register. L (I) or L (O) is stepped up by one whenever a memory reference is made using that field as an address.



O Register - This register is the leftmost register of a pair of registers which are used to assemble the edited data. The O register receives the edited information as it is shifted out of the W register. When the O register has been filled, its contents are automatically stored at the address L (O) specified in the D register. The contents of the O register are reset to a one in the low order position whenever a readout occurs from the O register.

W Register - This is the rightmost register of the pair O-W. This register receives data from the I register or the memory. Data placed in the W register may replace data already there or may be added to data already there. The contents of the W register may be shifted left into the O register.

II The use of these registers in carrying out an editing assignment is facilitated by a generalized Tranform command. This Transform command utilizes a special form of table lookup and normally causes a lookup on data in the I register to be transformed into data which is placed in the W register and then shifted into the O register.

In general, the operation is carried out as follows:

A table lookup is performed on a number of characters in the I register. The contents of the table entry are placed in the W register and a specified shift takes place to the left.

The size and number of characters to be examined in the I register may be specified.

The disposition of the table entry may be specified.

The operation is continuous but may be interrupted conditionally.

The scanning of the data in the I register may be altered depending upon the contents of the table entires.

III Execution Word Layout

Opn	J	H	C	A	N	B	Table Origin
	3	8	5	4	12	4	20 bits

J - not used at present
H - Index Register tag
C - Control

a) Autoloading of the I register. If autoloading is specified, when 60 bits have been shifted in the I register, word specified by L (I) in D register is loaded into the I register. L (I) is increased by 1.
b) Examine the I register from left to right.
c) When O register is full, replace the contents of L (O), or OR with the contents of L (O).
d) Add the character to the low order part of the Table Origin to be used next.
e) Compare tag in H field with tag in CA; Restore CA with C (H) if tag comparison is unequal.

N - maximum number of characters to use during execution of Transform command
A - not used at present
B - number of bits that constitute a character in 1
Table Origin - Origin of first table to be used by the Transform command

IV Table Word Layout

The arrangement of the Table Word and an explanation of the many variations of its uses is covered in Part II of this memo.

V End of Operation - It is possible to terminate the execution of the Transform command by appropriate designations in the table entries (See Part II). If an addressed table entry contains an "End-of-Operation" designation, the Table Origin field of the table entry will be placed in the Table Origin field of the Execution Word in the decoder, and the machine will proceed to the next instruction.

At this time a special instruction, Transfer to Origin, may be used to transfer to the address given by the Table Origin field in the decoder, provided that this field is not zero. This transfer may be indexed and will normally be used to transfer to a subroutine which will handle a special case not included in the normal Transform command routine.

If the field N in the Execution Word has been counted down to zero, the Table Origin field of the Execution Word will be reset to zero, and the machine will proceed to the next instruction.

VI An instruction, load D register, will cause the contents of the memory location addressed to be placed in the D register.

There are two bits in the instruction to control the loading of the I register and the resetting of the O register.

The I register bit, if present, causes the I register to be loaded immediately with the contents of L (I).

The O register bit, if present, causes the O register to be reset to one.

VII Edit Compare Instruction

This is a special instruction which will compare two records starting at different memory addresses. When this instruction is given, it will compare two records whose starting addresses are given by the

L (I) and L (O) fields of the D register.

Edit Compare Layout

opn	C	N	S_2	S_1	T	A
10	3	10	6	6	8	17

C - control

a) Transfer on S_1 high
b) Transfer on S_1 low
c) Transfer on $S_1 = S_2$
d) Transfer on $S_1 \neq S_2$
e) Do not transfer

N - maximum number of characters to be compared

B - size of characters

S_1 - starting bit position in word at L (I)

S_2 - starting bit position in word at L (O)

T - Index Register Tag

A - Transfer Address

This compares two sequences:

Sequence 1 starts at the S_1 bit of word at L (I)
Sequence 2 starts at the S_2 bit of word at L (O)

A special set of high, low, equal indicators will be set as a result of the outcome of the comparison, and a transfer to address A will be controlled by the bits in the C field.