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PROJECT STRETCH
File Memo # 15

Poughkeepsie, New York
December 15, 1955

COMPANY CONFIDENTIAL

SUBJECT: A method to Eliminate Some Problems Caused by Non-sequential References to Memory

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The title refers to the problem which arises due to a reference to a memory location A which is yet to be changed by a store type instruction to memory location A, even though the store type instruction precedes the reference instruction in the program sequence.

The following outlines an address comparison system which, when combined with the tag comparison (given in the memo on Indexing), makes the Stretch machine look like a sequential machine to the programmer.

The principle of operation is that should an occasion as described in paragraph one arise, the conflicting memory reference is blocked until the store instruction is executed, if the reference to memory is from the arithmetic decoder and follows the store instruction in sequence of execution. If the conflicting reference to memory is from the control section of memory, the memory request is blocked and the control section ceases operations until the store instruction is completed.

Memory requests by the I/O and from the control section during break-in are not compared with the address of the store instruction in the arithmetic decoder.

A method of implementing address comparison with the store instructions is to:

(1) mark the store instructions in the arithmetic decoders,
(2) determine by its position in the instruction sequence if the memory address being transmitted to memory should be compared with the store instruction (s),
(3) compare against all store instructions which have not been executed and precede it in the program sequence,
(4) if a compare is obtained, block the start memory pulse or block the data from that memory and cause the request for a memory cycle to remain unfilled.

(5) make no further requests from the conflicting address until the (or a) store instruction has been completed.

The comparison can be made by transmitting only the ones of the address being sent to the memory address register, also, to the register which contains the store type instruction's address where they are used to complement the respective bits of the store's address. A test for a comparison is made by testing for all zeros in the store's address register. After the test is completed the store's address is restored by again complementing the store's address register with the respective one bits of the address being sent to memory.

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