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PROJECT STRETCH
FILE MEMO #4

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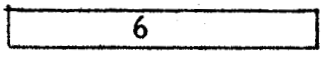
Logical rules for sequencing memory references: COMPANY CONFIDENTIAL

look ahead

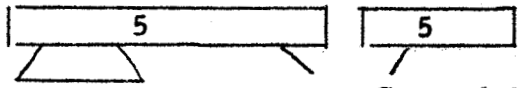
1. An order of priority is assigned to registers requiring memory references. This priority is:

   a) Input/output control register
   b) Arithmetic decoding registers - highest priority given to arithmetic instruction nearest in time to being executed.
   c) Control decoding register including the control accumulator.
   d) Program counter.

e.g.

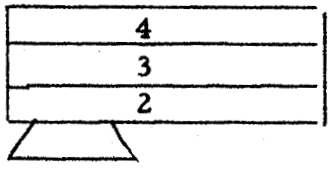


- Program Counter

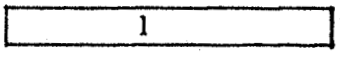


Control decoder & accumulator

Arithmetic Decoder



I/O Control Register



2. The order of priority is effectively altered by supression of references from the various registers by the rules given below:

   a) Data references called for by the instructions in the arithmetic decoder are suppressed if the memory box referred to is in use, or if the arithmetic instruction being executed is "long" relative to a memory cycle. Example - when a multiply instruction is being executed, references from arithmetic decoder suppressed and the con-

trol decoder takes precedence after the I/O control register.

b) When the control decoder is occupied and instruction not executable the program counter will discontinue calling for memory references.

3. As an arithmetic instruction goes through the control decoder, signals are generated to control memory references and are sent with the instruction to the arithmetic decoder. Instructions are classed as "Long" or "not long", requiring a memory reference to "read" or to "write", and referring to a memory box with a "long" or a "short" cycle. If an instruction in the arithmetic decoder is a "long" operation, references by instruction following the "long" instruction are inoperative.

   Only a "read" from "slow" memory may be excuted before the instruction reaches box 2 of the arithmetic decoder.

4. When an arithmetic "read" operation is immediately preceded by an arithmetic "write" and the instructions refer to different locations, the memory references are interchanged. If the "read" and "write" instructions refer to the same memory location, the two memory cycles, "write" and "read" are replaced by one cycle "write" and retain data.

5. An instruction tag is provided for all instructions that "write" in memory from the arithmetic accumulator. When this tag is inserted in an instruction, the operation of the control decoder is inhibited, and the computer operates as a sequential computer until the "write" operation is concluded.

6. When a transfer instruction is brought into the control decoder, it is executed immediately, provided the decision is not dependent on the status of the main arithmetic unit. If the outcome of the instruction is dependent on the status of the main arithmetic unit, the instruction is held in the control decoder until a decision can be made.

7. The main arithmetic unit generates 4 types of signals to control timing while executing an instruction:
   a) Permissible to start "read" from "slow" memory
   b) Permissible to start "read" from "fast" memory [1]
   c) Permissible to start "write" to "fast" memory [1]
   d) End of operation.

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1. "Write" to "slow" memory signal will be part of b or c.

8. A sequential mode of operation, that can be set manually or in the program, is provided. When operating in the sequential mode, no operation will be started until the "end of operation" signal has been given for the previous instruction. A switch is provided to put the computer in the sequential or non-sequential mode and the mode can be changed only by placing the switch in the opposite position. If the external swtich is set to "non-sequential" the computer can be placed in the sequential mode by execution of an instruction. The computer may later be returned to the non-sequential mode by execution of another instruction.

Note:

Programming sequential and non-sequential operating modes is effective only if the manual switch is set to non-sequential. If the manual switch is set to sequential, the program can not alter the mode of operation.

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