IBM Meeting concerning Announcement of New Machine

Head:

Machine Speed: 10 Miplets, arithmetic unit.
memory needs a read time of fraction of yrs to be considered
- high speed switching
- high speed memory
- media area to utilize

L. Hunter:

Finite core method

Reciprocal Sw. Time \( \frac{1}{T} \)

\[
\begin{align*}
H_0 & \quad \text{Mag Field} H_B \\
H_2 & \quad \text{Switching Time} \tau
\end{align*}
\]

Speed is limited by slope of curve; speed of motion of domain walls
- can cut size of domain walls
- can operate at high field \( H_0 \) is higher for smaller grain

Consider toroid with 2 extra holes

if \( x \) current in, \( y \) is out same as doing whole core, if current goes thru \( x \) or \( y \) only set up a local flux with small hole.
If X or Y both or pulsed, get a pulse from S.

Init. Flux pattern XYS  Final Flux Pattern

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call "coincident flux" system; old form is "coincident current" system.

with this system - no longer depended on sense of hysteresis loop,
so can use poorer loop if use plastic materials

can go to 100 mps switching time

Exp. Switching Times

\[
\begin{align*}
\frac{1}{R} & \propto 10^n \\
10 \text{ ppm} & \propto \text{square loop (8\,\mu)} \\
\text{amp ppm} & \propto \text{square loop (-35\,\mu)} \\
\end{align*}
\]
can use shaper during pulses, because of lines.
also temperature difficulties are much smaller, no moving thresholds.

But each drive line must have full current, not just half.
also actually switch some material near hole so need more power.

1/2 us include addressing, puling, and restoring.

Coincident Flex Plane

large memory timing.

0 5 10 15 20 μs

address
read
sense

can pull any one of inhibit lines then away

limitation in transit time down lines
High Speed transistors:
- Typical alloy junction transistors:

\[
\begin{array}{c|c|c}
P & N & P \\
\hline
\text{emitter} & \text{base} & \text{collector} \\
\end{array}
\]

- p-type emitter on 2 sides
- has very high p-type region; sharp boundary
- cut off freq. of transistor

\[ f_{co} = \frac{2.14}{W^2} \text{ Me} \quad W = \text{mils} \]

Susceptible to "punch thru" failure: depletion layer widens out until it touches emitter

\[ V_p = 630 \frac{W^2}{\rho} \quad \text{widths of base region} \]

Can speed up by putting a field,
- can put in a p-type field by diffusing atoms of n-type in gaseous phase

Then override this by previous alloy method

\[ f_{co} = 8 \times \frac{2.14}{W^2} \text{ Me} \quad \text{exp. quality is best} \quad W = 0.5 - 0.3 \text{ mil} \]
Need production of a transistored machine state in Jan.

Logical organization:
- do useful arithmetic longer 70% of time,
- would like joint committee to agree on final order structure of machine

Anne Dunwell

Sample Machine Organization

"slow" memory

Fast memory

Very fast memory

0.1 μs used for indices or other cases

Decimal - floating or fixed machine - address in loc. registers.

- Three arithmetic units

- Two fast memories are separate - no overall clock

- Memories are detailed serially - need not consider separately

- Word size: 12 digits + 2 exp., + sign digit

Decimal - floating or fixed machine - address in loc. registers.

Full automatic checking

Add - subtr. 0.6 μs (6 pulse times)

Mult 1.2 μs (12 pulse times)

Divide 1.8 μs

Memory: 40,000 bits

Large degree of simultaneity of parts - multiplex

Fast tapes

Selection systems (sure of transfer)
control of logic is in parallel:
- works ahead as much as possible; looking for indices, etc.
- ahead of arithmetic,
- on transfer, will go ahead on "main branch".
This multiplying is automatic - needs no special coding.

- 100 transistor triggers which record actions in various parts
of machine, overflows, etc.
- also have error triggers
- also I/O triggers (status)
- some triggers set by program
- some by console switches,
These can be interrogated in groups; patterns of logic can be
checked in one order: "on," "off," or "don't care."

Instruction Set: ~100 instructions

Address System: modified single address system
Storage: 1024 bits, 6 8-bit registers + operation bits

O.R. equipment:
- all std. IBM equipment, 1000 LPM printer, 704 tape
- and fast tape not now available, purpose: for large data problems,
- can read into any 10,000 memory, another, can be read out of another,
- while one goes on in parallel.

Speed: 2,400,000 bits/sec
20 information tracks (2" wide tape), 500 bits/inch
16% of data are information, every 5 7/8 in timing bit, go into register (4 words of data) which smoothes out timing.

Type speed 300"/sec,

compare to NORC:

4 Tracks 704 rev/min 500"/sec
500 bits/inch
142 "/sec

Question: what is information flow in & out of machine?

Can use RAM (?) fast memory or drum.

Register: Input - Input Exchange Register - transfer to register tally of appropriate high speed mem.

Card read: 500 cards/min or 1000 cards/min.
Some Comparisons of Problems:

701: 45,000 µs/peal Ching Hsi perf.
New Model: 94 µs (not counting tape2)
T0RC: 170 x more speed

Mpj 704: 240 µs 1.7 µs
Feldig + 704: 84 µs 0.6 µs

Roughly 100 times 704 speed

Automatic Programming:
Controls Ray tube (manual or camera)

Gene Amelio: Control Unit

control decoder

control acc.

conditinal

transfer into done line

3 register "stacked" of operations to be performed

memory address

can make 5 refs to memory
At one end of the area, a large group of people were gathered, discussing their plans for the day. One person, bearing a sign that read "Welcome to our community," was engaging in conversation with a group of youngsters. Another, holding a camera, was taking photos of the scene, capturing the essence of the community. A group of children, some holding colorful balloons, were playing games on the grassy area, their laughter filling the air. A few adults were busy setting up tables and chairs for an upcoming event. The atmosphere was one of excitement and anticipation, as everyone prepared for a day filled with activities and togetherness. The community seemed to have come together, ready to enjoy a day of fun and interaction.
$315M  

Selling late 1958  (39ns)  

1st quarter $100,000 per mo.  

year about 2 yrs.  

Last 12 ms,  

Expening planning, setting up production.  

Real speed gain in asynchronous nature of machine.  

Example:  

Quintus  

9  

RO MM4  

AN T.R.  

(Flowa Regents)  

11  

RO T.R.  

FL X  

12  

Ank U.  

T.R.  

13  

Lcd Control Acc  

14  

MM3  

AR  

15  

Lcd CA  

16  

MM1  

AR FL  

17  

AR  

TR  

18  

Lcd CA  

19  

MM4  

AR.  

Comments for testing: click interlocks if T.O. unit is available  

No. of Transistors:  

less than 40,000.  

(20 - 40,000 hours life seems average life.)  

Adder:  

Matrix is used.  

got add in 1 pulse time  

(650 time)  

Product Statistics:  

5 miles per month.  

2 - 3 mpy per decade.