1st STRETCH discussion

Sept 20, 1955

IBM Meeting concerning announcement of new machine

C. Heard:

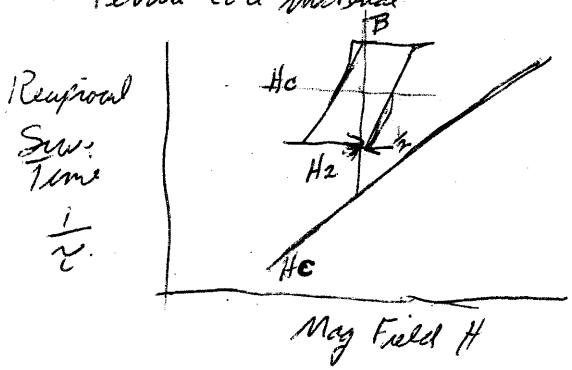
Machine Speed: 10 Mpulses arithmetic unit.

memory needs a read time of fraction of μs to be consistent

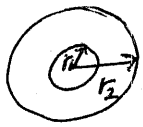
- high speed switching
- high speed memory,
- machine org. to utilize

L. Hunter:

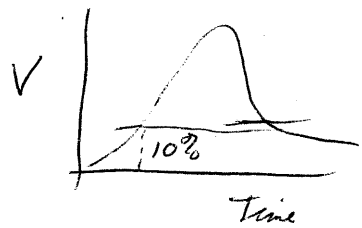
Ferrite core material



straight up to 30-40 mps



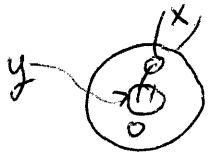
Switching Time τ = ten %



∴ Speed is limited by slope of curve: speed of motion of domain walls

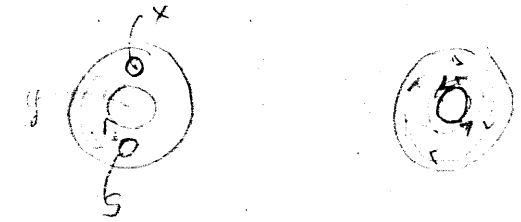
- can cut size of domain walls
- can operate at higher field Hc is higher for smaller grains

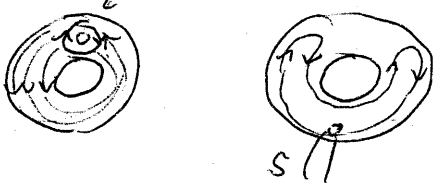
Consider toroid with 2 extra holes



if X current is in, Y is out same as doing whole core.

if current goes thru X or Y only set up a local flux path around hole.



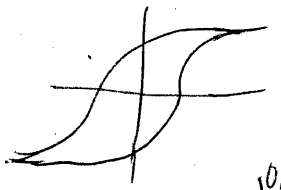


get circuit shaped flux path. does not change S appreciably,

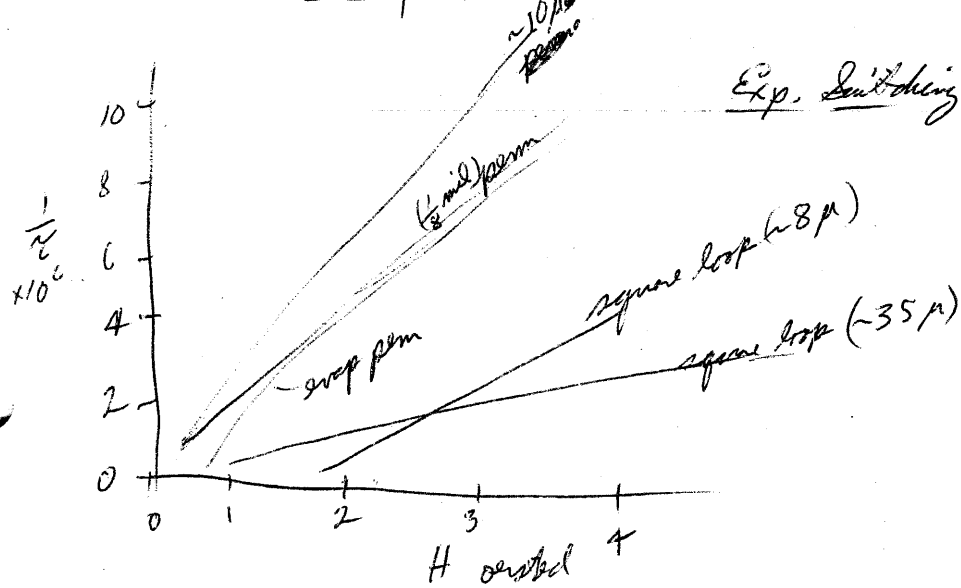
If X & Y both are pulsed, get a pulse from S,

	Initial Flux pattern		X	Y	S	Final Flux Pattern		
	inner	outer				inner	outer	
(0)	−	−	+	0	0	+	−	(1)
(0)	−	−	0	+	0	+	−	(1)
	−	−	+	+	+	+	+	(1) reading a one
	+	−	+	0	0	+	−	
	−	−	−	−	0	−	−	zero undisturbed
	+	−	−	−	0	−	−	zero disturbed

call "coincident flux" system; old form is "coincident current" system,
with this system - no longer depend on knee of hysteresis loop,
so can use poorer loop i.e. use faster materials



can go to 100 mpcs switching time

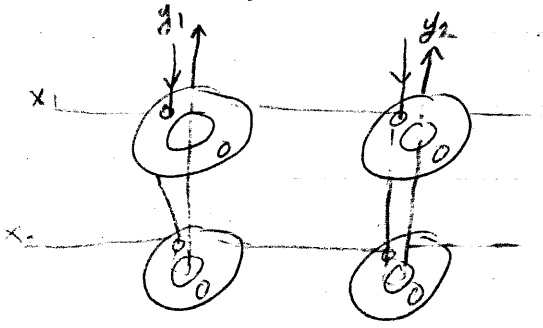


- can use sloppier driving pulses. because of knee.
- also temperature difficulties are much smaller, no moving thresholds,

But Each drive line must have full current, not just half.
also actually switch some material near hole so need more power.

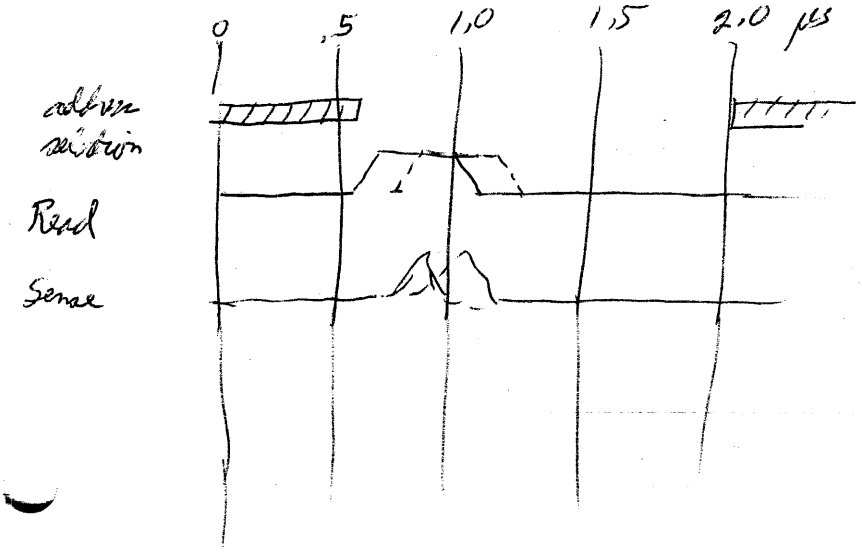
$\frac{1}{2}$ μs includes addressing, pulsing, + restoring,

Coincident Flux Plane



can put any no of inhibit lines thru array

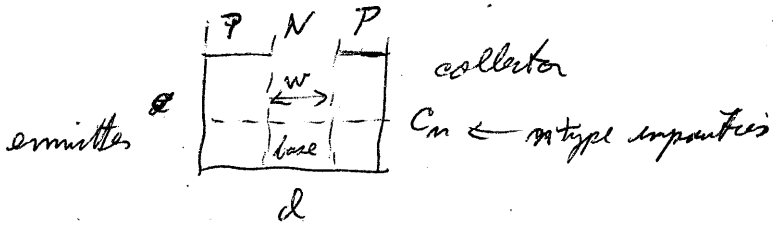
Large Memory Timing.



limitation is transit time down lines

High Speed Transistors:

- Typical alloy junction transistors:



Diffuse p type impurities on 2 sides

base very high p type region. sharp boundary

α cut off freq. of transistor

$$f_\alpha^{co} = 2.14/W^2 \quad Mc \qquad W = mils$$

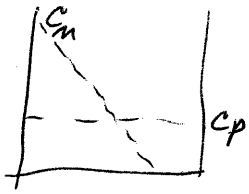
Susceptible to "punch thru" failure; depletion layer widens out until it touches emitter.

$$V_p = 630\, W^2/\rho$$

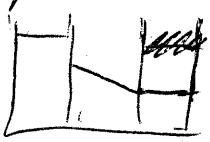
ρ ← resistivity of base region, ohm-cm

Can speed up by putting a field.

- can put in a permanent field by diffusing atoms of n-type in gaseous phase



Then override this by previous alloy method



limit is $f_\alpha^{co} \doteq 8 \times 2.14/W^2$ exp. gradient is best.

i.e. higher freq. & no punch thru. $W \approx 0.5 - 0.3$ mil

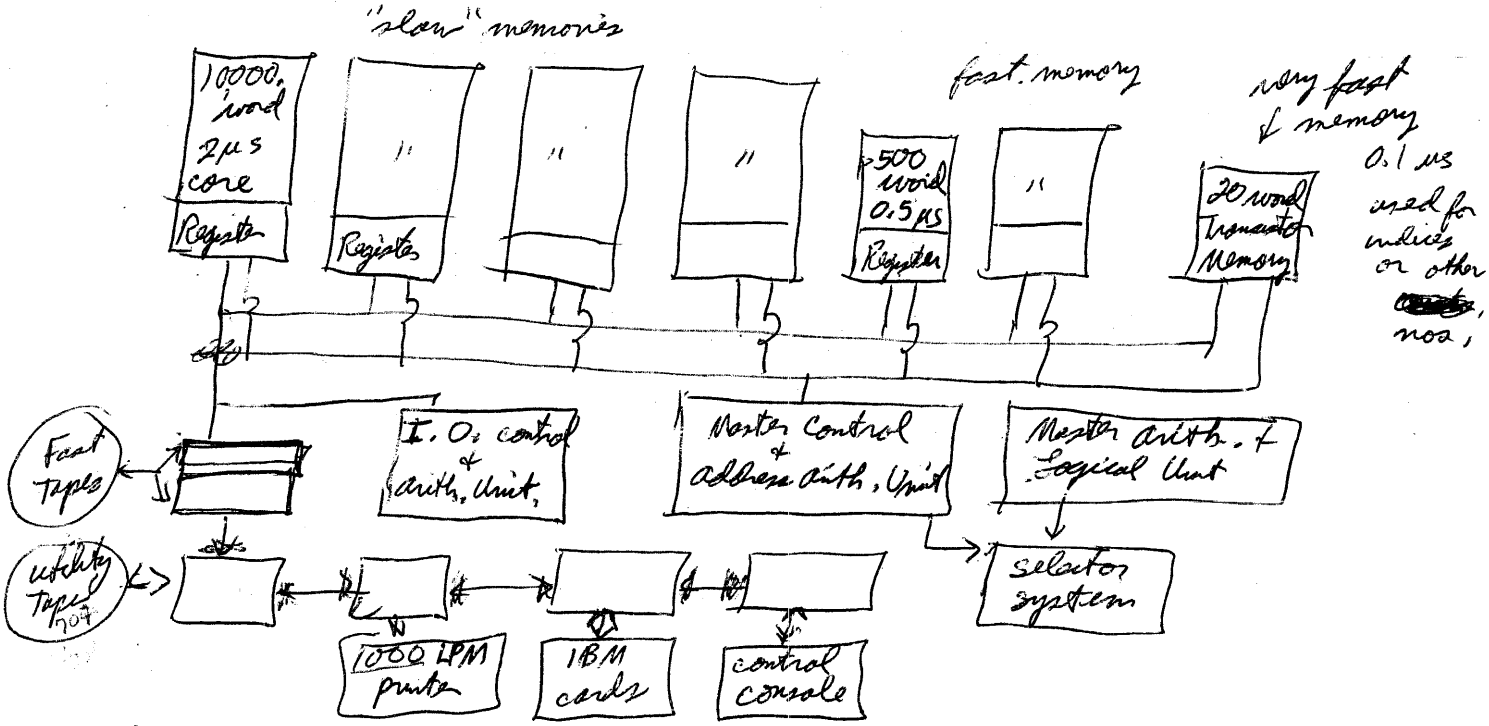
Herd: production of a transistorized Machine started in Jan,

Logical organization:

- do useful arithmetic larger % of time,
- would like joint committee to agree on final order structure of machine

Steve Dunwell:

Sample Machine Organization



Decimal - floating or fixed machine - address index registers.

Full automatic checking

- add-subtr 0.6 μs (6 pulse times)
- mult 1.2 μs (12 pulse times)
- divide 1.8 μs

memory 40,000 wds.

Large degree of simultaneity of ports - multiplex

Fast tapes

Selection Systems (series of transfers)

- three arithmetic units
- two fast memories are separate - no overall clock, can get words every 0.25 μs holds in its register,
- Memories are labeled serially - need not consider separately
- word size 12 digit + 2 sp. + sign digit

. control of logic is in parallel.
- works ahead as much as 9 orders looking for indices, etc. ahead of arithmetic,
- on transfers: will go ahead on "main branch".
. This multiplexing is automatic - needs no special coding.

- 100 Transistor Triggers which record situations in various parts of machine, overflows, etc.
- also have error triggers
- also I.O. triggers (status)
- some triggers set by program
- some by console switches.

These can be interrogated in groups, patterns of logic can be checked in one order. "on," "off," or "don't care".

Instruction Set: ≈ 100 instructions

Address System: modified single address system
Storage addr. + index registers + operation bits

I.O. equipment:
all std. IBM equipment. 1000 LPM printer, 704 tapes
and fast tapes not now available, purpose: for large data problems.
can read into any 10,000 memory, another can be read out of another, while calc. goes on in parallel

Speed: 2,400,000 bits/sec
20 information tracks (2" wide Tape), 500 bits/inch

4/5's of bits are information, every 5th is timing bit,
go into register (4 words of data) which smoothes out timing

Tape speed 300"/sec,

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compare to NORC:

4 Tracks 704 rewind 500"/sec
500 bits/inch
142 "/sec

Question: what is information flow in & out of machine?
can use RAM(?) disk memory or drums

Register: Input-Output Exchange Register – transfers to register ~~of~~ of appropriate high speed mem.

card reader: 500 cards/min or 1000 cards/min

Some Comparisons of Problems:

701: 45,000 μs/point Chemistry prob

New Machine: 94 μs (not counting tapes)

IORC: 170 × Nov. speed

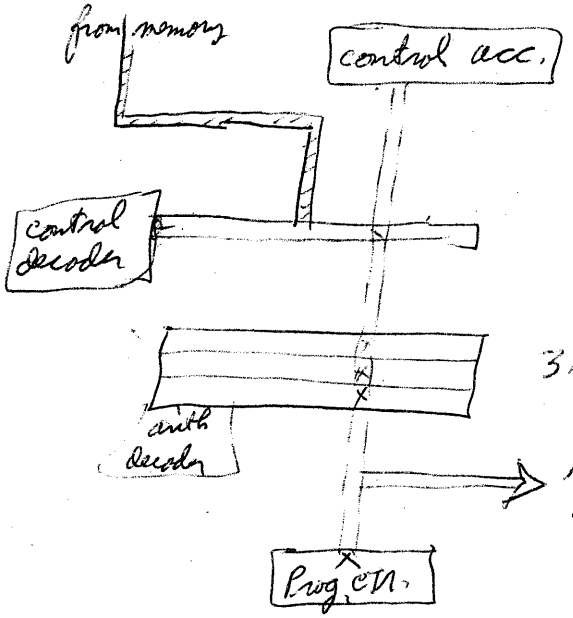
Mpy 704:	240 μs	1.2 μs
Floating + 704:	84 μs	0.6 μs

Roughly 100 Times 704 speed

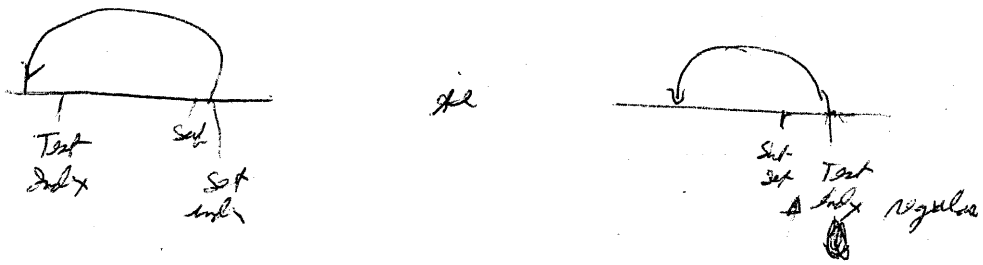
Automatic Programming:

- Cathode Ray Tube (visual or camera)

Gene Amdahl: Control Unit



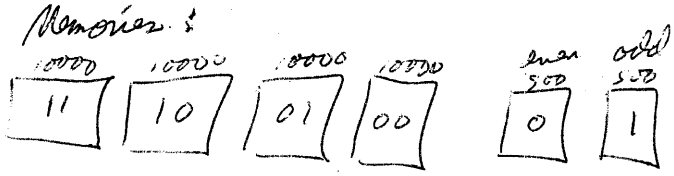
Can make 5 refs. to memory



about 4 orders in this region

Or one can ignore the above and loose the 3 or 4 palec times.

Addressing of Memories:



so sequencing addresses, one gets advantage of accesstime,

Fast Mem.	Read	Box #
FM	Write	"
LM	Read	"
LM	Write	"
Length of operation		

} These are generated in Control Decoder & passed down to Arith. Decoder & use them for rules of calling

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D. Griffith: Mesh 50×50 = 32,500 nodes

95 μs per point

0.25 sec/Δt

1000 cycles = 250 sec 4 min,

In detail 41.1 1st pass = { 7 μs address calc, 35.4 computation, 50. access time } ← These Two overlap,
53.8 2nd pass
95 μs

$\frac{35.4}{41.1} = 85\%$ efficient for one accumulator & 3 level decoder.

$3.5 M Delivery late 1958 (39 mos) Cost goes $100,000 per mo, gain about 2 yrs?
Last 12 mos, - factory planning & setting up production.

Real speed gain is in asynchronous nature of machine.

Example: Instruction

9	R.O. MM4
10	A.R. → T.R. (Transistor Register)
11	R.O. T.R. Fl. x
12	Auth U. → T.R.
13	Load Control Acc
14	$MM_3 \rightarrow AR$
15	Ld CA
16	$MM_1 \rightarrow AR$ Fl –
17	$AR \rightarrow TR$
18	Ld CA
19	$MM_4 \rightarrow AR$

Note T. Regs. for other than indexing

Commands for testing: checks interlocks if I.O. unit is available

No. of Transistors: less than 40,000,
(20 - 40,000 hours life seems average life.)

Adder: Matrix is used: get add in 1 pulse time (650 time)

Various Statistics: 5 adds per mpy,
2 or 3 mpys per divide