May 13, 1959

Mr. Bengt Carlson
Los Alamos Scientific Laboratory
Los Alamos, New Mexico

Dear Bengt:

Enclosed is a copy of the detailed specifications of the hardware changes which resulted from our recent Mathematical Planning Group Meeting.

As mentioned then the machine is so nearly complete that any changes are very hard to accomplish. We were able to do four out of the six hardware changes listed in the minutes of the meeting only with considerable difficulty.

The Exponent Underflow change was particularly difficult to do and was possible only because of a combination of "lucky breaks" in the circuitry. Even so it will have to be installed later as a correction to avoid delaying the design now--an expensive emergency procedure. We were willing to do this for Exponent Underflow because you convinced us of its importance and because we were not willing to put in a cheap but "unclean" substitute solution.

I understand Applied Programming will get in touch with Lou Gatt concerning mnemonics for the new operations, etc. I have a new set of the bar charts of I-Box instructions you requested and will mail them as a separate package.

Sincerely,

HGK:jcj
Enclosure
cc: Mr. P. Wilson
Mr. S. W. Dunwell
bcc: Dr. G. A. Blaauw
Mr. E. Bloch

H. G. Kolsky
Project Coordinator
Project 7000

SUBJECT: Changes in STRETCH Resulting From the Mathematical Planning Group Meeting, April 27-28, 1959

The information in I, II, and III below is extracted from three memos written by G. A. Blaauw, dated May 11 & 12, 1959 defining the hardware changes to be included in the STRETCH design:

I. Miscellaneous Changes

1. In single precision operation, accumulator bits 60-63 remain unchanged rather than set to zero as specified previously.

2. Indicators 41-47, the Harvest indicators, will be available for the programmers' use.

3. A change in the TRANSMIT and SWAP instructions involving:

   a. Bit 55, when zero, specifies positive incrementing of addresses; when one, negative incrementing of addresses.

   b. Half word transmission is deleted.

   c. Immediate counting is for 16 words maximum, not 32.

II. Exponent Underflow Changes

1. True Zero Handling will be incorporated.

2. In order to abide by the present schedule and meet delivery dates, the design of the computer may proceed without actually building in True Zero Handling at this time. If not built in now, the necessary changes will be made later as machine corrections.

3. A consistent and complete method of True Zero Handling, as specified below will be described in the Preliminary Manual of Operations.

4. Those details of True Zero Handling which permit alternate solutions will be adapted to the machine design in order to minimize the redesign effort. Since these details are of second order importance to the user, they will not be specified in the manual until the actual design is decided.

III. Description of True Zero Handling

1. Floating point numbers with exponents ≤ -1024 and zero fraction may be considered true zeros. These numbers are contrasted with floating point numbers with zero fraction and exponent > -1024, which represents an order of magnitude. Exponents ≤ -1024 should not be used with non-zero fractions.

2. The action of the computer is such that consistent results are obtained when true zeros are used as operands in floating point operations as follows:

   (1) Loading or storing of a true zero operand yields a true zero result.

   (2) Addition of a true zero operand to a non-true zero operand yields the non-true zero operand as a result. Addition of two true zero operands yields a true zero result.

   (3) In comparison, the magnitude of a true zero operand is considered smaller than the magnitude of a non-true zero operand. The signs of the operands are inspected in the normal manner to yield a high or low indication. Two true zero operands are considered equal.

   (4) Multiplication by a true zero factor yields a true zero result.

   (5) A true zero dividend yields a true zero quotient and remainder. A true zero divisor gives a program alert.

   (6) The square root of a true zero is a true zero.

   (7) Operations on parts of floating point words, such as exponent addition or fraction shifts, ignore the true zero definition.

   The computer action consists in recognizing exponents ≤ -1024 (not zero fractions) in operands and making the exponents of the result ≤ -1024 where necessary.

3. The program is alerted by indicators for all results which have exponent $\leq$ -1024 which are not derived from operands with exponents $\leq$ -1024, as follows:

   The indicators XPN, XPU and RU will be turned on for the proper result exponent range, provided none of the operands of the operation are $\leq$ -1024.

   The indicators can be used in reconstructing the proper exponent result. The programmer may use the results as true zero operands in subsequent operations by making the fractions equal to zero.

4. Results which are derived from operands with exponents $\leq$-1024 will not alert the program.

   The indicators XPN, XPU, RU, and PSH are not set to one if any operand has exponent $\leq$-1024.

IV. Changes Suggested in the Meeting not being Made

1. Floating Point SWAP with accumulator
   This instruction cannot be included because it would involve a combination of floating point and VFL data paths which are unnatural to the present design. Although the operation bears some relation to Floating Add to Memory, the sequences would be quite different and no faster than the three half word ops necessary to program it. (They are: LFT M, ST M, L $FR).

2. Load Exponent and Load Exponent Immediate
   Although these would have been easy at one time they cannot be done now because they would force a complete redesign of the floating point op code decoding network. This plus the fact the operation can be done quickly by two half-word orders (E- $L, E+ M) ruled against making the change.

H. G. Kolsky

HGK:jcj