MEETING OR CONTACT REPORT

Date of Report: November 20, 1957

Organization & Location: Los Alamos Scientific Laboratories - IBM Poughkeepsie, New York	Date: November 14-15, 1957 Reported By: H. G. Jones
Project: STRETCH Mathematical Planning Committee Meeting # 11	Department: 749 Follow-up Date:

PERSONNEL PARTICIPATING:

LASL	IBM Engineering	IBM Product Planning
Mr. D. Woods	Mr. W. Buchholz	Mr. D. W. Sweeney
Mr. R. Lazarus	Mr. G. A. Blaauw	Mr. E. F. Codd *
Mr. R. Frank	Mr. F. P. Brooks	Mr. H. G. Jones
Mr. M. Wells	Mr. S. G. Campbell	Mr. H. G. Kolsky
Mr. J. Whorlton	Mr. P. Herwitz	
Mr. B. Carlson	Mr. S. W. Dunwell*	IBM Applied Science
Mr. E. Voorhees	Mr. J. Cocke*	Mr. F. Johnston

Mr. Dunwell opened the meeting with an encouraging report on the progress of component manufacture.

He pointed out that detailing the machine must begin immediately if schedules are to be met, and asked the committee to finalize specifications at this meeting.

Specifications were discussed at length. Particular attention was paid to the concern of LASL that, since the machine will have only 15 index registers, those Registers be made as efficient and flexible as possible.

Four lists are appended of decisions reached regarding machine specifications. These lists are a part of this report.

A list is also appended of those errata and addenda to the preliminary manual which were proposed by the committee in session.

IBM pointed out that Chapter 10 of the preliminary manual is only a draft and is subject to considerable redefinition.

*Attended part of the meeting.

IBM solicited further information from and discussion with LASL regarding their requirements for miscellaneous low-speed I/O units.

Agreement was not reached to include or finally exclude a few facilities of the Direct Indexing type. LASL agreed not to press for inclusion of these facilities, reminding IBM that they would be watchful of the proper fulfillment of Article VI, section 2. b. of the Contract, which reads:

> "The computer system to be delivered hereunder will contain adequate space and power for the later inclusion of a reasonable number of additional commands."

IBM pointed out that any additional commands would not be permitted to involve appreciable logical reorganization, i. e. they would necessarily be truly additive, and that the principal limitation on the quantity of physical space left in the machine is the effect on machine speed of increasing the volume. It was agreed to include the above - mentioned Section in the Preliminary Manual, and to take other precautions necessary to ensure that all engineers keep this Section in mind while building the machine.

It was agreed that the decisions reached in this meeting be the final amendments to the machine specifications produced by this committee, subject to formal review with the AEC Contracting Officer. It was also agreed that such formal review be postponed until firmer details and performance figures are available.

Since the committee has now concluded that part of its business requiring regular monthly meetings, the next meeting is to be called approximately 90 days from the date hereof. Continuing personal contact by individuals is encouraged.

With the distribution of some sections of the Preliminary Manual, all parties were enjoined to maintain the company confidential nature of material therein.

Mr. Dunwell closed the meeting with a tribute to the LASL contingent, expressing IBM's appreciation for their indispensable contribution to the design of STRETCH.

Distribution

Mr. B. Carlson (10 copies)
All IBMers who attended meeting
Mr. B. Moncreiff
Mr. E. Coffin
Miss E. McDonough
Mr. J. C. Gibson

I It was agreed that the machine should include the following features:

1. In a Bring-Type floating point operation such as LOAD, when the effective address specifies the upper accumulator, the data read out shall be $(A)_{0-59}$ and $(AB)S_{0-3}$, which is normally a correctly signed floating point number. When the effective address specifies the lower accumulator, the data read out shall be $(AB)_{64-127}$, which is not normally a valid floating point number in standard format.

2. In a floating point operation of the STORE type, the sign modifier shall not affect the accumulator, only the number as it is deposited in memory. This is in contra-distinction to the normalizing modifier and the ROUND AND STORE instruction, both of which operations necessarily modify the accumulator itself prior to the storing operation.

3. When, in floating point addition, complete cancellation of the mantissa takes place, the exponent will be reduced by 48 while the mantissa remains zero. (Also see list III number 4.)

4. A COMPARE COUNT instruction shall be included with full 4-bit I and J fields and with a full 19-bit address part. The exact method of introducing this to the vocabulary is at the discretion of IBM.

5. The modifier which determines whether a BRANCH instruction affects the indicator on which it is branching shall operate on the basis of a RESET rather than an INVERT. Thus, a branching operation with the reset modifier on shall reset to zero the tested indicator, regardless of its previous condition or of which of the two conditions is being tested for.

6. A RELATIVE BRANCH shall be included, whose effective branching address shall be its address part plus the contents of IC plus the contents of I.

7. A RETURN BRANCH shall be included having a full 4-bit I field. The index register specified will index the branching address. Store IC cannot be accomplished. The instruction will not affect the interrupt status (but see list III, number 3.)

8. A STORE ADDRESS shall be included whose purpose is to deposit the V field of an index word in the address part of another instruction. Since A fields have different lengths, it is necessary to read out the addressed location, analyze the operation code contained therein to determine the length of the A field and then switch in the required portion (0-17, 0-18, or 0-23) of the V field of the specified index. V is thus "cut to size" before storing.

9. Sufficient physical space shall be left, when the machine is laid out, to insert a reasonable number of such miscellaneous operation codes as may be found necessary by further analysis.

II It was agreed that the following features should be included in some form, but that precise definition follows some further study:

1. Some method of properly recording flow of control through both branches and interrupts, such as a PATHFINDER register. After any branch, a pathfinder contains the value held in IC before the branch, which may then be stored by the transferred-to section. Some such facility is necessary, inasmuch as IR 1 is overtaxed when a branch is followed too closely by an interrupt.

2. The Interruption Enabling Mechanism was found to have some apparent inconsistencies with respect to I/O and WAIT operations. Enabling and disabling conditions will be restudied, and redefined if necessary.

III The following features will be studied further, their inclusion being conditional upon the results of that study.

1. Multiply and round in floating point.

2. Divide and round in floating point.

3. A return branch (see list I, number 7) and enable, so that this instruction may be used as an exit from an interrupt fixup routine.

4. In noisy floating point, after an addition causing complete cancellation of the mantissa, whether the inversion of result bit 58 shall be included as usual or suppressed.

IV The following specifics were discussed and rejected from the definition of the machine:

1. Form effective address, which would have modified the succeeding instruction, was found to raise too many awkward situations for the advantages it offered.

2. Transmit index was found to save only one memory reference in the rare case when all indices required redesignation. In all other cases, when it might be used because of programming ease, it would make the program less efficient.

3. Block store zero (or other constant) was found to be readily fulfilled by one store and one transmit instruction.

Errata and Addenda to Preliminary Manual

1. Page 4.10, 11. Cancel Status:
   For: Status indicators (11-16)
   read: Status indicators (11-15)

2. Page 4.12, 22. Instruction Location Match:
   This section shall be more precisely defined.

3. Page 4.12, 23. Instruction Location Non-match:
   For: bit 23
   read: bit 22

4. Page 4.12, 25. Effective Address Non-match:
   For: bit 25
   read: bit 24

5. Page 4.15, 41. Exponent Underflow:
   For: Exponent $< -2^{11}$
   read: Exponent $\leq -2^{11}$

6. Page 4.17, 55. Index Comparison Result Equal Add:
   A comparison of -0 with +0 is considered equal.

7. Page 4.19, 4.4.3 The Mask Register:
   For: bit 16
   read throughout: bit 15

8. Page 7.6, 3. (list of unaffected commands)
   Add: 7.3.23 ADD EXPONENT

9. Page 7.8, 7.3.2 STORE, item 3:
   For: replaces AB (S)
   read: replaces C bit 60
   Same section, final sentence:
   Delete:.... modify the accumulator sign or.....

10. Page 9.19, 9.8.1 Disabling of Interrupts
    Delete last sentence: Further interrupts.....
    ....all interrupts.