LA-IBM STRETCH Meeting: Nov 14, 1957

Br to 0 all zeros.

- illegal addr,
  no. op? if masked, —?

stop button?
mem. clear button?
load button — masks

(Dunwell) components:

- sm. transistors production in Jan
- quality on pilot line very good. PNP 50% useable
- core driver transistors (small germ. only) several hundred in Jan.
  - 5 amps in 50 mps switch required.
- packaging - plugable units { 2 methods being studied. — 2 or 3 mths to decision. logical blocks are worked out.
  - problem: oscillations over 100 Mc.
- Must start detailing machine now to meet schedules ... must have frozen design. must firm up specifications now so that after this meeting, hardware considerations are main ones.

— are moving to new Bldg now.

(Sweeny) Fl pt.: Double precision add — carry problem

have defined: 1. 49 bit
2. Single + Double → Double.

— Eff. sign fields — bit shifted off { than error of 1 in last place }

Com Mpy — still tentative.

Sign Modifiers Fl pt - accumulator is changed.
Integer - " not changed.

Loading from accumulator (+ other ops) get sign properly
seems important

makes accumulator a unique loc?
- sign modifiers should leave acc alone particularly on store
what about normalize + store - do change acc.

- low order B 20 bits need VFL to change...

Store tag bits come in to C register on load.
Store ships out from C.
add to Mem replaces tags to Mem.

— 0 mantissa — large exp.

IBM will look into — question of Mpy R. (also Div R) — should be looked into — people will not round if it takes extra op.
[on Maniac - if round causes spill - omit the round] — O.K. Mathematically - may be easier hardwarewise.

Sq. Root - may be single only. — seems to be in definitely - - .

64 bit register to test against — instead of 20 bits.

Acc (AB)
Sign Reg (8 bit) also other. acc.
Mask Reg.

Exchange: End of op. suppress — new 4 op codes instead of modal

33rd channel --- low speed channels — a future expansion.

{ 32 channels can have low speed units — how does one connect typewriter — paper tape — etc ?
IBM will furnish standards (such as summary punch)

— ask LosAlamos for details on what they want to connect —

178 people on STRETCH now

question of determining ~~last~~ exchange is all through ?
— table of ops. by ~~mon~~ monitor prog.

Has exchange been examined carefully — in/out programs been examined carefully ? — reject interrupt — one can blunder & and make mistakes ~~and~~ and lose

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Indexing:

Geo. 0 refill ... ~~order~~ order is important.

Direct Ind. Format

— pros + cons : ~~left~~ left-right
{more ops

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load indirect needs rt. + left

Desire: to be able to store V's, Δ's, etc in half wds. — tables.
— all but load + store full — need half wds only —
— storage in high speed regs.

(Rogers) 1. orderly procedure – going thru table – makes no diff
2. out of order – (would have to have a 1 in 19 extra)
probably out.
The index order has 19th bit so can go right or left.

– concerning large arrays
duty cycle – need on high duty.

New ops desired:

Direct: Compare C vs indexed table. (C vs interface) (highest priority)

– be able to make V + C go in opp. directions.

load, store R in misc. field.

Want Symmetry Incr + Dec, count up or down.

– out + back would need two tables

→ Most serious limit is still the no. of index reg. allowable
should make index field

1 Ds compare C (vs V of E)
2 Count down/up
3 Decr./Incr ±Δ

could omit count up in integer case.

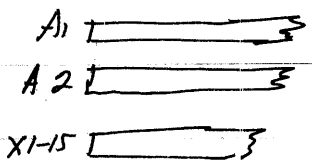
(afternoon) Indexing Questions:

✓ (1) Direct compare count

X (2) count up/down

X (3) V ± Δ

X (4) Transmit Index registers — Full Wd.



give A1 + A2 + a count

(1) store all 15 in A2 ff
Bring all 15 in A1 ff

(2) also give no. of indices

(3) geometric.

X (5) "Continue" bit,

clear as ie — flag bit in index — indicator goes on

If continue bit = 0 exit from loop
" " = 1 chain — saves a branch op.

X (7) modify V by c field. { decrease / increase

✓ (8) Transmit zero. (or const if possible)
— don't move up fill indexing on 1st addr.

✓ (9) Skip type op. (rel. unc. branch)

→ ✓ (10) Unconditional Branch with 4 bit I field. .. return branch

Worth considering → ✓ (11) Store address to next instr. — would need to inhibit interrupt,
ie Form off-Addr

✓ (12) Branch (insert/clear) or reset zero.

X (13) Block Swap of index regs

? (14) Count on up to 20 or more transmit . . ?

? (15) Path finder register

We agree to (1) block store zero,
(2) Reset to zero,
(3) put in Relative Unc. Branch (in c+Br format)

Misc: Store V in W addr. (either 18, 19, 24 dep. on form of instr)
(Fl)(Div). Compare C direct
Unc Br: Relative Branch