

LA & IBM Meeting:

Thurs AM

Oct 18, 57

Los Alamos Says

I. Symmetry of OA + index SA + index, more
simp - than 12 bit I Field,

II. Full rod, symmetry 6 Bit natural

Lowest half rod - indexing becomes hard ^{rel to} to 16 registers.
larger generality & flexibility,

In full rod decision - groundrules were dropped in going
to 1/2 rods, - minimum format - 12 bit index field - field
of code formats,

Preferences between full rod - half rod

↑
more flex. simpler, - fewer compound
& power in indexing,

Pr. & Store loc. counter,

Convenience in Coding in large problems
Simplicity in Thinking need flexibility

Operational Definition of Weights: - years of experience - gives feeling"
- proof

- don't want machines to be "tricky" for every one.

- This present IBM format is ^{at least as} good as old full word format but either of LA formats are better than any of the others.

Geometric indexing -----

) ~~A~~ Important difference

gemt: Description of IBM

IBM Philosophy: - can use any mem loc. in a full word (2 halves)

----- e.g. geometric index - question of what is ^{more & less} important.

question of Immediate Index: - bit address

End: very-very useful

Register: half word only.

) ~~A~~ Imp. difference

Register → (Load Geom: question of using 15 + 3 others as modifiers of some sort. ?)

we have assumed half word index reg - single vocab -

could use complicated vocab. just as well - here as in full word.

need not increase vocab for full word ind. regs?

Re Name Store C(II) → C(CI)

Load W → C(I) (name)

Load C(W) → C(II) (value)

} use any mem loc. for index

Branch: — almost complete agreement.

leave or set to zero.

better to say leave or invert, conditional invert,

Chain indexing — not vital

Brook

- Geom:
1. at 16 insufficient compared
 2. geom indexing on every fl. pt. instr.
 3. if ^{it} have do 4 bits vs 6 bits?

Points for geom every other.

1. Will increase code.

2. Convenience to coder.

3. Looping back is dangerous if may be ^{r, s, t} or r, s, t

conceptually →
better speed
speed penalty

Worlton: (comparison) of LA & IBM half wd

1. 6/4 bit index in correct format

2. 2 vs 3 index addr. on transmit format

3. 64/192 Floating point ops, Floating

4. Dir. Geometric⁶ + 63 index vs Geometric¹⁸ + 15

→ SLA can have an order
to also load also.

(Conditional Br.)
are same

Fixed fields
this is worst →

5. Indexed-Indexing } Full wd vs half wd
LA IBM

6. 25 bit immediate

7. Full wd. Index vs half wd index

8. Direct-Indirect in Fl Pt. vs. general indirect loading, etc.

1 & 5 are almost incompatible

LA Full word answers all the above

(Fred.) \rightarrow compound with orders are redundant \leftarrow extra decode time, 2 adds, multiple...

(2) - Simplicity of putting 2 halves together -

code length - compensation -

| | | | |
|--------|----------------------|------|---------------------|
| Kaloby | (1) Full no prepost | 1.0 | |
| | (2) Full pre or post | 0.71 | $\downarrow 29\%$ |
| | (3) Half with "name" | 0.61 | $\downarrow 18\%$ |
| | (4) Present Half | 0.53 | \downarrow (0.55) |

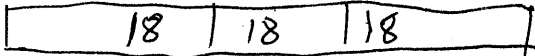
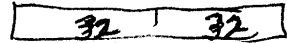
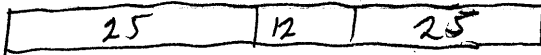
try with Pre store, Post load

Friday:

Bit efficiency — but restrict future changes.

Store effective address — order — — some is load gen ...

Index Registers Full or half?



would rather have full with two fields than 2 halves.

V A L

which?

V C L

V C R

V L R

L = 25

R can be 18

count can be 18 ..

1. V=25 L=25 R=12

2. V=25 L=25 unused (12)

1, 2, 6, 7

3. V=25, C=18, R=18

3, 4, 5, 9

4. V=25, L=~~18~~¹⁹, ~~18~~ Δ=19

5. V=25, Δ=~~18~~¹⁹, C=~~18~~¹⁹ ← in Δ bitaddr?

6. V~~25~~, L=25, Δ=12

~~V=25~~ ~~V=25~~

7. V₂₅, L₂₅; C=12

10. V₂₅, Δ₂₅, C₁₂

8. V₂₅, (op. code determined)₃₇ (eg #3, #4, #5)

9. V₂₅, L₁₈, R₁₈ (exchange)