PRODUCT PLANNING & MARKET ANALYSIS DIVISION

IBM

MEETING OR CONTACT REPORT

70-6076-0

Project: STRETCH Mathematical Planning Meeting # 7	Date of Report: July 3, 1957
Purpose of Meeting or Contact:	Date of Meeting or Contact: July 27, 28, 1957
	Reported by: John E. Griffith
	Dept.: 749, Product Planning
Place of Meeting or Contact: ☐ WHQ ☐ Phone Other:	Follow-up Date:

List Personnel Participating
Give Report (including next action)
Indicate Distribution

Participants:

IBM	LASL
Mr. G. A. Blaauw	Mr. B. Carlson
Mr. J. E. Griffith	Mr. I. Cherry
Mr. F. E. Johnson	Mr. R. Lazarus
	Mr. E. Voorhees
	Mr. D. Woods
	Mr. J. Worlton

The meeting opened with a discussion of the memories. IBM reported that there was no new information on the state of development of the memories. LASL wished to make clear their feelings on possible memory configurations:

1. LASL believes that the number of boxes of 2.0 usec memory is more important than the number of words in a box. In particular, 4 boxes are required for multiplexing. In case the boxes have a large number of words, LASL does not wish to be bound by the amount of memory stated in the contract (32,000 words), because they wish 4 boxes of memory, regardless of size. In any case, they do not want to approach the AEC for more money for memory in order to get a total of four boxes.

2. It is generally felt that 0.5 usec memory is much more important than 2.0 usec memory and that a possible solution might be to put all memory and look-ahead money into 0.5 usec memory and depend on Disks or Tapes to extend the memory. This would depend on the relative costs of 0.5 and 2.0 usec memory and the expense of the look-ahead system.

Mr. R. Lazarus reported on some coding comparisons between present day machines and Stretch. His conclusions (all of a preliminary nature) :

1. The number of instructions for Stretch to do a job is about the same as the 704, but the Stretch instruction is 64 bits versus 36 bits for the 704.

2. Skips are often as good as Branch instructions when there is no room for the Branch address in the instruction.

3. Pre and Post - store are useful to reduce the number of instructions. In a sample case, 13 out of 21 arithmetic instructions had used Pre or Post - store.

4. There is need for an order which interchange the contents of two locations in either memory or registers.

FORMAT

LASL presented a proposed format for IBM consideration:

Bits	
20	Word Address
12	Second Address
12	Index Address
1	Index Address Designator (Geometric or Direct Addresses)
1	Blank
1	Operand Address Designator - floating pt. only (Direct or Indirect)
1	Address Interchanger - reverses role of WA and SA
8	Operation Code and Sign Modifier
2	Blank
2	Second Address Use Designator (Preload, Poststore, etc.)
2	Second Address Index Address (Geometric Only - to index second address, etc.)
2	Breakpoint and Programmers Tog

It is assumed that the WA and IA will always be tied together; also, the SAIA will be tied together.

This format generally coincides with the thinking of the IBM Planning group, so little discussion was necessary.

IBM stated that two features of the LASL format were questionable:

1. Indexing the SA as well as the WA
2. Reversing the use of WA and SA.

It was promised that the feasibility of these two features would be considered.

MEMORY ADDRESSING

LASL stated that they thought that the memory addressing should be continuous from 0.5 to 2.0 memory.

LASL is willing to accept the blocked out addresses in the low order part of the 2.0 usec memory, but asks if a special Transmit command can be included so that the blocked out portion may be used as a solid block for intermediate storage. This command would allow data to be moved as a block into and out of the blocked out portion, but would not imply that any other references be made to it.

MISCELLANEOUS OPINIONS

There is a strong objection to stripped I/O units, in particular to reading cards row-wise.

All Selector operations must be optional as to turning off the Selector when testing it.

Manual switches are desired by some for operator intervention.

The Sign Modifier need not include the absolute value mode as absolute values are not needed that often. An alternate specification:

1 bit for operand sign
1 bit for answer sign

A secondary operation code for use within Second Address would increase the usefulness of the 64 bit instruction.

TSX instruction need not store in an Index Register, but could store in a special register - this would free an index register in many cases, for it would not be necessary to store the IR for later use.

The Instruction Counter +1 may be stored is a special register upon any discontinuous break in the sequence. This could be used later programmed for returns and for breakin returns.

Chain Indexing is heavily favored as an adjunct to the present modes of indexing.

If tag bits on data or instructions are to cause interrupt, the action should be taken after the completion of the operation, not before.

A special Store Address order is needed to store an Effective address in an IR.

Integer arithmetic appears to be satisfactory in the B machine, if it sufficiently flexible.

Provision should be made to test and Branch on the condition of a bit in memory without altering the contents of any of the Arithmetic registers.

There is a need for TXI type instructions. A possible format:

WA	IA	SA
Δ	Tag	Tr

This instruction increments, tests against limit, and Branches to SA. Skip may be acceptable if there is not room for a Branch address.

It is generally felt that the Branch address should always be in the SA field.

A separate set of 64 programmable triggers is highly desirable. Decisions on these would often be used to trigger I/O, restore, etc.

Should bit addressing be done with double indexing only?

Los Alamos gave the following answers to questions posed during their visit to Poughkeepsie in June, 1957.

(Questions were posed to LASL at Meeting # 6, June, 1957.
Answers given at Meeting # 7, June, 1957)

Q. Is it acceptable to have instructions of the pre-load, post-store type apply to floating point type instructions only?

A. Probably.

Q. Is it a sufficient advantage to have only multiple accumulator operation and not pre-store, post-store, pre-load operations?

A. Two op. codes with mult. Acc. may be better than pre & post store.

Q. How large should the second address be?

A. 12 bits

Q. Is it acceptable to have geometric indexing for floating point operations only?

A. Not very important.

Q. What is the smallest number of index registers acceptable?

A. 10

Q. What is an optimum?

A. 12

Q. Would it be desirable to address high-speed registers both as geometric indices and multiple accumulators?

A. Very necessary.

Q. If the operand address would not span full memory, what size of address would be acceptable?

A. No agreement; but if not 20, 16 minimum.

Q. Is it acceptable to concentrate the effort of obtaining very high-speeds upon floating point arithmetic rather than other data manipulations?

A. Indexing, Branches should be fast.

Q. Is the floating point format acceptable.

A. mantissa	48 + 1
B. exponent	10 + 1
C. tag bits	4

A. Acceptable; 1st, 3rd, 5th bits of exponent should be tagged.

Q. If it were possible to use and specify variable field length floating point operations, would this be useful?

A. Not unless free. Saves storage only - not time.

In closing, LASL agreed to try evaluate by programming the following features:

1 - Address Interchange
2 - Indexing on SA
3 - Mult Accumulators or Pre and Post store
4 - Decision procedures and use of indicator bits
5 - Tag bits on data
6 - Chain Indexing
7 - Branch addresses in SA only
8 - Compound orders (extra A, S, M, D opns)

IBM agreed to investigate the Look Ahead decoder to see if short loops could be completely contained so that memory references for the instructions would be eliminated until a Branch is taken out of the loop.

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