Harwood

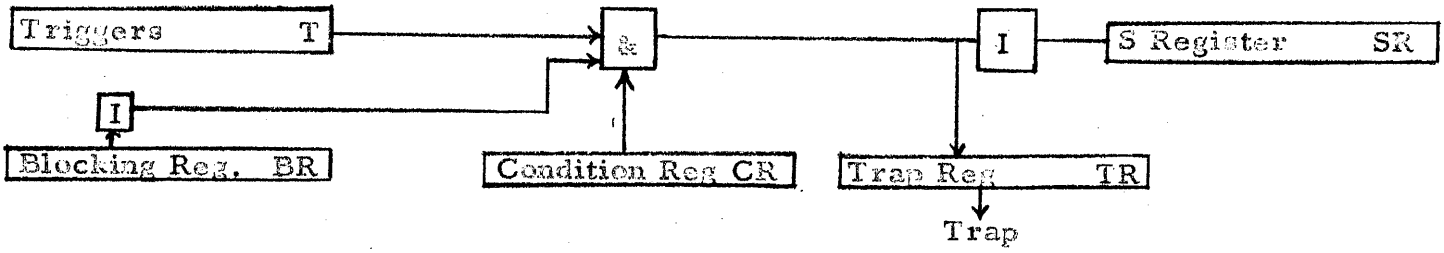
TESTING FOR UNUSUAL CONDITIONS IN STRETCH

Triggers will be turned on for any unusual condition such as overflow, underflow, division by zero, etc. A condition register may be set to cause the program to trap out when a trigger goes on. If a trigger is turned on and a matching bit in the condition register is a one then the trap becomes effective. On the other hand, if a trigger is turned on and the matching bit in the condition register is a zero, then the trap does not take place and a bit is placed in the summary register. If it is desired to set the trigger without effecting either the summary register or the trapping mode then a bit is stored in a blocking register which blocks the trigger from testing with the condition register or changing the summary register.

DEBUGGING: The condition register would be set to zero. At appropriate places in a program the summary register will be tested to see if any unusual conditions have occurred which were not trapped out. The procedure would be to place the contents of the summary register in the condition register and rerun the last section of the program. When the program is rerun a trap will occur on each condition and a sub-program will print the contents of all registers concerned which caused the condition. After the program has been debugged there will probably be certain conditions which one would not wish to trap in certain sections of the program. If any condition is not to activate a trap it will be blocked by a bit in the blocking register.

A test operation will test the summary register, set up the condition register and the blocking register in one instruction. This instruction will be executed in the first decoder, and it will also place the decoders in a sequential mode if the summary register is not zero.

SUMMARY REGISTER TEST OPERATION



i = bit in register

$$T_i \times \overline{BR_i} \times \overline{CR_i} = SR_i \times \overline{Trap} \times \overline{TR_i}$$

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$$T_i \times BR_i \times \overline{CR_i} = \overline{SR_i} \times \overline{Trap} \times \overline{TR_i}$$

Test operation would consist of the operation, an indicator bit, and 3 adrs.

Bit	Test Operation	Adr A	Adr B	Adr C

If Bit = 0 Clear summary register

If Bit = 1 Do not clear summary

If SR = 0 Go to next instr and load CR from contents of word stored at Location C. Also load blocking register from contents of word stored at Location B.

If SR ≠ 0 Go to instr at A and OR the contents of the CR into the BR, load the CR from the SR.

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