RULES USED ON "$\sum_{j=0}^{2} a_{ij} b_{jk}$ and next outer loop" 10/26/56 (referring to p.6)

1. Start FM reference for next instruction .2 μs before end of last IM reference made by present instruction and no sooner than .1 μs after the loading of the present instr. into level 4 of the Decoder Buffer. (See description of Transfer operations.)

2. M.Mem. RO can be initiated only from Decoder Buffer level 2 or below for Arith instrs.

   M.Mem RI can be initiated only from Execution Control level for Arithmetic instrs.

   FM RO and Temp.Reg. RO will be started .2 μs before end of present Arith. execution.

   FM RI and Temp. Reg. RI is same as M.Mem. RI.

3. All address modification is done in level 4 of Decoder Buffer. The instruction must reside in level 4 for at least .1 μs and may then drop unless address modification is being performed, in which case it can drop after the beginning of the last indexing operation.

4. The temporary (Storing) register (Temp. Reg.) is assumed to have its own bus line distinct from the IM bus. In addition, it is assumed that the Main Mem. and FM have separate bus lines.

5. IM RO. It has been assumed that the word from IM is available after .1 μs. It has further been assumed that fixed point addition take place during the second .1 μs of the .2 μs fixed add time. Hence the overlap yielding the time of .2 μs for forming the effective address for a_i (and .4 μs for a_{ij}).

6. Transfer Operations. During the .1 μs following the loading (4) of an instruction into level 4 an examination of the instruction is made to determine if it is a tranfer type before initiating the reference for the next instr. If it is not a transfer, then 1 is added to the instruction counter and reference is started for next following instr. If it is an unconditional transfer, then proper ref. for next instr. is made. If it is a conditional transfer,

RULES USED ON $\sum_{j=0}^{2} a_{ij} b_{jk}$, etc (CON'T.)

then one plays the probability of the condition for transferring being satisfied and makes the reference for the next instr. on the basis of the address. The "next instr." may be allowed to enter level 4 and be indexed, etc. but may not leave level 4 or be executed in any way until the condition is known to be satisfied. If the condition is not satisfied, this next instruction is "killed" in either FM or in level 4 and reference for the correct next instruction is made. (Note the killing of 1''' at 9.4 μs in FM, and the reference for 6 (also at 9.4 μs.)

$\sum_{j=0}^{2} a_{ij} b_{jk}$ and "next outer loop."

E. VOORHEES 10/26/56
(LASL)

```
0.2   0 → Σ
0.1   J → j   (J=3)
1.0   LOAD  a_ij
2.0   MPY   b_jk
3.0   ADD   Σ
4.0   STORE Σ
5.0   TX    1.0   j Δ
6.0   STORE C_ik
7.0   TX    0.2   i δ
```

OUTER LOOP
$EFF_{AR} = 80/105 = 76\%$

INNER LOOP
$EFF_{AR} = 26/27 = 96.3\%$

TEMP. REG.

MM_1

MM_2

MM_3

MM_4

FM_1

FM_2

CA_{AR}

CA_{DH}

IM

AR

MAIN BUS

FM (INSTR.) BUS

DECODER BUFFER 4 3 2 1

DECODER

EXECUTION CONTROL

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 M. SEC.