

Cherry Pie

Trial 1.

Add, Sub 0.6
Mpy 1.2
Div 1.8

- Notes:
- 3.5 - assume no look ahead on end of instr 5
 - 4.8 - start M₃ reference for 9 at start of previous with instruction, skipping load or store instructions
 - 4.8 - same for instr 10, except start delayed by 0.2 use
 - 6.0 - In case of instr reference and data reference conflict, take data ref. first
 - 6.2 - start M₄ for instr 12 as soon as 12 hits level 2 in decoder
 - 38.7 Reg'd Mem reference was made by instr 48
 - 40.6 - Instr 53 is assumed to be 0.2 ^{use} long
 - 50.8 Instr 68 has been executed by control decoder.

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Cherry Tree Memory Layout (4 memories)

10/15/56 JEG

		neighbors				
	id	1	2	3	4	
F^n	1	2	3	4	1	
F^{n+1}	2	3	4	1	2	
F^{n+2}	3	4	1	2	3	
U^{n+2}	4	1	2	3	4	
W^{n+2}	1	2	3	4	1	
Z^{n+2}	2	3	4	1	2	
V^{n+2}	3	4	1	2	3	
P^n	4	1	2	3	4	
P^{n+2}	1	2	3	4	1	
E	2	3	4	1	2	
const	3	4	1	2	3	
neighbor distances	L_1, L_2	4	1	2	3	4
	L_3, L_4	1	2	3	4	1

This is an arbitrary memory layout

Cherry Pie

10/16/56

JEG

Inst #	Tag	op	Remarks
1	1	R Add	P ₁
2	3	Sub	B ₃
3		Store F ₁	P ₁₃ (F ₁ , F ₂ mean reference to Fast Memory)
4	2	R Add	B ₂ (any tagged instruction refers to Main Mem)
5	4	Sub	B ₄
6		Store F ₂	B ₂₄
7		Mpy F ₁	P ₁₃ B ₂₄
8		Store F ₁	P ₁₃ B ₂₄
9	2	Load	P ₂
10	4	Sub	P ₄
11		Store F ₂	P ₂₄
12	1	load	B ₁
13	3	Sub	B ₃
14		Store F ₁	B ₁₃
15		Mpy F ₂	P ₂₄ B ₁₃
16		Sub F ₁	P ₁₃ B ₂₄
17		Store F ₂	(P ₁₃ B ₂₄ - P ₂₄ B ₁₃)
18	1	load	r ₁
19	3	Sub	B ₃
20		Store F ₁	r ₁₃
21		Mpy F ₂	P ₂₄
22		Store F ₂	P ₂₄ r ₁₃
23	2	Load	r ₂
24	4	Sub	r ₄
25		Store F ₁	r ₂₄
26		Mpy F ₁	P ₁₃ r ₂₄
27		Sub F ₂	P ₂₄ r ₁₃ - P ₁₃ r ₂₄

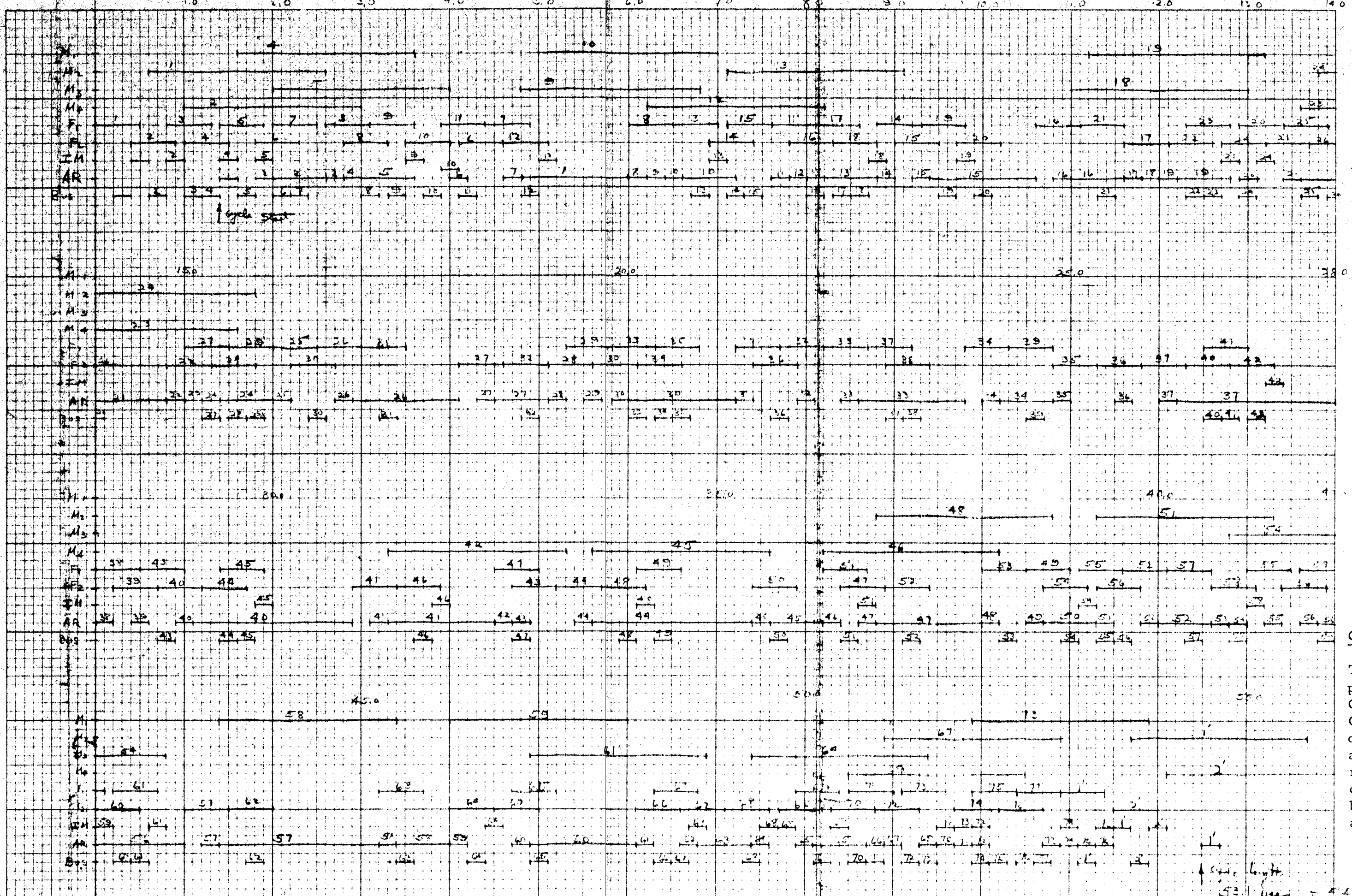
Inst #	Tag	Op	
28		Store F ₂	$(P_2 + r_{13} - P_{13} r_{24})$
29		Load F ₁	r_{13}
30		Mpy F ₂	$r_{13} \beta_{24}$
31		Store F ₁	$r_{13} \beta_{24}$
32		Load F ₁	r_{24}
33		Mpy F ₁	β_{13}
34		Sub F ₁	$r_{13} \beta_{24} - r_{24} \beta_{13} = \Delta$
35		Store F ₂	Δ
36		Load F ₂	$P_2 + r_{13} - P_{13} r_{24}$
37		Div F ₂	Δ
38		Store F ₁	$\frac{\partial P}{\partial \beta}$
39		Load F ₂	$P_{13} \beta_{24} - P_2 + \beta_{13}$
40		Div F ₂	Δ
41		Mpy F ₂	$\frac{\partial P}{\partial r} \Delta t$
42	o	Load	ρ_0
43		Store F ₂	ρ_0 (Store for later use)
44		Div	$\frac{1}{\rho} \frac{\partial P}{\partial r} \Delta t$ (No memory ref necessary)
45	o	Sub	$u^{n-1/2}$
46	o	Store	$u^{n+1/2}$ (Final result)
47		Mpy F ₂	$u^{n+1/2} \Delta t$
48	o	Load	r^n
49		Store F ₁	r^n
50		Add	r^{n+1}
51	o	Store	r^{n+1} (Final result)
52		Add F ₁	$r^n + r^{n+1}$
53		Sub Exp	$\frac{1}{2}(r^n + r^{n+1})$ (Subtract from Exponent)
54	o	Store	$r^{n+1/2}$ (Final result)
55		Load F ₁	$\frac{\partial P}{\partial \beta}$
56		Mpy F ₂	$\frac{\partial P}{\partial \beta} \Delta t$
57		Div F ₂	$\frac{1}{\rho} \frac{\partial P}{\partial \beta} \Delta t$

Inst #	Tag	Op	
58	0	Sub	$w^{n-1/2}$
59	0	Store	$w^{n+1/2}$ (Final result)
60		Mpy F_2	$w \Delta t$
61	0	Load	z^n
62		Store F_2	z^n
63		Add	z^{n+1}
64	0	Store	z^{n+1} (Final result)
65		Add F_2	z^n
66		Sub Exp	$\frac{1}{2}(z^n + z^{n+1})$ (Subtract from Exponent)
67	0	Store	$z^{n+1/2}$ (Final result)
68		Indx Add & Test	against loop end; set selector
69	0	load	l_1, l_2
70		store Addr	l_1
71		shift	
72		st. Addr	l_2
73	0	load	l_3, l_4
74		st. Addr	l_3
75		shift	
76		st. Addr	l_4
77		Tr(Sel)	to inst # 1

Sketch - 10/15/50 JEG

Chasing the Trail

$\frac{53.1 - 5.5}{50} = 10.0\%$
 $\frac{4.6}{23} = 20.0\%$



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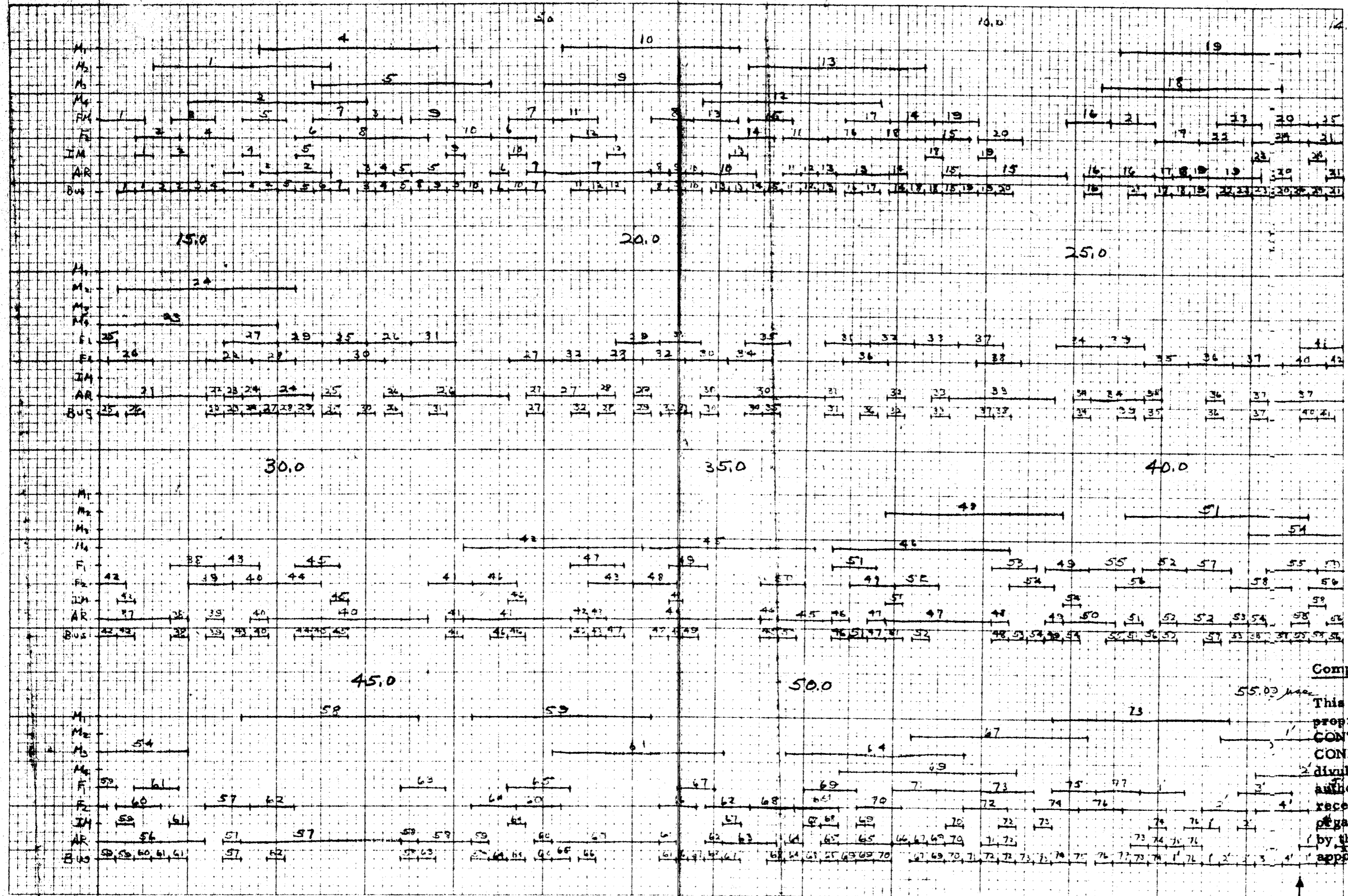
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Scale Length
53.1 - 5.5 = 47.6

CHERRY PIE

assuming:
 1. Same as Trial 1 except that only one bus system exists for all memory and indexing references.



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↑ cycle length = 55.5 - 1.4 (start) = 54.1 usec.

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