

Meeting on STRETCH & Super Stretch Plans
Paughkeeperie Oct 27, 1960

Buchholz - chairman	E. Adams	C. Kraus
Campbell	F. Brooke	EW Pugh
Hoffler	H. Kolesky	M. Klein
Merwin	S. Dunnell	D. Crawford
Cypser	J. Knox	G. Amdahl
Leiner	R. Henley Walsh	

Purpose: To recommend what Corporation should do in area of large scale computers. -- advice to mgmt.

Report on Super Stretch: (Leiner)

- waiting for reply from AEC -- now before commission -- Research proposal to John Pasta interested in cygones
- "100X stretch" -- or "70X stretch"

Looking into Cygones ^{mainly} 1 - to now or year from now
Now laying out 200 cygones: 16 1 bit words - full selection - full access -- address counters - registers - clocking circuits

There is more possible payoff in cyg. -- Pasta is interested
Studies ~~in~~ contract? (1) AEC numerical math, teching?

- not clear how many people. --

- Teller water meeting
- Last Dec - meeting at Quinmore
- proposal
- subsequent meeting

STRETCH (Dennell)

- no formal plans now - must be integrated
- we could now build with $\frac{1}{2}$ components, size ~~etc~~, cost, etc.
eg. 50,000 Trz \rightarrow 15,000 Trz + (30,000 diodes)
+ better low-speed channels (std interface)
- multiple computers: STRETCH + 4 70K's (MITRE)
- parts of problems on each - 2 or other computers?
- simulator of peripheral systems in real time.

DSD's Plans (Proctor)

- next immediate effort will be in lower performance.
\$10,000 per month up (250,000) '80, '90, '90, '94 has been put out.
('90 is only modest machine)
- long range - above 90 - up to STRETCH - compatible with rest of line
- not highest priority (63-'64 amendment)
- (not cryogenics or new tech.)

FSD Plans (Copper)

- accepts resp for design, ^{release} prod. of adv. machine (Super Stretch)
- not the design etc early phases
- Research and/or PSD will do original work;

Refer to Learson's letter: future work will be done on CPFF basis

now Technology... FBR will have to work

(Alana)

cost for complete level: \$100M sales price,

- need a lot more thru-put - large memory, needs to be 10x bigger,
- essential problem: shuffling data back & forth between high speed machine computer net --
- only a factor of 2 increase in present STRETCH frame organization (factor of 5 if all zero)
(20% of time is transmission time now)
- research into cryogenics must go on --

(Hale)

10x faster circuits as possible at present STRETCH circuit costs,
compact circuits, --- size would be smaller --- no change in
machine organization,
--- STRETCH is already fast on common inputs

(Arnold) $\frac{1}{2}$ cost of STRETCH is already in memory

100x machine (needs 10 or 100x as much memory)

intermediate storage -- need much more & high speed?

ARPA possible customer?

(Hale)

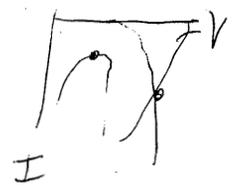
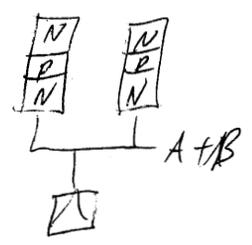
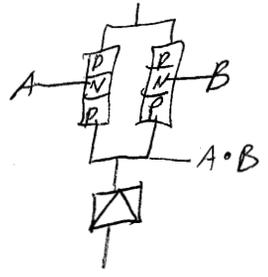
Ⓞ Circuits: DSP-Components -- look at component needs -- will put less
memory -- 0.1 ps cycle on high speed area.

(J. Walsh)

- work on faster circuits
 { faster diodes came in
 { faster transistors.

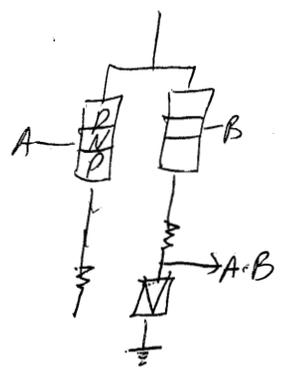
o. (5 nsec circuits) has high power levels,

started Esaki diodes Jan '60



switches fast one way, slow the other

Tried to linearize Esaki diode



GAAS diodes
~~2 nsec~~
 2 nsec delays.

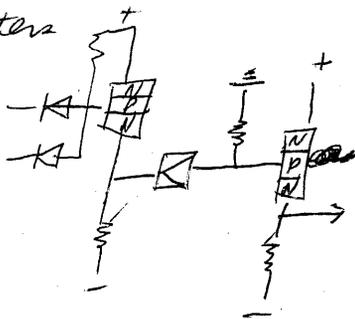
power goes up but is more linear

tolerances are very tight 30mw spread
 - small ~~low~~ voltage DC circts 5% resistors, 3% power supplies.
 - 300mw signal swing,
 → emitter-base drop over T_{22} -- most critical factor



→ 30-40 mWatts per logical block

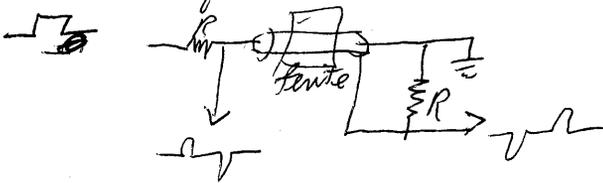
Diodes



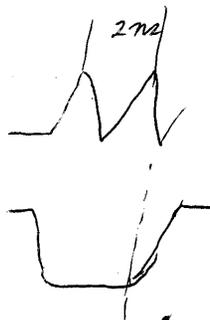
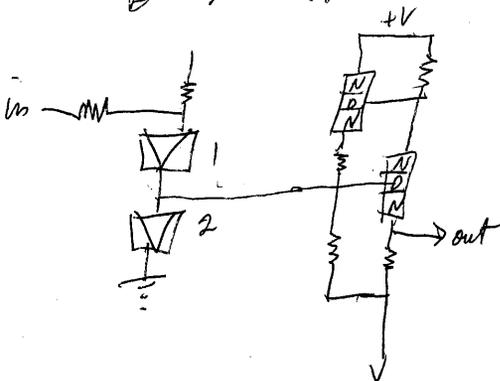
little signals are amplified - large ones are not.

Pulse Transformer:

not too successful -- too much capacitance



Binary Trigger

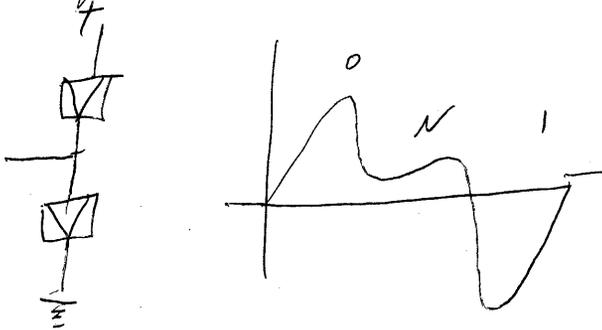


this is overlapped - not really 500Mc
 300 Mc is limit now

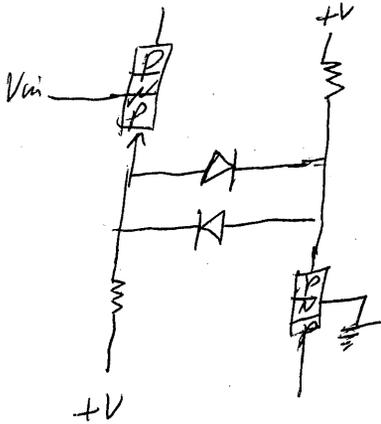
one pulse out for 2 pulses in

Asynchronous Circuits

Required - 3 levels 1 - nothing - 0



3 level current switch - not as fast



Program to Transient Analysis on 610. Emitter diodes - load lines, etc.

expect to ~~be~~ achieve:
100 Mc. with 1 ns delay



RCA folks?
what about ~~RCA~~?
~~we have no advantage~~
- low capacitance diodes
are not common,
(only 14 now in existence)

5 nsec circuits:



rep rate is less
can't start to reduce input signal



1 ns
rep rate higher

packaging may be most
important

(150 to 200 sessions on card) ←

compact ^{card} - 4x8 card - can be used - but not as easy,
- solid state strip lines - on back panel - next extension?

Research will have a high speed machine project regardless
of outside funding,

High Speed Technology is not some or large machine question

Memories: (Crawford)

- restarted advanced development last Dec. (7 eng & technical work)

- partial switching techniques was looked into - 2 cores per bit,
(polarity of difference switching - which was up)

drive circuits: { 1 to 2 amps load voltage 30-35 v
have seen { rise times 8 ns

- driving toward 100 ns full cycle
25 ns switching time

Plans: 77 bit/word 1000 words - next summer - plan to use diode
selection.

{ will build 16 word cross-section this year ←
{ Logic: 5 ns circuits will be used for 16 word

16 K. $\frac{3}{4}$ μ s mem now being worked on

→ - relaxation effect - serious limit after pulse to settle down
eg. 25 ns pulse don't reach disturbed threshold for 20-30 μ s } other materials
at $\frac{3}{4}$ μ s down 30-40% } are ok down to
0.1 μ s

- The above is limit for rep rate on cores

{ 40-50 mvolts signals
- gain needed 10

100ns cycle 10 Mc are questionable now for cores,

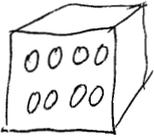
- cores out of thin metallic films (cylinder glass tubing)

- better below 10-15 ns, - less drive current full switching

hope for future

{ signal is variable depending on width

(maybe 1000 word memory will be these)



20 tubes in mil plastic - put, printed wiring

~~erase~~ ~~erase~~ memory

- flat thin film

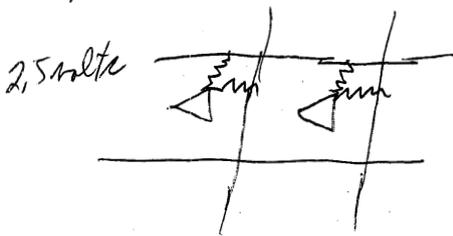
{ 3 or 4 mvolts for flat thin films

Eraser Diode memory

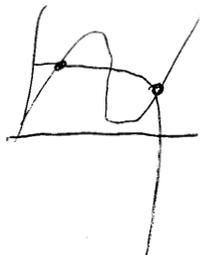
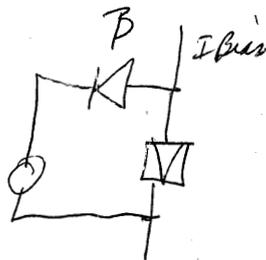
have built: 16 words 32 bit/word,

150 ns cycle -- can be cut in several ways,

"parallel-parallel" selection



amt of current in a cell depends on state -- variable load on driver (serious problem)



got good pulse for 1, very little for 0,

may go to 50 ns

Read only memory -- will look into next year -- lower cost, -- study effort,

Flat thin films (Hughes)

competition is up on us

Sperry Rand,

1000 w/d 50ms, memory now being discussed,
low level outputs, (maybe 30ms) - so really 100ms

100ms within 1 year ← target of Junch Lab.

50 x 50 bit
w/d

Hughes - multilayered films? plated toroids

1.5 KMc Transistors can be made at not too much
additional cost. -- very small -- in 1 year
- cheap packaging is important, (device cost 1¢ ea - package much more)
silicon-passivating circuits? - glass - cut cost of headers,
"surface passivation"

NPN Mesa Transistors -- fastest in quantity now.

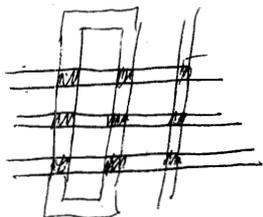
Cryogenics (Littner)

ADL plans to build small Assoc mem.
STL?

- costwise would be quite favorable -- if it can be accomplished in large quantities,

Model for circuits -- optimum,

assume $\rho_s = .007$
 $d = \text{insulation thickness } 5000 \text{ \AA}$



$F_i = \text{fan in of 2 (4 controls) 4 gates}$
 $F_o = \text{fan out of 4 (8 controls) 4 1st 2 gates}$
 4 2nd controls
 3 gates

2L/R for loop.

- | | | |
|--|--------|-------------------|
| 1. unbiased crossed film
(4 to 1 crossing ratio.) | 120 ns | 12 cryotrons/loop |
| 2. biased crossed films | 10 ns | |
| 3. In-line cryotrons | 5 ns | |

Perhaps gain factor of 2 with thinner insulation - ^{unknown} Time scale?
" " 2.5 with alloys - by end of year '61,

So may get to 1 or 2 ns

Inductance of line = $L \sim (d+l) \left(\frac{l}{w} + 1 \right)$

Resistance of line = $R \sim \rho_s \frac{l}{w}$

↑
assumes
1 width
between
cryotrons.

$\lambda = \text{penetration depth into film}$
{ 500 \AA lead
{ 1500 \AA alloys, etc

$l = \text{length of cryotron}$
 $w = \text{width}$

$$\frac{L}{R} \sim \frac{d+l}{\rho_s} \left(1 + \frac{w}{l} \right)$$

$$H = 300 \left(1 - \frac{t_c^2}{t_{emp}} \right)$$

Power dissipation: per switch = $\frac{1}{2} L i^2$

constant switching = $\frac{\frac{1}{2} L i^2}{24R} = \frac{1}{4} i^2 R = \frac{1}{2} i^2 \left(\frac{L}{R} \right)$
 ↑ ↑
 these can be changed

Δ insulation thickness	R_s needed for 1ms	
500°A	.014	.007 ohms/sq is value for Tin being used now.
1000	.017	
2000	.023	
5000	.041	

Field $H = \frac{4\pi I}{w}$
 $w \leftarrow .006'' \text{ width}$
 6-8 oersteds nominal value

so $I \approx 100 \text{ ma}$

$i^2 \approx 10^{-2} \quad \frac{L}{R} \approx 10^2$

Power = $\frac{P_s}{4} \approx \underline{5 \text{ watts/cryotron}}$ (100 millamp switching $\frac{1}{2} \text{ ms}$)

or 200 cryotrons/watt 1 watt \approx present cryostats

if one gate in each loop were being used ~~all the time~~ all the time,

$\frac{2 \times 10^2}{2 \times 10^5} = .001$ efficiency,

1 watt in the watt need 3 horsepower motor

- now considering 4" x 4" substrates,

3 watts - 5 hp.

→ by next June '61 will know how well it works

(Klaus) 40 bit mem, has been built at Kingston

135. $2 \times 1 \frac{5}{8}''$ 19 preparations tolerance $\pm 15\%$

\rightarrow will need $\frac{1}{4}$ mil registration eventually, $\sim \frac{1}{8}$ part area

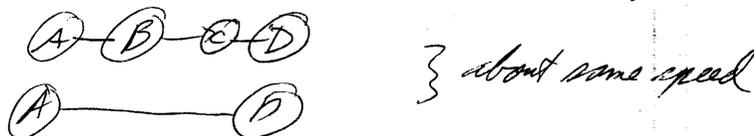
3 μ s read cycle } present speeds.
4 μ s read-write cycle }

(Lena) Problems! (1) coupling high speed internal with slow external -- variable speeds of cytrons may be useful

6 mil $w = l$

40 to 50 bits / sq in for regular memory array
 \sim half for other circuitry,

- linear distance between exit gate & gate being driven counts:



circuit speed \sim perimeter of the plate

So machine would have to be organized into little units, interplane connections? -- AMS leads have been done, -- requires considerable power,

(2) cross over problem -- connecting planes elements together

- no. of layers is serious problem -- { 20 or more layers of circuits

- cytrons seem to be more promising for small memories than for large memories, - switching circuitry are same as mem. layout
- larger memories will be slow $\sim 10 \mu$ s (200,000 words $\& \mu$ s)

speed depends on shape of circuits not size??

2000 per square inch - present core densities }
0.30 per linear inch

it. This is much better than computers now.

1.2×10^6 bits $5'' \times 5'' \times 24''$ = core memory now.

External Storage:

- new tapes - plated tapes are coming along.
- TRACTOR: 3000 bits/inch 10% phase shift
- plated tape: 4500 bits/inch no detectable phase shift.

nothing in works now

Disk: 50 micron separation being sought between disks & head

Magnetic strip -

transfer from drum to tape



Coding memory:

- different length delay lines
- get equiv of tape with zero start time

-
- continue to push high speed computers & computers.
 - recognize that IBM will build a super machine.
 - must at least match RCA
 - machine organization
 - shall observe STRIPS
 - problem studies
 - Applications studies in SDP

Lighting: 1965 ~~the~~ megabyte
- Rem Rand Thin film
- RCA ~~the~~ tunnel diode (microwaves earlier)
IBM cryogenics -- have been pushed --
(no working hardware was shown)

RCA will no doubt get contract. --

(Rem Rand - memory - RCA - logic)

IBM might be able get
if cryogenic.

Burroughs -- a special machine

Recommendations:

1. Now is the time to get a machine study contract
2. Continue to support high speed circuits & memories dev.
3. IBM will build a 10x to 100x machine
4. Don't let make AEC & NSF make the same again
5. Application studies be undertaken

JCG Oct 31,

above are trade point? Policy 100% by govt money in FSD,
except for component res. But this can be violate in specific areas,
eg, files, memories -- might be DSD,

But 100% funding can't hold since IBM is going to work
in areas anyway -- cost sharing? when time comes, -- CMC will
decide. Will DSD give up or not?