Detailed instruction breakdown

Steps in Execution

Floating load

| | | |
|---|---|---|
| 1. | I Box Memory address Bus (fetch by IC to $Y_1$) | 0.4 |
| 2. | Mem bus Control Unit & Bus in | 0.4 |
| 3. | Memory Read out | 1.0 |
| 4. | Mem bus out, Control & Control Bus out to $Y_1$ | 0.2 |
| 5. | Checker $Y_1 \rightarrow Y_1$ | 0.4 |
| 6. | Read out $\overset{\text{x mem}}{\text{input}}$ $Y_1$, Readout $Y_{1L}$ | 0.4 |
| 7. | Add +put in $Z_R$ | 0.4 |
| 8. | Send IC, etc, to LA | 0.4 |
| 9. | I Box Mem address bus (fetch operand out to $Z_R$) | 0.4 |
| 10. | Mem bus Control & Bus in | 0.4 |
| 11. | Mem Read out | 1.0 |
| 12. | Mem bus out, Control & bus out to LA(+Y) | 0.2 |
| 13. | Check operand = | 0.4 |
| 14. | Start arithmetic operation if possible. | 6.0 |

(Refer to timing chart)

# Load index

## from External Memory

| | | |
|---|---|---|
| 1. | IBox Mem address bus (fetch $Z_{0A}$ to $Y_1$ or $Y_2$) | 0.4 μs |
| 2. | Mem Bus Control, Bus in, Mem RO, Bus out etc | 1.6 μs |
| 3. | Fetch Index per $Z_J$ | 0.4 |
| 4. | Check & send X to LA | 0.4 |
| 5. | Check Y to X | 0.4 |
| 6. | Clear Index per $Z_J$ | 0.4 |
| 7. | Store Index per $Z_J$ | 0.4 |
| 8. | Send Ind Reg to LA | 3.2 μs |

## from Index Memory.

1. IBox Mem address bus (fetch $Z_{0A}$ to Y)
2. Fetch Index (X Mem to X
3. Check X to Y
3. Fetch Index Index per $Z_J$
4. check & send x to LA
5. Check Y to X
6. Clear Index
7. Store Index.
8. Send Ind to LA

Also go thru Incr, Count, & Refill.